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A High Resolution and High Accuracy R-2R DAC Based on Ordered Element Matching

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***Abstract*—Random mismatch errors in the resistor networks are one of the dominant nonlinearity sources for high resolution and high accuracy resistor DACs. This paper applies the theory of ordered element matching in a high resolution segmented R-2R DAC. It can achieve high matching accuracy by regrouping the resistors in the MSB array according to their resistance ranks obtained by the INL test. The implementation only requires adding some additional digital circuits to the typical design. A behavioral model of 18-bit segmented R-2R DAC is created in MATLAB. The statistical results show a significant resistor area reduction compared with state of the art.**

I. INTRODUCTION

Up until now, the performance of digital circuits is constantly enhanced by the scaling of device dimension and supply voltage. However, the technology advancement does not benefit many analog and mixed-signal circuits and in fact it poses higher requirements on their performance. Digital-to-analog converter (DAC) is one of the circuits facing high performance demand in high-resolution high-accuracy signal processing and telecommunication applications.

The R-2R DACs offer high resolution and simple structure, which makes them easy to realize and widely used. Fig.1 illustrates a typical structure of the current-output segmented R-2R DAC which is extensively used in high accuracy applications such as sensors and digital instruments.

However, the accuracy of a R-2R DAC is very sensitive to the matching performance of the resistor networks. Yet, the integrated-circuit (IC) fabrication technology always produces imperfectly matched resistors and with the process scaling the random mismatch errors deteriorate significantly [1]-[2]. Therefore, random mismatch is regarded as one of the major sources of errors that degrade the linearity and yield performance of a R-2R DAC.

The most straightforward approach to reduce random mismatch errors is to enlarge the area of R-2R DAC. From [3], 1-bit linearity enhancement will lead to a quadruple of circuit area, which is a huge cost increase especially for the high resolution designs. Moreover, parasitic capacitance effects of the large size devices undermine the performance of the DACs and often bring up more power consumption [4].

Additionally, several other techniques can be applied to compensate random mismatch errors for R-2R DACs. The most popular one is trimming technique, which could be mainly divided into two categories: the laser-trimming and fuse-trimming. Laser-trimming employs the laser beams to accurately adjust the resistor parameters at the wafer level; while fuse trimming utilizes the fuse or anti-fuses for opening or closing the interconnections of a network of resistive

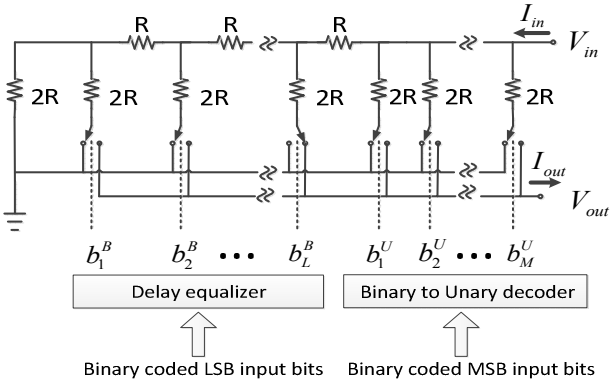


Figure 1. Current-output segmented R-2R DAC

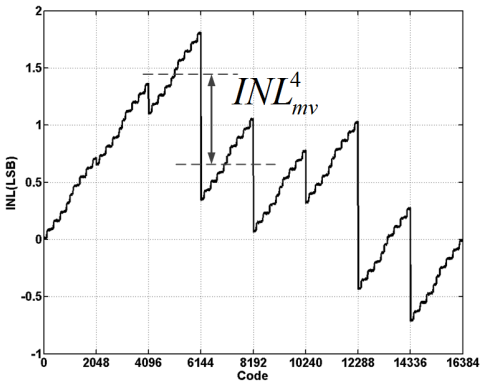
elements to minimize the mismatch errors. Unfortunately, this technique usually demands high expenses such as extra layer or more die area for trim-pads and the achieved accuracy is reduced by the temperature and aging effects [5].

Besides these, calibration is another popular technique, but it is mainly used in other types of DACs. It could cut down the mismatch errors by feed-back signals from error measuring circuits such as a high-resolution high-accuracy analog-to-digital converter (ADC) [6]-[7]. Due to its design complexity, this technique is rarely used in R-2R DACs.

Ordered element matching (OEM) theory [3] showed the capability of significantly reducing the random mismatch errors in unary weighted circuit components. By combining and grouping components with complementary mismatch errors together, the total random mismatch errors could be cut down. It mainly consists of two steps, firstly sort the circuit components according to their parameter magnitudes, and then pair and sum the complementary ordered components (which is called "folding" operation). The random mismatch errors can be further decreased if the folding operation continues and eventually transforms the unary weighted array into a binary weighted array, which is called "complete folding" [3] [8].

In this paper, a novel segmented R-2R DAC design based on OEM theory is presented. We get the order of unary weighted resistors from the INL test and implement complete folding according to their order. Statistical results based on MATLAB model show that an 18-bit segmented R-2R DAC achieves the same accuracy in much smaller resistor area compared to state of the art.

This paper is organized as follows. In Section II, the OEM based R-2R DAC is presented in details. The MATLAB behavioral model and statistical results are provided in Section III. Finally the conclusion is drawn in Section IV.



Fiugre 2. INL curve of 14 bits current-output with 3-11 segmentation R-2R DAC

II. R-2R DAC BASED ON OEM

A. Analysis of the typical R-2R DAC

The current-output segmented R-2R DAC often consists of unary weighted bits ($b_1^U - b_M^U$) and binary weighted bits ($b_1^B - b_L^B$). The former part is often called the most significant bit (MSB) array, whereas the other part is named as the least significant bit (LSB) array as shown in Fig.1. The MSB input bits need a binary to unary decoder, while the delay equalizer is used to align the timing of LSB with the MSB bits.

Based on the accurate matched resistors, the output current can be calculated as:

$$I_{out} = I_{in}\left(\sum_{k=1}^{L}\frac{b_k^B}{2^{k+\sum_{i=1}^{M} b_i^U}} + \sum_{k=1}^{M}\frac{b_k^U}{2^{1+\sum_{i=1}^{M} b_i^U}}\right) \tag{1}$$

where, I_{in} is the input current, and L and M are the resolutions of LSB and MSB array, respectively. It is well-known that the R-2R DAC's accuracy is mainly decided by the matching level of the resistors in the MSB array. As a result, most of our works in this paper focus on minimizing the MSB resistor mismatch errors.

B. Resistor order extractions from INL test

It is easy to simplify (1) into:

$$I_{out} = V_{in} \times \left(\frac{1}{\mathrm{Re}(b_1^B \ldots b_L^B)} + \sum_{k=1}^{M}\frac{b_k^U}{R_k^M}\right) \tag{2}$$

where, V_{in} is the input voltage; R_k^M is the kth MSB resistor value; Re is the equivalent resistor value of LSB array and it is determined by the binary weighted bits.

If we arbitrarily choose one digital input code D1 where its first T unary weighted MSB bits set to '1' and the rest of unary weighted bits set to '0', the output current at D1 is:

$$I_{out}^{'} = V_{in} \times \left(\frac{1}{\mathrm{Re}(b_1^B \ldots b_L^B)} + \sum_{k=1}^{T}\frac{1}{R_k^M}\right) \tag{3}$$

Now define another input code as D2 where we switch the (T+1)th unary bit from '0' to '1' and keep all other bits the same, the output current changes to:

$$I_{out}^{"} = V_{in} \times \left(\frac{1}{\mathrm{Re}(b_1^B \ldots b_L^B)} + \sum_{k=1}^{T+1}\frac{1}{R_k^M}\right) \tag{4}$$

Subtract (3) from (4):

$$I_{out}^{"} - I_{out}^{'} = V_{in} \times \frac{1}{R_{T+1}^M} \tag{5}$$

From (5) the value of the (T+1)th MSB resistor (R_{T+1}^M) could be estimated by measuring the difference of output current when switching (T+1)th unary bit from 0 to 1.

Now considering the INL test, the INL at digital input code D can be written as:

$$INL(D) = \frac{I_{out}(D) - I_{out}(0)}{[I_{out}(N) - I_{out}(0)]/N} - D \tag{6}$$

where, $N = 2^n - 1$ and n is the DAC's resolution. If we write the INL at D1 as:

$$INL^T_{b_1^B \ldots b_L^B} = INL\left(\sum_{k=1}^{L} b_k^B \times 2^{k-1} + \sum_{k=1}^{T} 2^L\right) \tag{7}$$

and assuming $I_{out}(0) = 0$, then (7) equals to:

$$INL^T_{b_1^B \ldots b_L^B} = \frac{I_{out}\left(\sum_{k=1}^{L} b_k^B \times 2^{k-1} + \sum_{k=1}^{T} 2^L\right)}{I_{out}(N)/N} - \left(\sum_{k=1}^{L} b_k^B \times 2^{k-1} + \sum_{k=1}^{T} 2^L\right) \tag{8}$$

Similarly, we can write the INL at D2 as:

$$INL^{T+1}_{b_1^B \ldots b_L^B} = \frac{I_{out}\left(\sum_{k=1}^{L} b_k^B \times 2^{k-1} + \sum_{k=1}^{T+1} 2^L\right)}{I_{out}(N)/N} - \left(\sum_{k=1}^{L} b_k^B \times 2^{k-1} + \sum_{k=1}^{T+1} 2^L\right) \tag{9}$$

then, subtract (8) from (9), and take (5) into the equation:

$$\begin{aligned} INL^{T+1}_{b_1^B \ldots b_L^B} - INL^{T}_{b_1^B \ldots b_L^B} &= \frac{I_{out}^{"} - I_{out}^{'}}{I_{out}(N)/N} - 2^L \\ &= \frac{V_{in}/R_{T+1}^M}{I_{out}(N)/N} - 2^L \end{aligned} \tag{10}$$

Based on (10), it is obvious that the (T+1)th MSB resistor (R_{T+1}^M) could be estimated by evaluating the INL difference when (T+1)th unary bit change from 0 to 1.

Additionally, in order to minimize the noise effect, we will keep the unary bits of D1 and D2 unchanged but sweep their binary bits ($b_1^B - b_L^B$) from all '0' to all '1', and then calculate the average difference of INL as:

$$\begin{aligned} INL_{mv}^{T+1} &= \overline{INL^{T+1}_{b_1^B \ldots b_L^B}} - \overline{INL^{T}_{b_1^B \ldots b_L^B}} \\ &= \frac{\overline{I_{out}^{"}} - \overline{I_{out}^{'}}}{I_{out}(N)/N} - 2^L = \frac{V_{in}/\overline{R_{T+1}^M}}{I_{out}(N)/N} - 2^L \end{aligned} \tag{11}$$

where, $\overline{INL^{T+1}_{b_1^B \ldots b_L^B}}$ and $\overline{INL^{T}_{b_1^B \ldots b_L^B}}$ are the intended average INLs for D1 and D2, respectively; $\overline{I_{out}^{"}}$ and $\overline{I_{out}^{'}}$ are the related output currents. Then, a more accurate estimation for (T+1)th MSB resistor ($\overline{R_{T+1}^M}$) can be obtained .

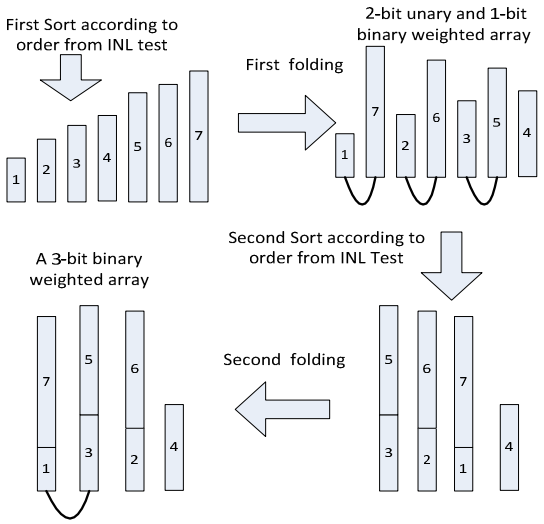


Figure 3. Complete folding for a 3-bit unary weighted resistors array

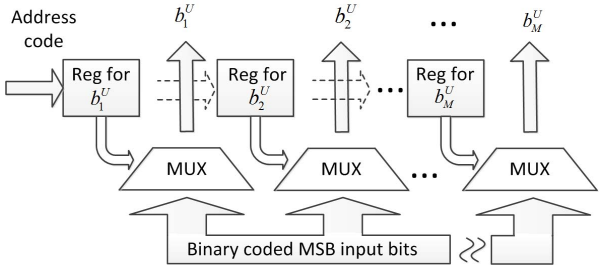


Figure 4. Register and mux array

From (11), it is clear that all the unary resistors can be ranked from the INL test. To illustrate this concept, we will take a 14-bit R-2R DAC with 3-11 segmentation as an example. Fig. 2 shows an INL curve of this DAC model. By measuring the average INL difference between two MSB bit transitions, it could estimate the corresponding MSB resistor value. If we repeat this process, all the unary MSB resistors can be ranked according to their magnitudes.

C. Resistor reorganization by complete-folding

As illustrated in Fig.3, each rectangle denotes a resistor with random mismatch error. Based on INL test, all MSB resistors are sorted according to their magnitudes. Next, all the complementary ordered resistors are paired, and only the resistor in the middle is left alone. This operation is called one "folding" [3]. In this way, the original 3-bit unary coded resistor array is converted into a 2-bit unary-weighted and 1-bit binary-weighted array. In details, the resistor value of each 2-bit unary weighted array is nearly twice of the last single resistor, and the random variations in resistors are reduced.

The mismatch errors are consistently diminishing after each folding operation. As shown in Fig.3, if the INL test and single folding operation are repeated until the 3-bit unary weighted array is converted into 3-bit binary weighted array, the mismatch errors are further reduced. This process is so-called "complete-folding" [3].

In [8], the complete-folding technique was introduced for current-steering DACs. It requires an accurate analog comparator to measure the difference between the currents to rank all the MSB current sources. However, in this paper, the ranks of resistors are directly obtained from the INL test, so there is no requirement for additional analog circuitry and we only need replace the binary-to-unary decoder with a register and mux array as shown in Fig. 4. Then, each MSB resistor contains one mux and register. The address code obtained from the complete-folding operation is stored into each register, and based on those codes the MUX chooses the appropriate input bit to control the corresponding MSB resistor. The register and mux array can easily be implemented and they scale with the IC technology.

III. MATLAB SIMULATION RESULTS

A MATLAB model of an 18-bit current output R-2R DAC with 7-11 segmentation is built based on Fig. 1 to verify the OEM based matching performance. In order to compare with state of the art, three types of R-2R DAC models are included, i.e., the original DAC without any mismatch compensation, the trimmed DAC with technique presented in [9], and the OEM based DAC proposed in the last section.

Before anything, it is worth mentioning the setup of each DAC model. The original DAC just utilizes large resistor area to compensate random mismatch errors. In [9] the new laser trimming technique allows trimming MSB resistors with at least 48-ppm accuracy over a range about 0.1%. The trimmed DAC model uses this technique but increases the trimming accuracy from 48-ppm to 10-ppm in the simulations. This change will bring up the implementation cost. The OEM based DAC needs 6-time folding operations, and 24 extra MSB resistors are included for outlier elimination to discard the large defects in the design as presented in [3].

In Fig. 5, it shows DNL and INL distributions of 10,000 randomly generated 18-bit DACs with standard deviation $\sigma = 0.021\%$ for each DAC model. From the comparisons, the OEM based R-2R DAC achieves much better accuracy for the same relative unit resistor standard deviation.

Fig. 6 indicates the yield estimations by Monte Carlo simulation with DNL < 0.5 LSB and INL <0.5 LSB for all three DAC models. In order to achieve yield >99.7% with INL <0.5 LSB, we can get the required standard deviation of the unit resistor for each model from Fig. 6(b). Then the area deduction factor can be calculated based on these standard deviations, and the results are concluded in TABLE 1. As one can see, for the same yield requirement the proposed R-2R DAC has as large as 196 area reduction factor! Since the mismatch error is dominated by the LSB array in the simulation model, the area reduction factor can be improved much more if we assign different areas for LSB and MSB arrays.

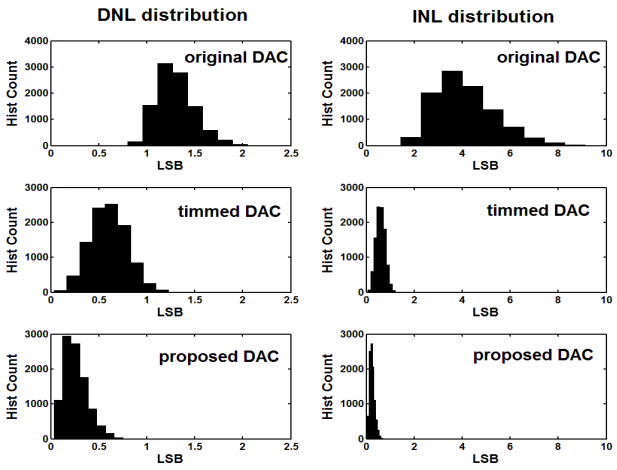


Figure 5. DNL and INL distribution comparison of 10,000 randomly generated resistor arrays in18-bit R-2R DAC with $\delta = 2.1\times10^{-4}$

Furthermore, the OEM based DAC has big advantages in implementation. The trimmed DAC requires special process, and accurate test equipment, all of which demand high cost. In comparisons, the OEM based DAC only needs to add some digital circuits to the original design, which can easily be implemented with the modern IC technologies. Besides these, we can measure INL on-chip for some BIST applications so that the mismatch errors can be continuously corrected using our technique. Alternatively, we can obtain the optimal groupings based on the INL test at productions. In this case, similar to the traditional trimming technique, it will not account for the temperature and aging effects, but the implementation cost is greatly reduced.

IV. CONCLUSION

In this paper, a novel high resolution and high accuracy R-2R DAC based on OEM theory has been presented. It achieves high accuracy by re-grouping the MSB resistors corresponding to their magnitude orders obtained from the INL test. Its implementation only requires adding some digital circuits into the traditional design. A MATLAB behavioral model of 18-bit segmented R-2R DAC is created. The statistical results show that the proposed R-2R DAC can achieve very high accuracy in a much smaller real estate compared to state of the art.

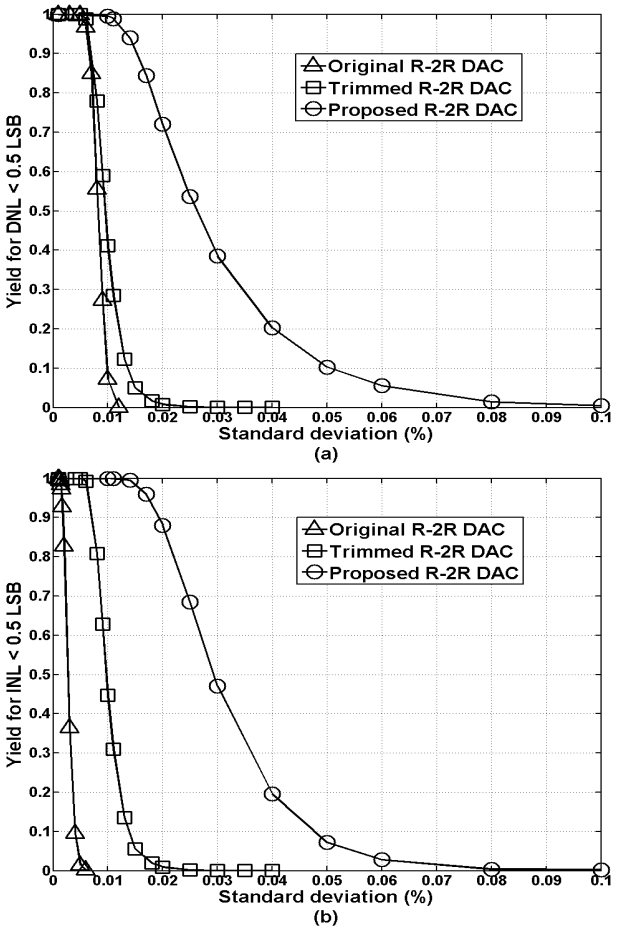


Figure 6. Yield comparisons of 18-bit segmented R-2R DACs with (a) DNL<0.5LSB and (b) INL<0.5LSB

TABLE1. REQUIRED STANDEARD DEVIATION AND AREA DEDUCTION FOR YIELD>99.7% WITH INL<0.5LSB

Types of 18-bit R-2R DAC	Standard deviation (%)	Area deduction factor
Original R-2R DAC	0.001	1
Trimmed R-2R DAC	0.005	25
Proposed R-2R DAC	0.014	196

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