LINEAR INTEGRATED CIRUITS

SYLLABUS

EC 2254   **LINEAR INTEGRATED CIRCUITS**   **3 0 0 3**

AIM:

To teach the basic concepts in the design of electronic circuits using linear integrated circuits and their applications in the processing of analog signals.

OBJECTIVES
- To introduce the basic building blocks of linear integrated circuits.
- To teach the linear and non-linear applications of operational amplifiers.
- To introduce the theory and applications of analog multipliers and PLL.
- To teach the theory of ADC and DAC
- To introduce the concepts of waveform generation and introduce some special function ICs.

UNIT - I   IC FABRICATION AND CIRCUIT CONFIGURATION FOR LINEAR ICS

9

Advantages of ICs over discrete components – Manufacturing process of monolithic Ics – Construction of monolithic bipolar transistor – Monolithic diodes – Integrated Resistors – Monolithic Capacitors – Inductors. Current mirror and current sources, Current sources as active loads, Voltage sources, Voltage References, BJT Differential amplifier with active loads, General operational amplifier stages -and internal circuit diagrams of IC 741, DC and AC performance characteristics, slew rate, Open and closed loop configurations.

UNIT - II   APPLICATIONS OF OPERATIONAL AMPLIFIERS   9

Sign Changer, Scale Changer, Phase Shift Circuits, Voltage Follower, V-to-I and I-to-V converters, adder, subtractor, Instrumentation amplifier, Integrator, Differentiator, Logarithmic amplifier, Antilogarithmic amplifier, Comparators, Schmitt trigger, Precision rectifier, peak detector, clipper and clamper, Low-pass, high-pass and band-pass Butterworth filters.

UNIT - III   ANALOG MULTIPLIER AND PLL   9

Analog Multiplier using Emitter Coupled Transistor Pair - Gilbert Multiplier cell - Variable transconductance technique, analog multiplier ICs and their applications, Operation of the basic PLL, Closed loop analysis, Voltage controlled oscillator, Monolithic PLL IC 565, application of PLL for AM detection, FM detection, FSK modulation and demodulation and Frequency synthesizing.

UNIT - IV   ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS   8

Analog and Digital Data Conversions, D/A converter – specifications - weighted resistor type, R-2R Ladder type, Voltage Mode and Current-Mode $R\text{-}2R$ Ladder types - switches for D/A converters, high speed sample-and-hold circuits, A/D Converters – specifications - Flash type - Successive Approximation type - Single Slope type - Dual Slope type - A/D Converter using Voltage-to-Time Conversion - Over-sampling A/D Converters.

UNIT - V   WAVEFORM GENERATORS AND SPECIAL FUNCTION ICs   9

Sine-wave generators, Multivibrators and Triangular wave generator, Saw-tooth wave generator, ICL8038 function generator, Timer IC 555, IC Voltage regulators - Three terminal fixed and adjustable voltage regulators - IC 723 general purpose regulator - Monolithic switching regulator, Switched capacitor filter IC MF10, Frequency to Voltage and Voltage to Frequency converters, Audio Power amplifier, Video Amplifier, Isolation Amplifier, Opto-couplers and fibre optic IC.

TOTAL : 45 PERIODS

TEXT BOOKS:

1. Sergio Franco, Design with operational amplifiers and analog integrated circuits, 3rd Edition, Tata McGraw-Hill, 2007.
2. D.Roy Choudhry, Shail Jain, Linear Integrated Circuits, New Age International Pvt. Ltd., 2000.

REFERENCES:

1. B.S.Sonde, System design using Integrated Circuits , New Age Pub, 2nd Edition, 2001
2. Gray and Meyer, Analysis and Design of Analog Integrated Circuits, Wiley International, 2005.
3. Ramakant A.Gayakwad, OP-AMP and Linear ICs, Prentice Hall / Pearson Education, 4th Edition, 2001.
4. J.Michael Jacob, Applications and Design with Analog Integrated Circuits, Prentice Hall of India, 1996.
5. William D.Stanley, Operational Amplifiers with Linear Integrated Circuits, Pearson Education, 2004.
6. K Lal Kishore, Operational Amplifier and Linear Integrated Circuits, Pearson Education, 2006.
7. S.Salivahanan & V.S. Kanchana Bhaskaran, Linear Integrated Circuits, TMH, 2008.

UNIT -I

IC FABRICATION AND CIRCUIT CONFIGURATION FOR LINEAR ICs

Integrated Circuits:

An integrated circuit (IC) is a miniature, low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon. The active components are transistors and diodes and passive components are resistors and capacitors.

Advantages of integrated circuits:

Miniaturization and hence increased equipment density.

Cost reduction due to batch processing.

Increased system reliability due to the elimination of soldered joints.

Improved functional performance.

Matched devices.

Increased operating speeds.

Reduction in power consumption

Classification:

Integrated circuits can be classified into analog, digital and mixed signal (both analog and digital on the same chip). Based upon above requirement two different IC technology namely Monolithic Technology and Hybrid Technology have been developed. In monolithic IC ,all circuit components ,both active and passive elements and their interconnections are manufactured into or on top of a single chip of silicon. In hybrid circuits, separate component parts are attached to a ceramic substrate and interconnected by means of either metallization pattern or wire bounds.
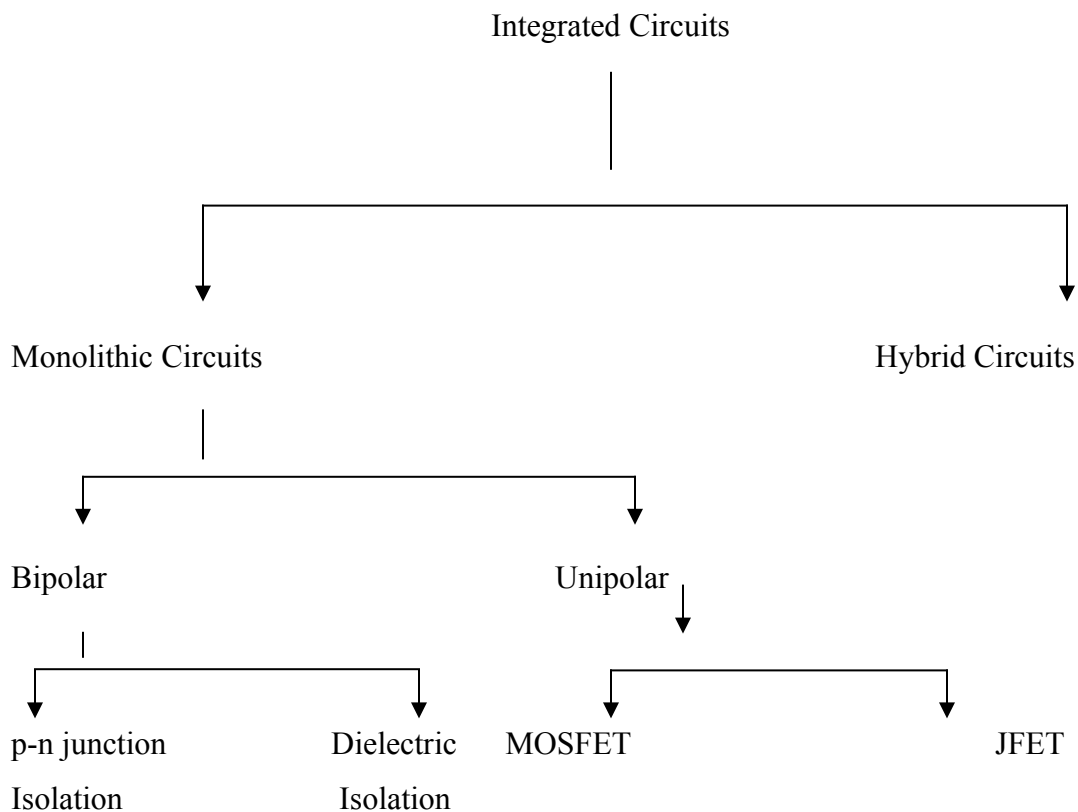
Digital integrated circuits can contain anything from one to millions of logic gates, flip-flops, multiplexers, and other circuits in a few square millimeters. The small size of these circuits allows high speed, low power dissipation, and reduced manufacturing cost compared with board-level

integration. These digital ICs, typically microprocessors, DSPs, and micro controllers work using binary mathematics to process "one" and "zero" signals.

Analog ICs, such as sensors, power management circuits, and operational amplifiers, work by processing continuous signals. They perform functions like amplification, active filtering, demodulation, mixing, etc. Analog ICs ease the burden on circuit designers by having expertly designed analog circuits available instead of designing a difficult analog circuit from scratch.

ICs can also combine analog and digital circuits on a single chip to create functions such as A/D converters and D/A converters. Such circuits offer smaller size and lower cost, but must carefully account for signal interference

Classification of ICs:

```
                          Integrated Circuits
                                  |
           ┌──────────────────────┴──────────────────────┐
           ▼                                              ▼
   Monolithic Circuits                              Hybrid Circuits
           |
     ┌─────┴─────┐
     ▼           ▼
   Bipolar     Unipolar
     |              |
  ┌──┴──┐        ┌──┴──┐
  ▼     ▼        ▼     ▼
p-n junction  Dielectric  MOSFET        JFET
Isolation     Isolation
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Generations

SSI, MSI and LSI

The first integrated circuits contained only a few transistors. Called "Small-Scale Integration" (SSI), digital circuits containing transistors numbering in the tens provided a few logic gates for example, while early linear ICs such as the Plessey SL201 or the Philips TAA320 had as few as two transistors. The term Large Scale Integration was first used by IBM scientist Rolf Landauer when describing the theoretical concept, from there came the terms for SSI, MSI, VLSI, and ULSI. They began to appear in consumer products at the turn of the decade, a typical application being FM inter-carrier sound processing in television receivers.

The next step in the development of integrated circuits, taken in the late 1960s, introduced devices which contained hundreds of transistors on each chip, called "Medium-Scale Integration" (MSI).

They were attractive economically because while they cost little more to produce than SSI devices, they allowed more complex systems to be produced using smaller circuit boards, less assembly work (because of fewer separate components), and a number of other advantages.

VLSI

The final step in the development process, starting in the 1980s and continuing through the present, was "very large-scale integration" (VLSI). The development started with hundreds of thousands of transistors in the early 1980s, and continues beyond several billion transistors as of 2007.

In 1986 the first one megabit RAM chips were introduced, which contained more than one million transistors. Microprocessor chips passed the million transistor mark in 1989 and the billion transistor mark in 2005

ULSI, WSI, SOC and 3D-IC

To reflect further growth of the complexity, the term ULSI that stands for "Ultra-Large Scale Integration" was proposed for chips of complexity of more than 1 million transistors.

Wafer-scale integration (WSI) is a system of building very-large integrated circuits that uses an entire silicon wafer to produce a single "super-chip". Through a combination of large size and reduced packaging, WSI could lead to dramatically reduced costs for some systems, notably

massively parallel supercomputers. The name is taken from the term Very-Large-Scale Integration, the current state of the art when WSI was being developed.

System-on-a-Chip (SoC or SOC) is an integrated circuit in which all the components needed for a computer or other system are included on a single chip. The design of such a device can be complex and costly, and building disparate components on a single piece of silicon may compromise the efficiency of some elements.

However, these drawbacks are offset by lower manufacturing and assembly costs and by a greatly reduced power budget: because signals among the components are kept on-die, much less power is require. Three Dimensional Integrated Circuit (3D-IC) has two or more layers of active electronic components that are integrated both vertically and horizontally into a single circuit. Communication between layers uses on-die signaling, so power consumption is much lower than in equivalent separate circuits. Judicious use of short vertical wires can substantially reduce overall wire length for faster operation.

Construction of a Monolithic Bipolar Transistor:

The fabrication of a monolithic transistor includes the following steps.

1. Epitaxial growth
2. Oxidation
3. Photolithography
4. Isolation diffusion
5. Base diffusion
6. Emitter diffusion
7. Contact mask
8. Aluminium metallization
9. Passivation

The letters P and N in the figures refer to type of doping, and a minus (-) or plus (+) with P and N indicates lighter or heavier doping respectively.

1. Epitaxial growth:

The first step in transistor fabrication is creation of the collector region. We normally require a low resistivity path for the collector current. This is due to the fact that, the collector contact is normally taken at the top, thus increasing the collector series resistance and the $V_{CE(Sat)}$ of the device.

Epitaxial layer
(N layer)
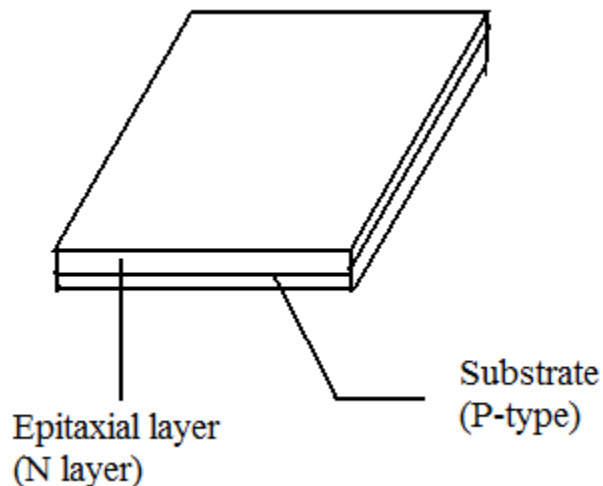
Substrate
(P-type)

The higher collector resistance is reduced by a process called buried layer as shown in figure. In this arrangement, a heavily doped 'N' region is sandwiched between the N-type epitaxial layer and P – type substrate. This buried N^+ layer provides a low resistance path in the active collector

region to the collector contact C. In effect, the buried layer provides a low resistance shunt path for the flow of current.

For fabricating an NPN transistor, we begin with a P-type silicon substrate having a resistivity of typically 1Ω-cm, corresponding to an acceptor ion concentration of $1.4 * 10^{15}$ atoms/cm^3. An oxide mask with the necessary pattern for buried layer diffusion is prepared. This is followed by masking and etching the oxide in the buried layer mask.

The N-type buried layer is now diffused into the substrate. A slow-diffusing material such as arsenic or antimony us used, so that the buried layer will stay-put during subsequent diffusions. The junction depth is typically a few microns, with sheet resistivity of around 20Ω per square.

Then, an epitaxial layer of lightly doped N-silicon is grown on the P-type substrate by placing the wafer in the furnace at 1200^0 C and introducing a gas containing phosphorus (donor impurity). The resulting structure is shown in figure.

The subsequent diffusions are done in this epitaxial layer. All active and passive components are formed on the thin N-layer epitaxial layer grown over the P-type substrate. Obtaining an epitaxial layer of the proper thickness and doping with high crystal quality is perhaps the most formidable challenge in bipolar device processing.

2. Oxidation:
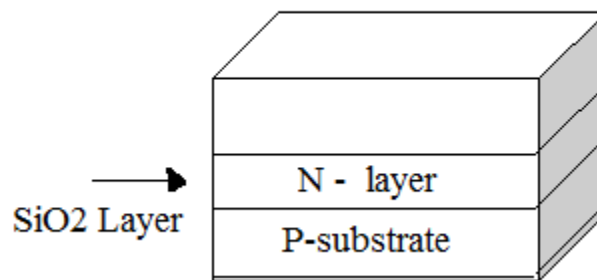
As shown in figure, a thin layer of silicon dioxide (SiO$_2$) is grown over the N-type layer by exposing the silicon wafer to an oxygen atmosphere at about 1000^0 C.

3. Photolithography:

(a) ... Photoresist film 5000-10000Å SiO₂ Silicon wafer
(b) Ultraviolet radiation Photo mask SiO₂ Silicon wafer Photo resist
(c) Polymerised photoresist SiO₂ Silicon wafer
(d) Photoresist SiO₂ Silicon wafer
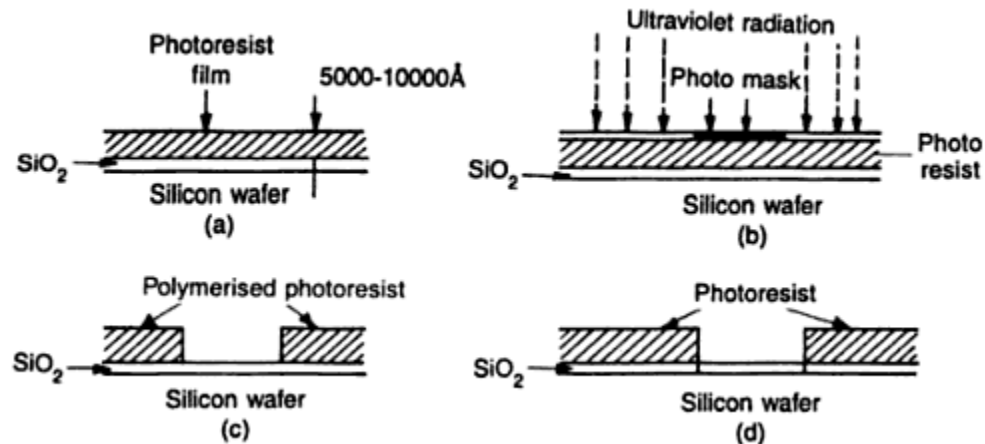
The prime use of photolithography in IC manufacturing is to selectively etch or remove the SiO₂ layer. As shown in figure, the surface of the oxide is first covered with a thin uniform layer of photosensitive emulsion (Photo resist). The mask, a black and white negative of the requied pattern, is placed over the structure. When exposed to ultraviolet light, the photo resist under the transparent region of the mask becomes poly-merized. The mask is then removed and the wafer is treated chemically that removes the unexposed portions of the photoresist film. The polymerized region is cured so that it becomes resistant to corrosion. Then the chip is dipped in an etching solution of hydrofluoric acid which removes the oxide layer not protected by the polymerized photoresist. This creates openings in the SiO₂ layer through which P-type or N-type impurities can be diffused using the isolation diffusion process as shown in figure. After diffusion of impurities, the polymerized photoresist is removed with sulphuric acid and by a mechanical abrasion process.

4. Isolation Diffusion:

The integrated circuit contains many devices. Since a number of devices are to be fabricated on the same IC chip, it becomes necessary to provide good isolation between various components and their interconnections.

The most important techniques for isolation are:

1. PN junction Isolation
2. Dielectric Isolation

In PN junction isolation technique, the P⁺ type impurities are selectively diffused into the N-type epitaxial layer so that it touches the P-type substrate at the bottom. This method generated N-type isolation regions surrounded by P-type moats. If the P-substrate is held at the most negative potential, the diodes will become reverse-biased, thus providing isolation between these islands.

The individual components are fabricated inside these islands. This method is very economical, and is the most commonly used isolation method for general purpose integrated circuits.

In dielectric isolation method, a layer of solid dielectric such as silicon dioxide or ruby surrounds each component and this dielectric provides isolation. The isolation is both physical and electrical. This method is very expensive due to additional processing steps needed and this is mostly used for fabricating IC's required for special application in military and aerospace.

The PN junction isolation diffusion method is shown in figure. The process take place in a furnace using boron source. The diffusion depth must be atleast equal to the epitaxial thickness in order to obtain complete isolation. Poor isolation results in device failures as all transistors might get shorted together. The N-type island shown in figure forms the collector region of the NPN transistor. The heavily doped P-type regions marked P^+ are the isolation regions for the active and passive components that will be formed in the various N-type islands of the epitaxial layer.

5 Base diffusion:

Formation of the base is a critical step in the construction of a bipolar transistor. The base must be aligned, so that, during diffusion, it does not come into contact with either the isolation region or the buried layer. Frequently, the base diffusion step is also used in parallel to fabricate diffused resistors for the circuit. The value of these resistors depends on the diffusion conditions and the width of the opening made during etching. The base width influences the transistor parameters very strongly. Therefore, the base junction depth and resistivity must be tightly controlled. The base sheet resistivity should be fairly high (200- 500Ω per square) so that the base does not inject carriers into the emitter. For NPN transistor, the base is diffused in a furnace using a boron source. The diffusion process is done in two steps, pre deposition of dopants at 900^0 C and driving them in at about 1200^0 C. The drive-in is done in an oxidizing ambience, so that oxide is grown over the base region for subsequent fabrication steps. Figure shows that P-type base region of the transistor diffused in the N-type island (collector region) using photolithography and isolation diffusion processes.

6. Emitter Diffusion:

Emitter Diffusion is the final step in the fabrication of the transistor. The emitter opening must lie wholly within the base. Emitter masking not only opens windows for the emitter, but also for the contact point, which provides a low resistivity ohmic contact path for the emitter terminal.

The emitter diffusion is normally a heavy N-type diffusion, producing low-resistivity layer that can inject charge easily into the base. A Phosphorus source is commonly used so that the diffusion time id shortened and the previous layers do not diffuse further. The emitter is diffused into the base, so that the emitter junction depth very closely approaches the base junction depth. The active base is then a P-region between these two junctions which can be made very narrow by adjusting the emitter diffusion time. Various diffusion and drive in cycles can be used to fabricate the emitter. The Resistivity of the emitter is usually not too critical.

The N-type emitter region of the transistor diffused into the P-type base region is shown below. However, this is not needed to fabricate a resistor where the resistivity of the P-type base region itself will serve the purpose. In this way, an NPN transistor and a resistor are fabricated simultaneously.

7. Contact Mask:

After the fabrication of emitter, windows are etched into the N-type regions where contacts are to be made for collector and emitter terminals. Heavily concentrated phosphorus N^+ dopant is diffused into these regions simultaneously.

The reasons for the use of heavy N^+ diffusion is explained as follows: Aluminium, being a good conductor used for interconnection, is a P-type of impurity when used with silicon. Therefore, it can produce an unwanted diode or rectifying contact with the lightly doped N-material. Introducing a high concentration of N^+ dopant caused the Si lattice at the surface semi-metallic. Thus the N^+ layer makes a very good ohmic contact with the Aluminium layer. This is done by the oxidation, photolithography and isolation diffusion processes.

8. Metallization:

The IC chip is now complete with the active and passive devices, and the metal leads are to be formed for making connections with the terminals of the devices. Aluminium is deposited over the entire wafer by vacuum deposition. The thickness for single layer metal is 1μ m. Metallization is carried out by evaporating aluminium over the entire surface and then selectively etching away aluminium to leave behind the desired interconnection and bonding pads as shown in figure.

Metallization is done for making interconnection between the various components fabricated in an IC and providing bonding pads around the circumference of the IC chip for later connection of wires

9. Passivation/ Assembly and Packaging:

Metallization is followed by passivation, in which an insulating and protective layer is deposited over the whole device. This protects it against mechanical and chemical damage during subsequent processing steps. Doped or undoped silicon oxide or silicon nitride, or some combination of them, are usually chosen for passivation of layers. The layer is deposited by chemical vapour deposition (CVD) technique at a temperature low enough not to harm the metallization.

Transistor Fabrication:

PNP Transistor:

The integrated PNP transistors are fabricated in one of the following three structures.

1. Substrate or Vertical PNP
2. Lateral or horizontal PNP and
3. Triple diffused PNP

Substrate or Vertical PNP:

The P-substrate of the IC is used as the collector, the N-epitaxial layer is used as the base and the next P-diffusion is used as the emitter region of the PNP transistor. The structure of a vertical monolithic PNP transistor Q_1 is shown in figure. The base region of an NPN transistor structure is formed in parallel with the emitter region of the PNP transistor.

The method of fabrication has the disadvantage of having its collector held at a fixed negative potential. This is due to the fact that the P-substrate of the IC is always held at a negative potential normally for providing good isolation between the circuit components and the substrate.

Triple diffused PNP:

This type of PNP transistor is formed by including an additional diffusion process over the standard NPN transistor processing steps. This is called a triple diffusion process, because it involves an additional diffusion of P-region in the second N-diffusion region of a NPN transistor. The structure of the triple diffused monolithic PNP transistor Q_2 is also shown in the below figure.

This has the limitations of requiring additional fabrication steps and sophisticated fabrication assemblies.

Lateral or Horizontal PNP:

This is the most commonly used form of integrated PNP transistor fabrication method. This has the advantage that it can be fabricated simultaneously with the processing steps of an NPN transistor and therefore it requires as the base of the PNP transistor. During the P-type base diffusion process of NPN transistor, two parallel P-regions are formed which make the emitter and collector regions of the horizontal PNP transistor.
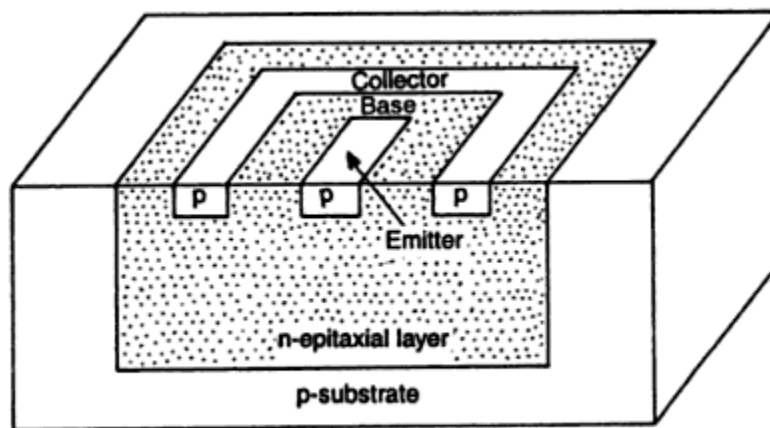
Fig. 1.17 A *pnp* lateral transistor

Comparison of monolithic NPN and PNP transistor:

Normally, the NPN transistor is preferred in monolithic circuits due to the following reasons:

1. The vertical PNP transistor must have his collector held at a fixed negative voltage.

2. The lateral PNP transistor has very wide base region and has the limitation due to the lateral diffusion of P-type impurities into the N-type base region. This makes the photographic mask making, alignment and etching processes very difficult. This reduces the current gain of lateral PNP transistors as low as 1.5 to 30 as against 50 to 300 for a monolithic NPN transistor.

3. The collector region is formed prior to the formation of base and emitter diffusion. During the later diffusion steps, the collector impurities diffuse on either side of the defined collector junction. Since the N-type impurities have smaller diffusion constant compared to P-type impurities the N-

type collector performs better than the P-type collector. This makes the NPN transistor preferable for monolithic fabrication due to the easier process control.

Transistor with multiple emitters: The applications such as transistor- transistor logic (TTL) require multiple emitters. The below figure shows the circuit sectional view of three N-emitter regions diffused in three places inside the P-type base. This arrangement saves the chip area and enhances the component density of the IC.
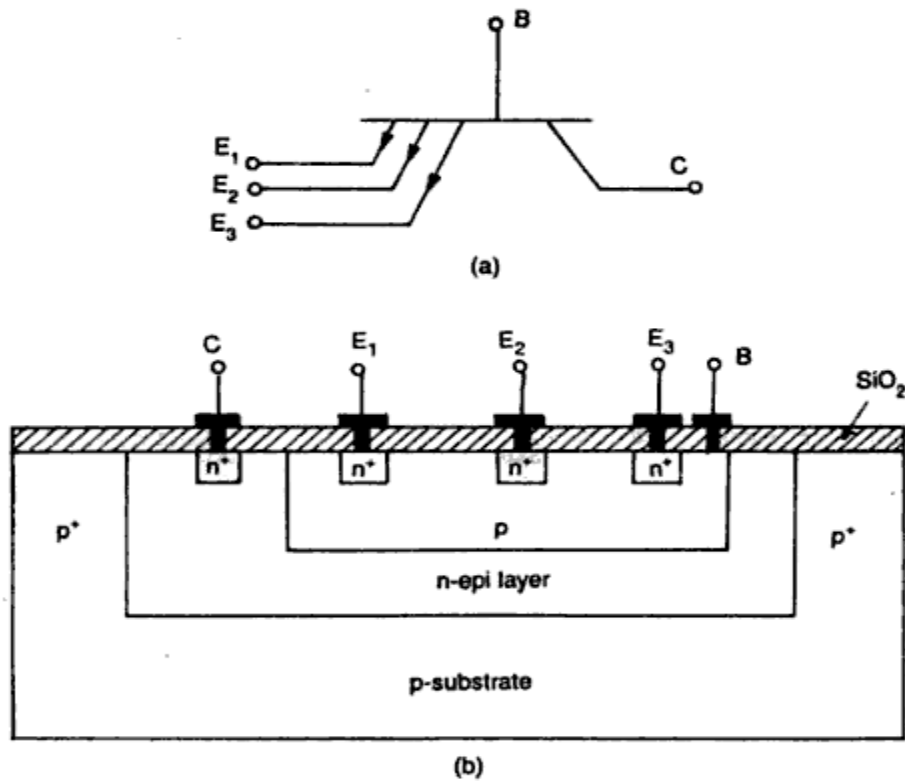
Fig. 1.18 (a) Multi-emitter transistor, (b) Cross-sectional view of a multi-emitter transistor

Schottky Barrier Diode:
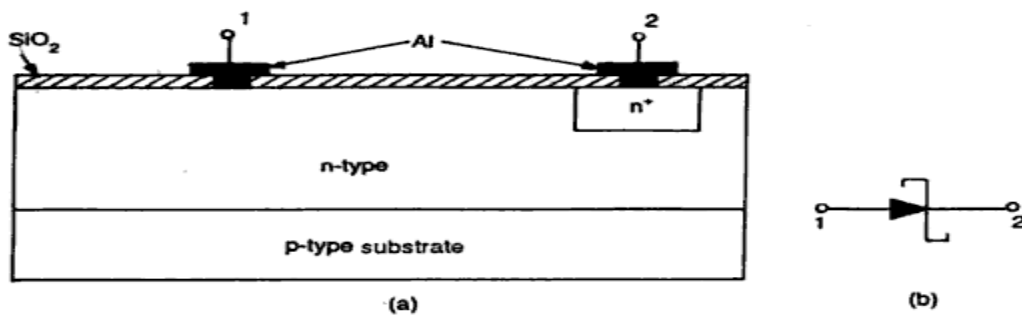
Fig. 1.21 (a) A Schottky diode, (b) Symbol for metal semiconductor diode

The metal contacts are required to be ohmic and no PN junctions to be formed between the metal and silicon layers. The N^+ diffusion region serves the purpose of generating ohmic contacts. On the other hand, if aluminium is deposited directly on the N-type silicon, then a metal semiconductor diode can be said to be formed. Such a metal semiconductor diode junction exhibits the same type of V-I Characteristics as that of an ordinary PN junction.

The cross sectional view and symbol of a Schottky barrier diode as shown in figure. Contact 1 shown in figure is a Schottky barrier and the contact 2 is an ohmic contact. The contact potential between the semiconductor and the metal generated a barrier for the flow of conducting electrons from semiconductor to metal. When the junction is forward biased this barrier is lowered and the electron flow is allowed from semiconductor to metal, where the electrons are in large quantities.

The minority carriers carry the conduction current in the Schottky diode whereas in the PN junction diode, minority carriers carry the conduction current and it incurs an appreciable time delay from ON state to OFF state. This is due to the fact that the minority carriers stored in the junction have to be totally removed. This characteristic puts the Schottky barrier diode at an advantage since it exhibits negligible time to flow the electron from N-type silicon into aluminum almost right at the contact surface, where they mix with the free electrons. The other advantage of this diode is that it has less forward voltage (approximately 0.4V). Thus it can be used for clamping and detection in high frequency applications and microwave integrated circuits.

Schottky transistor:
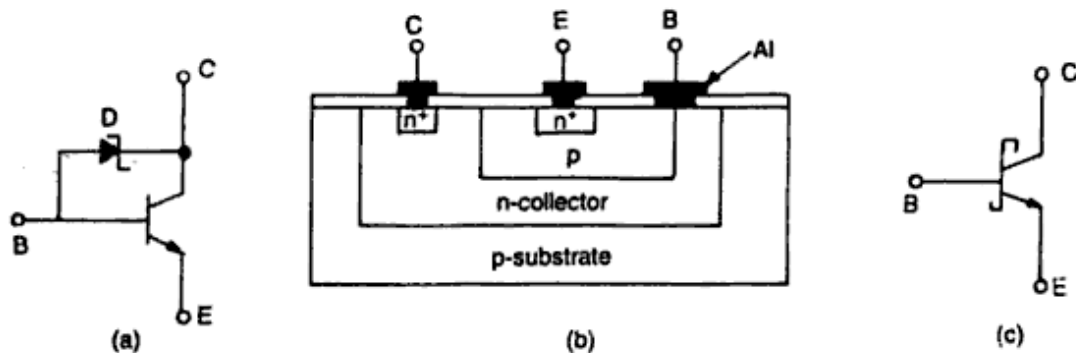
Fig. 1.19 (a) A transistor with a Schottky-barrier diode clamped between base and collector to prevent saturation, (b) Cross-section of a Schottky-barrier transistor, (c) Symbolic representation

The cross-sectional view of a transistor employing a Schottky barrier diode clamped between its base and collector regions is shown in figure. The equivalent circuit and the symbolic representation of the Schottky transistor are shown in figure. The Schottky diode is formed by allowing aluminium metallization for the base lead which makes contact with the N-type collector region also as shown in figure.

When the base current is increased to saturate the transistor, the voltage at the collector C reduces and this makes the diode Ds conduct. The base to collector voltage reduces to 0.4V, which is less the cut-in-voltage of a silicon base-collector junction. Therefore, the transistor does not get saturated.

Monolithic diodes:

The diode used in integrated circuits are made using transistor structures in one of the five possible connections. The three most popular structures are shown in figure. The diode is obtained from a transistor structure using one of the following structures.

1. The emitter-base diode, with collector short circuited to the base.
2. The emitter-base diode with the collector open and
3. The collector –base diode, with the emitter open-circuited.

The choice of the diode structure depends on the performance and application desired. Collector-base diodes have higher collector-base arrays breaking rating, and they are suitable for common-cathode diode arrays diffused within a single isolation island. The emitter-base diffusion is very popular for the fabrication of diodes, provided the reverse-voltage requirement of the circuit does not exceed the lower base-emitter breakdown voltage.

Characteristic	(a) $V_{CB} = 0$	(b) $V_{CE} = 0$	(c) $V_{EB} = 0$	(d) $I_C = 0$	(e) $I_E = 0$
Breakdown voltage in volts	7	7	55	7	55
Storage time, n sec	9	100	53	56	85
Forward voltage in volts	.85	.92	.94	.96	.95

(a)   (b)   (c)   (d)   (e)
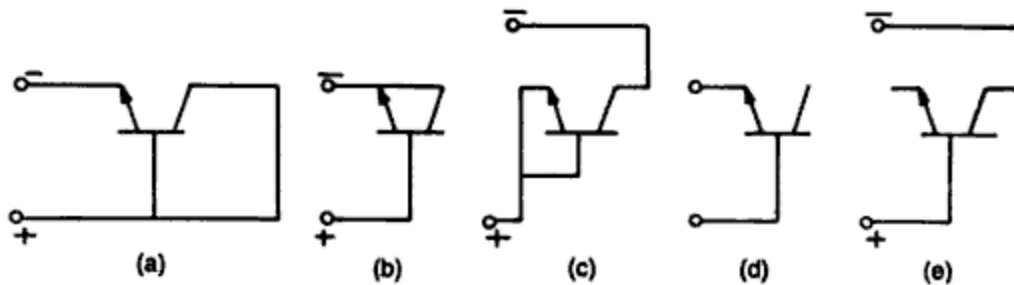
Integrated Resistors:

A resistor in a monolithic integrated circuit is obtained by utilizing the bulk resistivity of the diffused volume of semiconductor region. The commonly used methods for fabricating integrated resistors are 1. Diffused 2. epitaxial 3. Pinched and 4. Thin film techniques.

Diffused Resistor:

The diffused resistor is formed in any one of the isolated regions of epitaxial layer during base or emitter diffusion processes. This type of resistor fabrication is very economical as it runs in parallel to the bipolar transistor fabrication. The N-type emitter diffusion and P-type base diffusion are commonly used to realize the monolithic resistor.

The diffused resistor has a severe limitation in that, only small valued resistors can be fabricated. The surface geometry such as the length, width and the diffused impurity profile determine the resistance value. The commonly used parameter for defining this resistance is called the sheet resistance. It is defined as the resistance in ohms/square offered by the diffused area.

In the monolithic resistor, the resistance value is expressed by

$R = R_s \; 1/w$ where R= resistance offered (in ohms)

R_s = sheet resistance of the particular fabrication process involved (in ohms/square)

l = length of the diffused area and

w = width of the diffused area.

The sheet resistance of the base and emitter diffusion in 200Ω/Square and 2.2Ω/square respectively. For example, an emitter-diffused strip of 2mil wide and 20 mil long will offer a resistance of 22Ω. For higher values of resistance, the diffusion region can be formed in a zig-zag fashion resulting in larger effective length. The poly silicon layer can also be used for resistor realization.

Epitaxial Resistor:
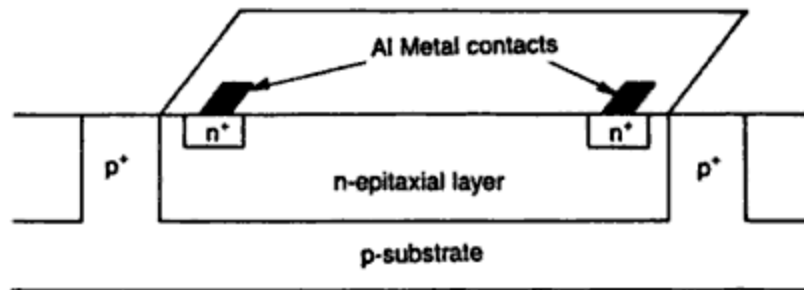
Fig. 1.23 (a) Epitaxial resistor

The N-epitaxial layer can be used for realizing large resistance values. The figure shows the cross-sectional view of the epitaxial resistor formed in the epitaxial layer between the two N^+ aluminium metal contacts.

Pinched resistor:
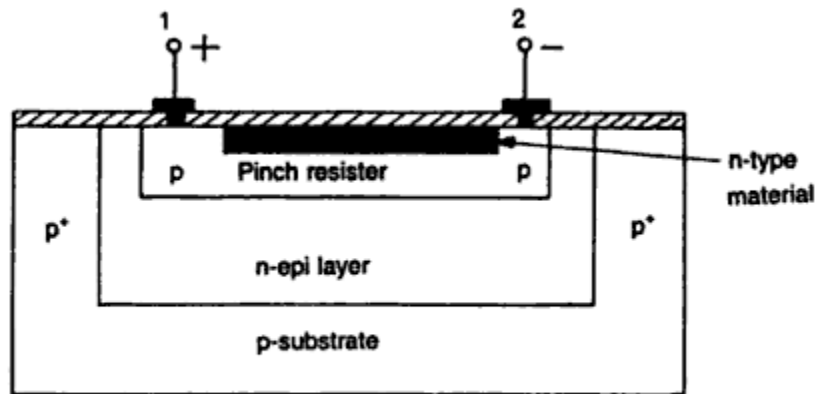
Fig. 1.23 (b) Cross-sectional view of a pinch resistor

The sheet resistance offered by the diffusion regions can be increased by narrowing down its cross-sectional area. This type of resistance is normally achieved in the base region. Figure shows a pinched base diffused resistor. It can offer resistance of the order of mega ohms in a comparatively smaller area. In the structure shown, no current can flow in the N-type material

since the diode realized at contact 2 is biased in reversed direction. Only very small reverse saturation current can flow in conduction path for the current has been reduced or pinched. Therefore, the resistance between the contact 1 and 2 increases as the width narrows down and hence it acts as a pinched resistor.

Thin film resistor:
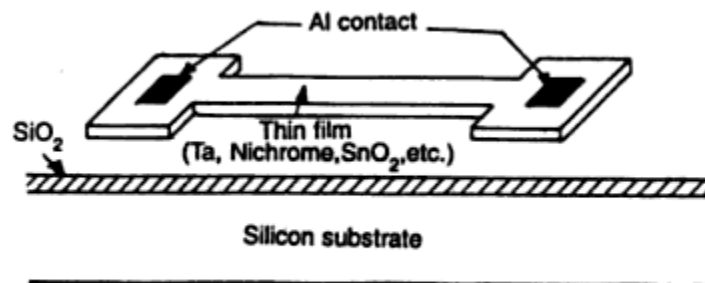
Fig. 1.23 (c) Cross-section of a thin film resistor

The thin film deposition technique can also be used for the fabrication of monolithic resistors. A very thin metallic film of thickness less than 1μm is deposited on the silicon dioxide layer by vapour deposition techniques. Normally, Nichrome (NiCr) is used for this process. Desired geometry is achieved using masked etching processes to obtain suitable value of resistors. Ohmic contacts are made using aluminium metallization as discussed in earlier sections.

The cross-sectional view of a thin film resistor as shown in figure. Sheet resistances of 40 to 400Ω/ square can be easily obtained in this method and thus 20kΩ to 50kΩ values are very practical.

The advantages of thin film resistors are as follows:
1. They have smaller parasitic components which makes their high frequency behaviour good.
2. The thin film resistor values can be very minutely controlled using laser trimming.
3. They have low temperature coefficient of resistance and this makes them more stable.

The thin film resistor can be obtained by the use of tantalum deposited over silicon dioxide layer. The main disadvantage of thin film resistor is that its fabrication requires additional processing steps.

Monolithic Capacitors:
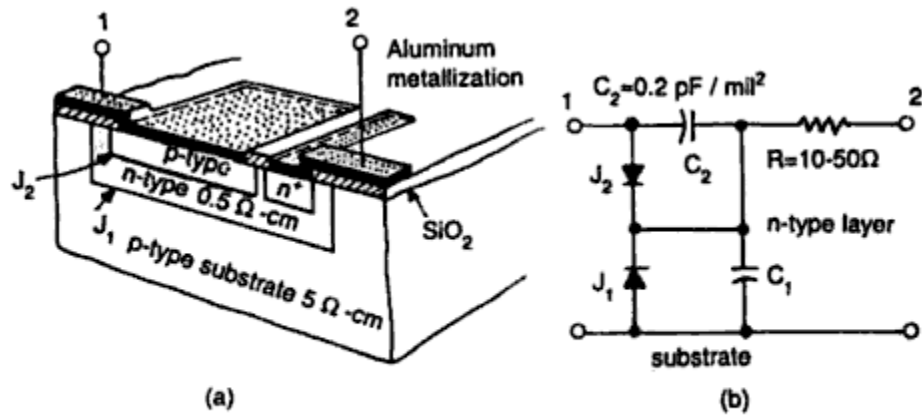
Fig. 1.24 (a) Junction-type IC capacitor, (b) Equivalent circuit

Monolithic capacitors are not frequently used in integrated circuits since they are limited in the range of values obtained and their performance. There are, however, two types available, the junction capacitor is a reverse biased PN junction formed by the collector-base or emitter-base diffusion of the transistor. The capacitance is proportional to the area of the junction and inversely proportional to the depletion thickness.

C   α A, where a is the area of the junction and

C   α T , where t is the thickness of the depletion layer.

The capacitance value thus obtainable can be around $1.2nF/mm^2$.

The thin film or metal oxide silicon capacitor uses a thin layer of silicon dioxide as the dielectric. One plate is the connecting metal and the other is a heavily doped layer of silicon, which is formed during the emitter diffusion. This capacitor has a lower leakage current and is non-directional, since emitter plate can be biased positively. The capacitance value of this method can be varied between 0.3 and $0.8nF/mm^2$.

Inductors:

No satisfactory integrated inductors exist. If high Q inductors with inductance of values larger than 5μH are required, they are usually supplied by a wound inductor which is connected externally to the chip. Therefore, the use of inductors is normally avoided when integrated circuits are used.

CURRENT MIRROR AND CURRENT SOURCES:

Constant current source(Current Mirror):

A constant current source makes use of the fact that for a transistor in the active mode of operation, the collector current is relatively independent of the collector voltage. In the basic circuit shown in fig 1
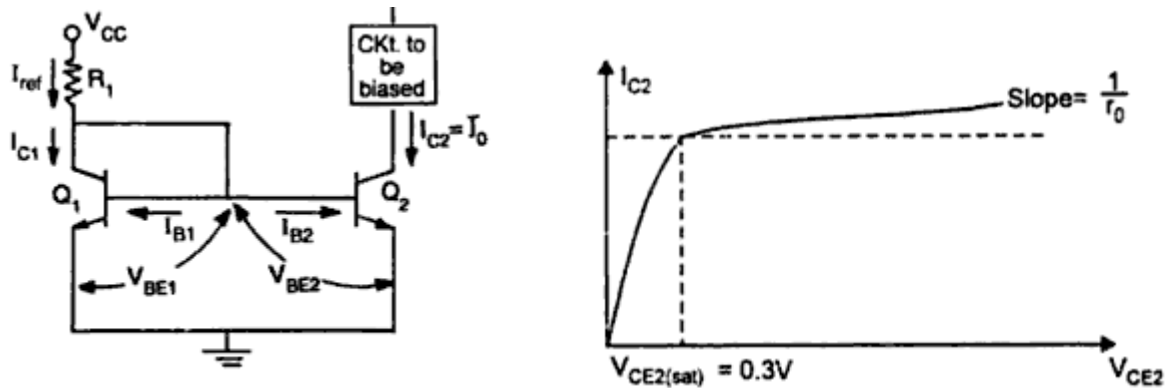
Transistors Q_1&Q_2 are matched as the circuit is fabricated using IC technology. Base and emitter of Q_1&Q_2 are tied together and thus have the same V_{BE}. .In addition, transistor Q1 is connected as a diode by shorting it s collector to base. The input current I_{ref} flows through the diode connected transistor Q1 and thus establishes a voltage across Q_1.

This voltage in turn appears between the base and emitter of Q_2 .Since Q_2 is identical to Q_1, the emitter current of Q_2 will be equal to emitter current of Q_1 which is approximately equal to I_{ref}

As long as Q2 is maintained in the active region ,its collector current $I_{C2=I_o}$ will be approximately equal to I_{ref}.

Since the output current Io is a reflection or mirror of the reference current I_{ref}, the circuit is often referred to as a current mirror.

Analysis:

The collector current I_{C1} and I_{C2} for the transistor Q1 and Q2 can be approximately expressed as

$$I_{C1} t\ \alpha_F\ I_{ES}\ e^{\frac{V_{BE1}}{V_T}} \text{---------(1)}$$

$$I_{C2} t\ \alpha_F\ I_{ES}\ e^{\frac{V_{BE2}}{V_T}} \text{-----------(2)}$$

From equation (1)&(2)

$$\frac{I_{C2}}{I_{C1}} = e^{\frac{V_{BE2}-V_{BE1}}{V_T}} \quad \text{-----------------(3)}$$

Since $V_{BE1}=V_{BE2}$ we obtain

$I_{C2}=I_{C1}=I_C=I_O$

Also since both the transistors are identical , $\beta_1 = \beta_2 = \beta$

KCL at the collector of Q_1 gives

$I_{ref}= I_{C1}+I_{B1}+I_{B2}$

$$=I_{C1} + \frac{I_{C1}}{\beta_1} + \frac{I_{C2}}{\beta_2} = I_C \left[1 + \frac{2}{\beta} \right] \quad \text{----------(4)}$$

solving Eq (4).

I_C may be expressed as

$$I_C = \frac{\beta}{\beta + 2} I_{ref} \quad \text{-----------(5)}$$

Where I_{ref} from fig   can be seen to be

$$I_{ref} = V_{CC} \frac{V_{BE}}{R_1} \approx \frac{V_{CC}}{R_1} \quad \text{(as } V_{BE}=0.7\text{V is small)}$$

From Eq.5   for $\beta \gg 1$, $\frac{\beta}{\beta + 2}$ is almost unity and the output current I_0 is equal to the reference current, I_{ref} which for a given R_1 is constant. Typically I_o varies by about 3% for $50 \le \beta \le 200$.

It is possible to obtain current transfer ratio other than unity simple by controlling the area of the emitter-base junction (EBJ) of the transistor Q_2. For example, if the area of EBJ of Q_2 is 4 times that of Q1,then

$I_O=4\, I_{ref}$

The output resistance of the current source is the output resistance,r_0 of Q2,

$$R_0 = r_{02} = \frac{V_A}{I_O} \approx \frac{V_A}{I_{ref}} \quad \text{[}V_A \text{ is the Early voltage]}$$

The circuit however operates as a constant current source as long as Q_2 remains in the active region.

Widlar current source:

Widlar current source which is particularly suitable for low value of currents. The circuit differs from the basic current mirror only in the resistance R_E that is included in the emitter lead of Q_2.

It can be seen that due to R_E the base-emitter voltage V_{BE2} is les than V_{BE1} and consequently current Io is smaller than I_{C1}
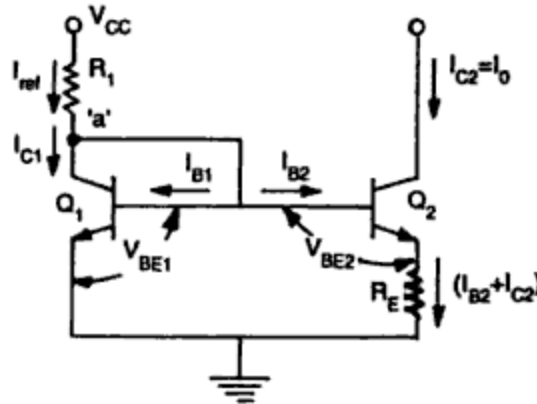
The ratio of collector currents I_{C1} & I_{C2} using

$$\frac{I_{C2}}{I_{C1}} = e^{\frac{V_{BE2}-V_{BE1}}{V_T}} \quad \text{-----------(1)}$$

Taking natural logarithm of both sides, we get

$$V_{BE1} - V_{BE2} = V_T \ln\left[\frac{I_{C1}}{I_{C2}}\right] \quad \text{-------(2)}$$

Writing KVL for the emitter base loop

$$V_{BE1} = V_{BE2} + (I_{B2} + I_{C2})R_E \quad \text{----------------(3)}$$

or $\quad V_{BE1} - V_{BE2} = (1/\beta + 1)I_{C2}R_E \quad \text{-----------(4)}$

From eqn (2)&(4) we obtain

$$\left[\frac{1}{\beta} + 1\right] I_{c2} R_E = V_T \ln\frac{I_{C1}}{I_{C2}} \quad \text{--------------(5)}$$

Or

$$R_E = \frac{V_T}{\left(1 + \frac{1}{\beta}\right)I_{C2}} \ln\frac{I_{C1}}{I_{C2}} \quad \text{--------------(6)}$$

A relation between I_{C1} and the reference current I_{ref} is obtained by writing KCL at the collector point of Q_1

$$I_{ref} = I_{C1} + I_{B1} + I_{B2}$$

$$= I_{C1}\left[1 + \frac{g_m}{\beta} + \frac{I_{C2}}{\beta}\right] \text{-----------------(7)}$$

(Assuming $\beta_2 = \beta_1 = \beta$ for identical transistors)

In the Widlar current source $I_{C2} \ll I_{C1}$, therefore the term $\frac{I_{C2}}{\beta}$ may be neglected in (7)

Thus $I_{ref} \doteq I_{C1}\left[1 + \frac{g_m}{\beta}\right]$

$I_{C1} = \frac{\beta}{\beta + 1} I_{ref}$

Where $I_{ref} = \frac{V_{CC} - V_{BE}}{R_1}$

For $\beta \gg 1$ $I_{C1} \doteq I_{ref}$

Wilson current source:

The Wilson current source shown in fig
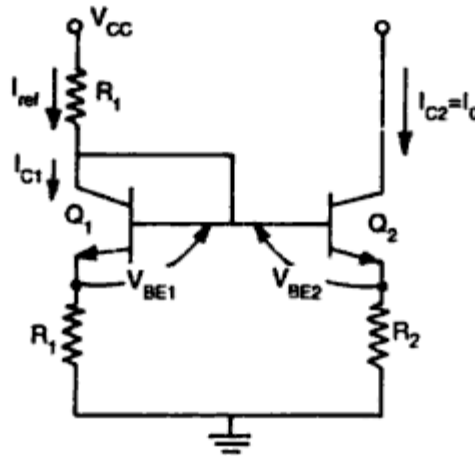
> A current mirror with magnification $(I_{c2}/I_{c1} \cong R_1/R_2)$

It provides an output current I_o, which is very nearly equal to V_{ref} and also exhibits a very high output resistance.

Analysis:

Since $V_{BE1} = V_{BE2}$

$I_{C1} = I_{C2}$ and $I_{B1} = I_{B2} = I_B$

At node 'b'

$I_{E3} = 2I_B + I_{C2} = \left[\frac{2}{\beta} + 1\right]I_{C2}$ -----------(1)

I_{E3} is equal to

$I_{E3} = I_{C3} + I_{B3} = I_{C3}\left[1 + \frac{g_m}{\beta}\right]$ -----------(2)

From Eqn (1)&(2) we obtain

$$I_{C3}\left(1+\frac{2}{\beta}\right)=I_{C2}\left(1+\frac{2}{\beta}\right)$$

$$I_{C3}=I_o=\frac{\beta+2}{\beta+1}I_{C2}$$

Since $I_{C1}=I_{C2}$

$$I_o=\frac{\beta+2}{\beta+1}I_{C1}$$

At node 'a'

$$I_{ref}=I_{C1}+I_{B3}=\frac{\beta+1}{\beta+2}I_o+\frac{I_o}{\beta}=\frac{\beta^2+2\beta+2}{\beta^2+2\beta}I_o$$

or $$I_o=\frac{\beta^2+2\beta}{\beta^2+2\beta+2}I_{ref}$$

where $$I_{ref}=\frac{V_{CC}-2V_{BE}}{R_1}$$

The difference $I_O-I_{ref}=\frac{2}{\beta^2+2\beta+2}I_{ref}$ is extremely small error for modest values of β

The output resistance of a Wilson current mirror is substantially greater $\approx\beta\frac{r_o}{2}$ than simple current mirror or Widlar current mirror.

Current sources as Active loads:

The current source can be used as an active load in both analog and digital IC's. The active load realized using current source in place of the passive load (i.e. a resistor) in the collector arm of differential amplifier makes it possible to achieve high voltage gain without requiring large power supply voltage. The active load so achieved is basically r_0 of a PNP transistor.

Voltage Sources:

A voltage source is a circuit that produces an output voltage V_0, which is independent of the load driven by the voltage source, or the output current supplied to the load. The voltage source is the circuit dual of the constant current source.

A number of IC applications require a voltage reference point with very low ac impedance and a stable dc voltage that is not affected by power supply and temperature variations. There are two methods which can be used to produce a voltage source, namely,

1. using the impedance transforming properties of the transistor, which in turn determines the current gain of the transistor and

2. using an amplifier with negative feedback.

Voltage source circuit using Impedance transformation:

The voltage source circuit using the impedance transforming property of the transistor is shown in figure. The source voltage V_s drives the base of the transistor through a series resistance R_S and the output is taken across the emitter. From the circuit, the output ac resistance looking into emitter is given by

$$\frac{dV_0}{dI_0} = R_0 = \frac{R_s}{\beta + 1} + r_{eb}$$

with values as high as 100 for β, R_S is transformed to a value of $\frac{R_s}{\beta+1}$
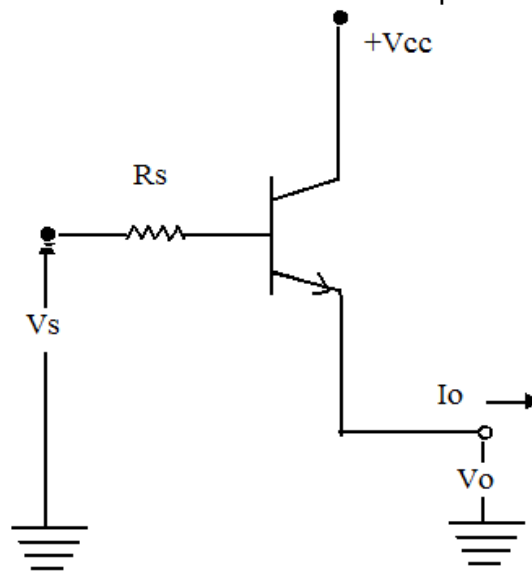
It is to be noted that, eqn is applicable only for small changes in the output current. The load regulation parameter indicates the changes in V_0 resulting from large changes in output current I_0, Reduction in V_0 occurs as I_0 goes from no-load current to full-load current and this factor determines the output impedance of the voltage sources.

Emitter – follower or Common Collector Type Voltage source:

The figure shows an emitter follower or common collector type voltage source. This voltage source is suitable for the differential gain stage used in op-amps. This circuit has the advantages of

1. Producing low ac impedance and
2. resulting in effective decoupling of adjacent gain stages.

The low output impedance of the common-collector stage simulates a low impedance voltage source with an output voltage level of V_0 represented by

$$V_0 = V_{cc} \frac{R_2}{R_1 + R_2}$$

The diode D_1 is used for offsetting the effect of dc value V_{BE}, across the E-B junction of the transistor, and for compensating the temperature dependence of V_{BE} drop of Q_1. The load Z_L shown in dotted line represents the circuit biased by the current through Q_1.

The impedance R_0 looking into the emitter of Q_1 derived from the hybrid π model is given by

$$R_0 = \frac{V_T}{I_1} + \frac{R_1 R_2}{\beta \ R_1 + R_2}$$
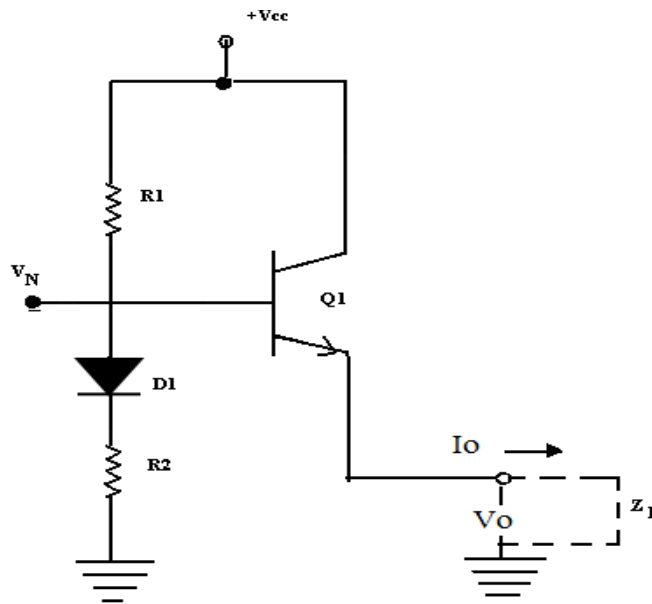
Voltage Source suing Temperature compensated Avalanche Diode:

The voltage source using common collector stage has the limitations of its vulnerability for changes in bias voltage V_N and the output voltage V_0 with respect to changes in supply voltage Vcc. This is overcome in the voltage source circuit using the breakdown voltage of the base-emitter junction shown below.

The emitter – follower stage of common – collector is eliminated in this circuit, since the impedance seen looking into the bias terminal N is very low. The current source I_1 is normally simulated by a resistor connected between Vcc and node n. Then, the output voltage level V_0 at node N is given by

$V_0 = V_B + V_{BE}$

Where V_B is the breakdown voltage of diode D_B and V_{BE} is the diode drop across D_1. The breakdown diode D_B is normally realized using the base-emitter junction of the transistor. The diode D_1 provides partial compensation for the positive temperature coefficient effect of V_B. In a monolithic IC structure, D_B and D_1 can be conveniently realized as a single transistor with two individual emitters as shown in figure.
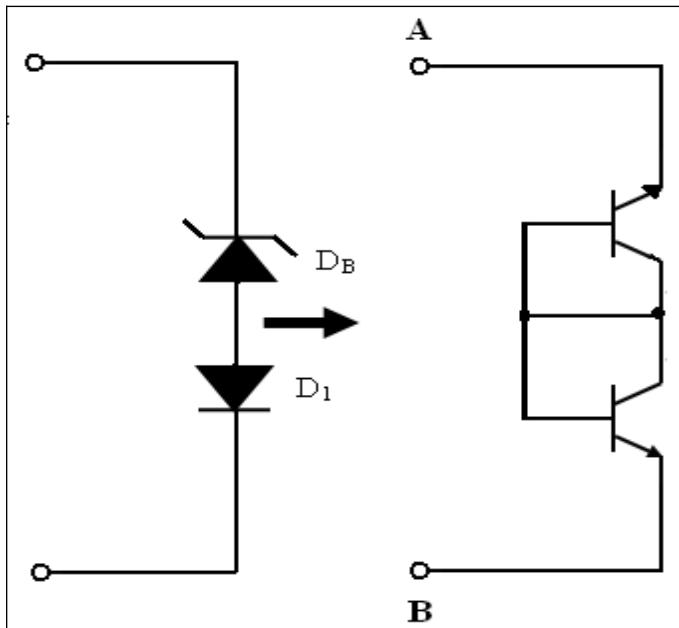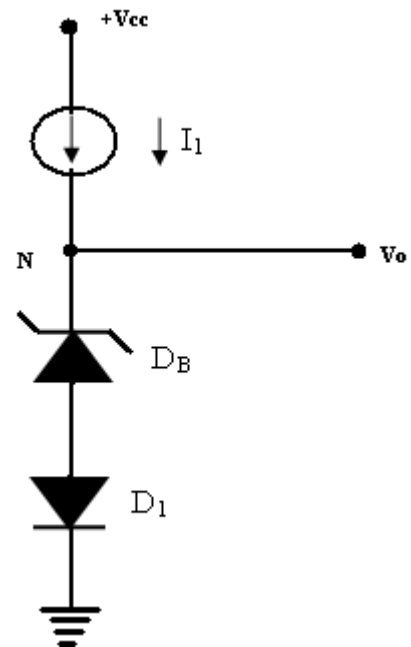
| **Temperature Compensated avalanche diode** | **Voltage source using breakdown voltage of the base- emitter junction** |

The structure consists of composite connection of two transistors which are diode-connected back-to back. Since the transistors have their base to collector terminals common, they can be designed as a single transistor with two emitters.

The output resistance R_0 looking into the output terminal in figure is given by

$$R_0 = R_B + \frac{V_T}{I_1}$$ Where R_B and V_T/I_1 are the ac resistances of the base –emitter resistance of diode D_B and D_1 respectively. Typically R_B is in the range of 40Ω to 100Ω, and V_0 in the range of 6.5V to 9V.

Voltage Source using V_{BE} as a reference:

The output stage of op-amp requires stabilized bias voltage source, which can be obtained using a forward-biased diode connected transistor.

The forward voltage drop for such a connection is approximately 0.7V, and it changes slightly with current. When a voltage level greater than 0.7V, is needed, several diodes can be connected in series, which can offer integral multiples of 0.7V. Alternatively, the figure shows a multiplier circuit, which can offer voltage levels, that need not be integral multiplied of 0.7V. The drop across R_2 equals V_{BE} drop of Q_1. Considering negligible base current for Q_1, current through R_2 is the same as that flowing through R_1. Therefore, the output voltage V_0 can be expressed as

$$V_0 = I_2\, R_1 + R_2 = \frac{V_{BE}}{R_2}\, R_1 + R_2 = V_{BE}\left[\frac{R_1}{R_2} + 1\right]$$
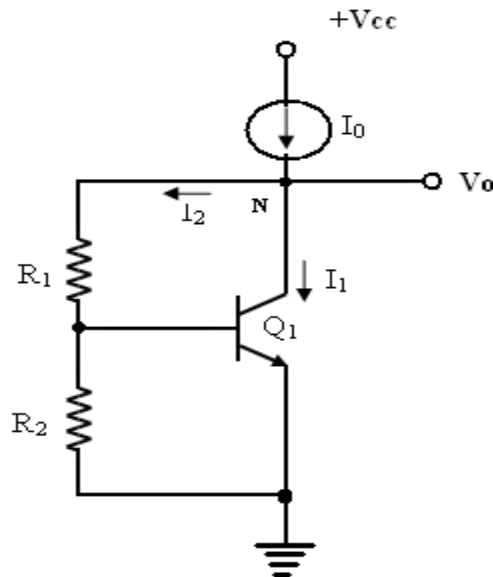
V_{BE} multiplier Circuit

Hence, the voltage V_0 can be any multiple of V_{BE} by properly selecting the resistors R_1 and R_2. Due to the shunt feedback provided by R_1, the transistor current I_1 automatically adjusts itself, towards maintaining I_2 and V_0 relatively independent of the changes in supply voltage.

The ac output resistance of the circuit R_0 is given by,

$$R_0 = \frac{dV_t}{dI_o} \cdot \frac{R_{out} \, R_{out}}{1 + g_m R_2}$$

when $g_m R_2 \gg 1$, *we have* $R_0 = \frac{R_{out} R_{out}}{R_2} A \frac{1}{g_m}$

Using this eqn we have,

$$\frac{V_{out}}{V_{BE}} = \frac{R_{out} R_{out}}{R_2}$$

Therefore,

$$R_0 = \frac{V_{out}}{V_{BE}} \frac{1}{g_m} = \frac{V_{out} V_t}{V_{BE} I_C}$$

Voltage References:

The circuit that is primarily designed for providing a constant voltage independent of changes in temperature is called a voltage reference. The most important characteristic of a voltage reference is the temperature coefficient of the output reference voltage TC_R, and it is expressed as

$$TC_R = \frac{dV_{ref}}{dT}$$

The desirable properties of a voltage reference are:

1. Reference voltage must be independent of any temperature change.
2. Reference voltage must have good power supply rejection which is as independent of the supply voltage as possible and
3. output voltage must be as independent of the loading of output current as possible, or in other words, the circuit should have low output impedance.

The voltage reference circuit is used to bias the voltage source circuit, and the combination can be called as the voltage regulator. The basic design strategy is producing a zero TC_R at a given temperature, and thereby achieving good thermal ability. Temperature stability of the order of 100ppm/^{0}C is typically expected.

Voltage Reference circuit using temperature compensation scheme:

      The voltage reference circuit using basic temperature compensation scheme is shown below. This design utilizes the close thermal coupling achievable among the monolithic components and this technique compensates the known thermal drifts by introducing an opposing and compensating drift source of equal magnitude.
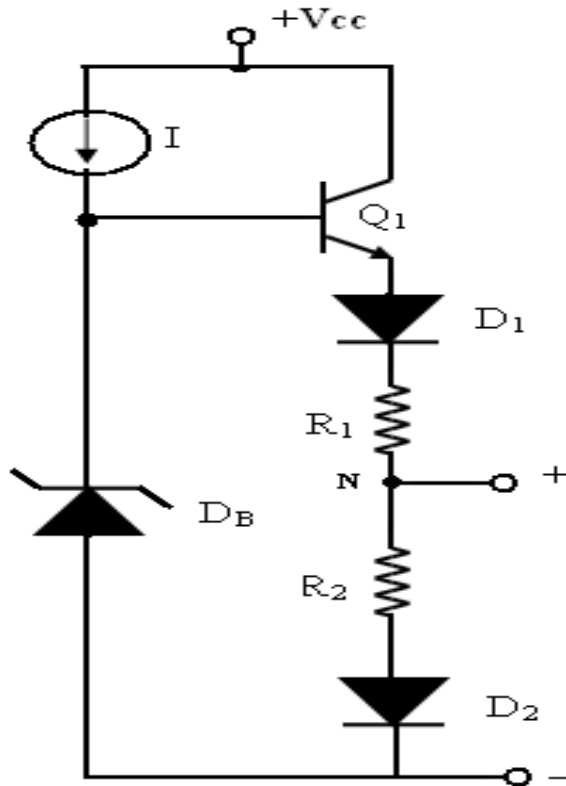
Voltage Reference circuit using temperature compensation Scheme

A constant current I is supplied to the avalanche diode D_B and it provides a bias voltage of V_B to the base of Q_1. The temperature dependence of the V_{BE} drop across Q_1 and those across D_1 and D_2 results in respective temperature coefficients. Hence, with the use of resistors R_1 and R_2 with tapping across them at point N compensates for the temperature drifts in the base-emitter loop of Q_1. This results in generating a voltage reference V_R with normally zero temperature coefficient.

Applying KCL at node N, we get

$$\frac{V_B @V_{BE\ Q_1} @V_{BE\ D_1} @V_R}{R_1} = \frac{V_R @V_{BE\ D_2}}{R_2}$$

Assuming matched transistors,

$$V_{BE\ Q_1} = V_{BE\ D_1} = V_{BE\ D_2} = V_{BE}$$

Then Eq can be expressed as

$$\frac{V_B @2V_{BE} @V_R}{R_1} = \frac{V_R @V_{BE}}{R_2}$$

Therefore, the voltage level V_R is given by

$$V_R = \frac{R_2 V_B + V_{BE} R_1 @2R_2}{R_1 + R_2}$$

Differentiating V_B and V_{BE} in eq(2) partially with respect to temperature, we get

$$0 = \frac{R_2}{R_1 + R_2} \frac{\partial V}{\partial T} + \frac{R_1 + 2R_2}{R_1 + R_2} \frac{\partial V}{\partial T}$$

That is,

$$\frac{2R_1 + R_2}{R_2} = \frac{\frac{\partial V}{\partial T}}{\frac{\partial V}{\partial T}} \qquad @@@\ 3^a$$

Therefore, it can be inferred that eq(3) is to be satisfied for obtaining zero temperature coefficient.

Voltage Reference circuit using Avalanche Diode Reference:

A voltage reference can be implemented using the brerakdown phenomenon condition of a heavily doped PN junction. The zener breakdown is the main mechanism for junctions, which breakdown at a voltage of 5V or less. For integrated transistors , the base-emitter breakdown voltage falls in the range of 6 to 8V. Therefore, the breakdown in the junctions of the integrated transistor is primarily due to avalanche multiplication. The avalanche breakdown voltage V_B of a transistor incurs a positive temperature coefficient, typically in the range of $2mV/^0C$ to $5mV/^0C$.

Figure depicts a current reference circuit using avalanche diode reference. The base bias for transistor Q_1 is provided through register R_1 and it also provides the dc current needed to bias D_B, D_1 and D_2 .

The voltage at the base of Q_1 is equal to the zener voltage V_B added with two diode drops due to D_1 and D_2 . The voltage across R_2 is equal to the voltage at the base of Q_1 less the sum of the base – emitter voltages of Q_1 and Q_2 .
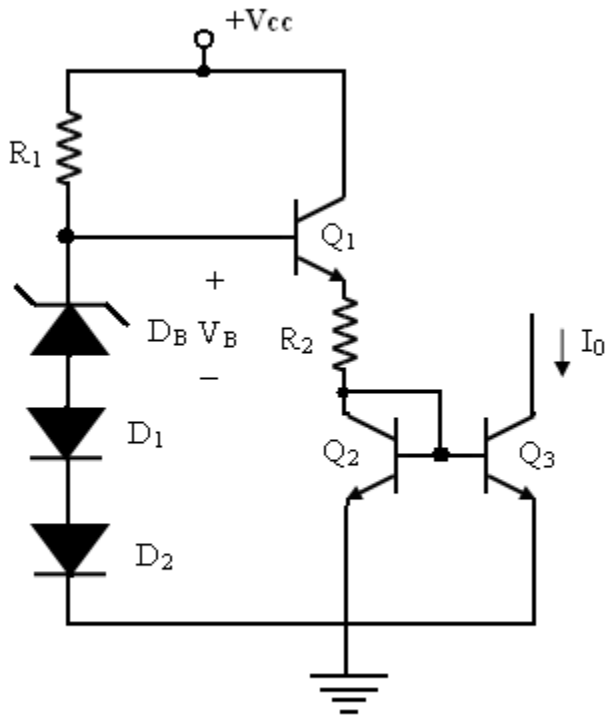
Voltage Reference using avalanche diode references
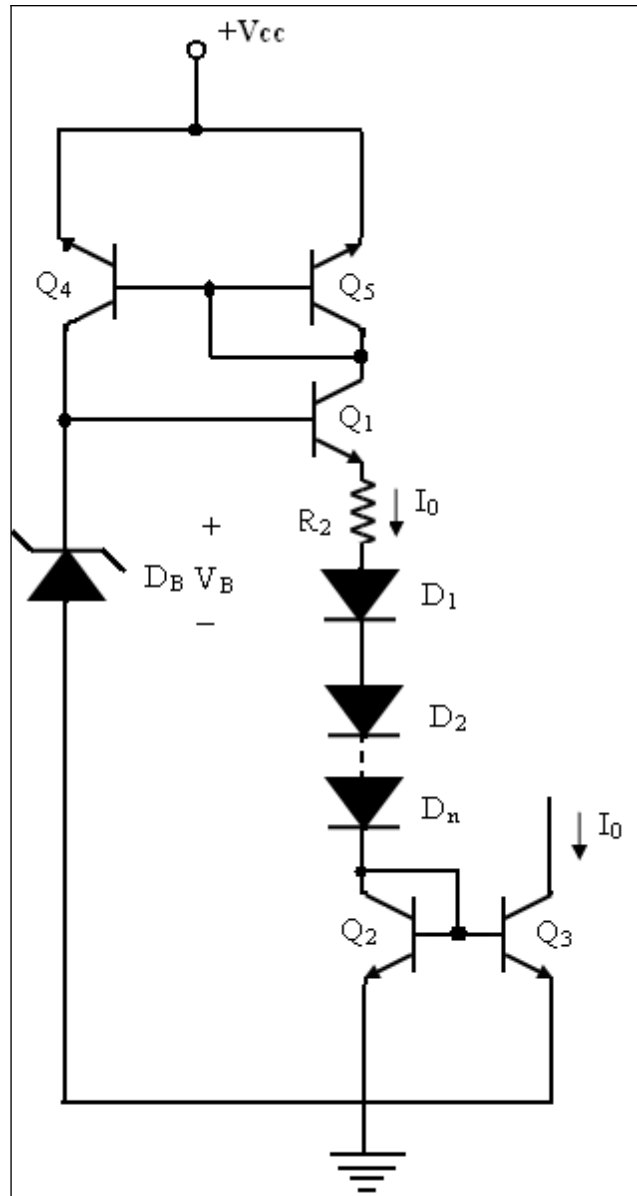
Temperature compensated avalanche diode reference source

Hence, the voltage across R_2 is approximately equal to that across $D_B = V_B$. Since Q_2 and Q_3 act as a current mirror circuit, current I_0 equals the current through R_2.

Therefore, $I_0 = \dfrac{V_B}{R_2}$

It shows that, the output current I_0 has low temperature coefficient, if the temperature coefficient of R_2 is low, such as that produced by a diffused resistor in IC fabrication.

The zero temperature coefficient for output current can be achieved, if diodes are added in series with R_2, so that they can compensate for the temperature variation of R_2 and V_B. The temperature compensated avalanche diode reference source circuit is shown in figure.

The transistor Q_4 and Q_5 form an active load current mirror circuit. The base voltage of Q_1 is the voltage V_B across zener D_B.

Then, $V_B = (V_{BE} * n) + V_{BE}$ across $Q_1 + V_{BE}$ across $Q_2 +$ drop across R_2. Here, n is the number of diodes.

It can be expressed as $V_B = n + 2\overset{\smile}{V}_{BE} + I_0 B R_2$

Differentiating for V_B, I_0, R_2 and V_{BE} partially, with respect to temperature T, we get

$$\frac{\partial V_B}{\partial T} = n + 2^a \frac{\partial V_{BE}}{\partial T} + R_2 \frac{\partial I_0}{\partial T} + I_0 \frac{\partial R_2}{\partial T}$$

Dividing throughout by $I_0 R_2$, we get

$$\frac{1}{I_0 R_2} \frac{\partial V_B}{\partial T} = \frac{n}{I_0 R_2} \frac{\partial V_{BE}}{\partial T} + \frac{1}{I_0} \frac{\partial I_0}{\partial T} + \frac{1}{R_@} \frac{\partial R_2}{\partial T}$$

Therefore, zero temperature coefficient of I_0 can be obtained, if the following condition is satisfied,

That is, $\dfrac{1}{I_0} \dfrac{\partial I_0}{\partial T} = 0 = \dfrac{1}{R_2 I_0} \dfrac{\partial V_B}{\partial T} n + 2^a \dfrac{\partial V_{BE}}{\partial T} @ \dfrac{1}{R_2} \dfrac{\partial R_2}{\partial T}$

Differential amplifier: The function of a differential amplifier is to amplify the difference between two signals. The need for differential amplifier arises in many physical measurements where response from dc to many MHz of frequency is required. This forms the basic input stage of an integrated amplifier.

The basic differential amplifier has the following important properties of

1. Excellent stability
2. High versatility and
3. High immunity to interference signals

The differential amplifier as a building block of the op-amp has the advantages of

1. Lower cost
2. easier fabrication as IC component and
3. closely matched components.

V$_1$

Amplifier with gain A$_{dm}$

V$_0$

V$_2$
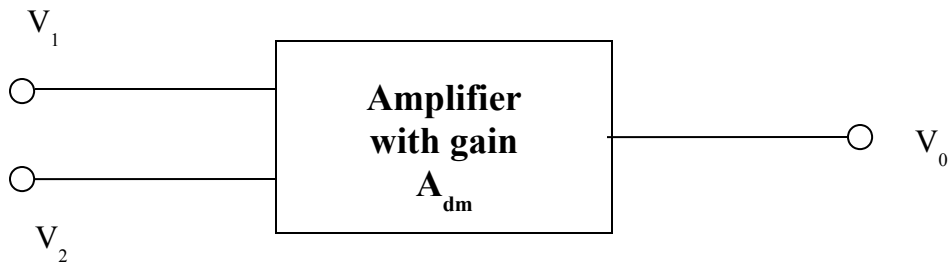
The above figure shows the basic block diagram of a differential amplifier, with two input terminals and one output terminal. The output signal of the differential amplifier is proportional to the difference between the two input signals.

That is $V_0 = A_{dm}(V_1 - V_2)$

If $V_1 = V_2$, then the output voltage is zero. A non-zero output voltage V_0 is obtained when V_1 and V_2 are not equal. The difference mode input voltage is defined as $V_m = V_1 - V_2$ and the common mode input voltage is defined as

$$V_{cm} = \frac{V_1 + V_2}{2}$$

These equation show that if $V_1 = V_2$, then the differential mode input signal is zero and common mode input signal is $V_{cm} = V_1 = V_2$.

Differential Amplifier with Active load:

Differential amplifier are designed with active loads to increase the differential mode voltage gain.

The open circuit voltage gain of an op-amp is needed to be as large as possible. This is achieved by cascading the gain stages which increase the phase shift and the amplifier also becomes vulnerable to oscillations. The gain can be increased by using large values of collector resistance. For such a

circuit, the voltage gain is given by $A_{dm} = @ g_m R_C = \dfrac{I_C R_C}{V_T}$

To increase the gain the $I_C R_C$ product must be made very large. However, there are limitations in IC fabrication such as,

1. a large value of resistance needs a large chip area.
2. for large R_C, the quiescent drop across the resistor increase and a large power supply will be required to maintain a given operating current.
3. Large monolithic resistor introduces large parasitic capacitances which limits the frequency response of the amplifier.

4. for linear operation of the differential pair, the devices should not be allowed to enter into saturation. This limits the max input voltage that can be applied to the bases of transistors Q_1 and Q_2 the base-collector junction must be allowed to become forward-biased by more than 0.5 V. The large value of load resistance produces a large dc voltage drop $(I_{EE}/2)R_C$, so that the collector voltage will be $V_C = V_{CC} - (I_{EE}/2)R_C$ and it will be substantially less than the supply voltage Vcc. This will reduce the input voltage range of the differential amplifier. Due to the reasons cited above, an active load is preferred in the differential amplifier configurations.

BJT Differential Amplifier using active loads:

A simple active load circuit for a differential amplifier is the current mirror active load as shown in figure. The active load comprises of transistors Q_3 and Q_4 with the transistor Q_3 connected as a diode with its base and collector shorted. The circuit is shown to drive a load R_L. When an ac input voltage is applied to the differential amplifier, the various currents of the circuit are given by

$I_{C4} = I_{C3} = I_{C1} = \dfrac{g_m V_{id}}{2}$. Where $I_{C4} = I_{C3}$ due to current mirror action. Here, I_{C2} is given by

$I_{C2} = @\dfrac{g_m V_{id}}{2}$. We know that the load current I_L entering the next stage is $I_L = I_{C2} @ I_{C4}$

.Therefore, $I_L = @\dfrac{g_m V_{id}}{2} @ \dfrac{g_m V_{id}}{2} = @g_m V_{id}$. Then, the output voltage from the differential amplifier is given by $V_0 = @I_L R_L = @ @g_m V_{id} R_L = g_m R_L V_{id}$. The ac voltage gain of the circuit is given by $A_s = \dfrac{V_0}{V_{id}} = \dfrac{g_m R_L V_{id}}{V_{id}} = g_m R_L$ .The differential amplifier can amplify the differential input signals and it provides single-ended output with a ground reference since the load R_L is connected to only one output terminal. This is made possible by the use of the current mirror active load.The output resistance R_0 of the circuit is that offered by the parallel combination of transistors Q_2 (NPN) and Q_4 (PNP). It is given by $R_r = r_{o2} \| r_{o4}$
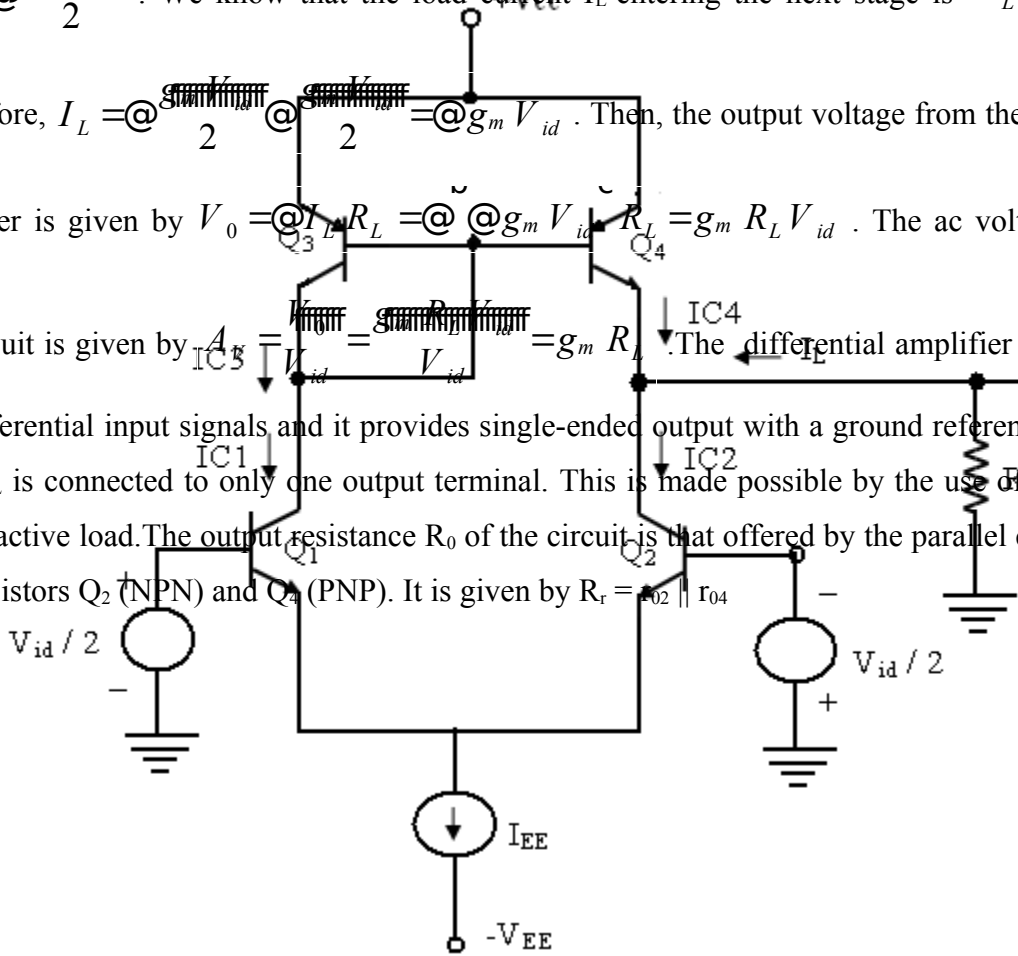
Analysis of BJT differential amplifier with active load:

Assuming $\frac{V_{out}}{2}=0$ *for transistor* Q_1 *and* Q_2 *and* $\beta =1$ *, then the bias current* I_{EE}
is divided equally between Q_1 *and* Q_2 *and*
hence, $I_{C1}=I_{C2}=I_{EE}$ *The current* I_{C1} *supplied by* Q_3 *is*

mirrored as I_{C4} *at the output of transitor* Q_4 *A*
therefore, $I_{C3}=I_{C4}=I_{EE}$ *and the dc current in the collector of* Q_4 *is exactly*
the current needed to satisfy Q_2 *A*
when β *is very large and* $V_{EC4}=V_{EC3}=V_{BE}$ *, the current mirror ratio becomes exactly*
unity A Then , the differential amplifier is completly balanced , and the output voltage
is $V_0=V_{CC}@V_{BE}$
Q @ points: The collector currents of all the transitors are equal A

that is, $I_{C1}=I_{C2}=I_{C3}=I_{C4}=\frac{I_{EE}}{2}A$

The Collector @ emitter voltages of Q_1 *and* Q_2 *are given by*

$$V_{CE1}=V_{CE2}=V_C@V_E=\breve{~}V_{CC}@V_{EB}\breve{~}@\breve{~}@V_{EB}\breve{~}=V_{CC}$$

The collector emitter voltages of Q_3 *and* Q_4 *are given by,*
$$V_{CE3}=V_{CE4}=V_{EB}$$
The input offset voltages V_{OS} *of the differential amplifier arises from the mismatches*
in the input devices Q_1 *,* Q_2 *and load drives* Q_3 *,* Q_4 *and from the base current of the*
Load devices A
an approxiamate expression for V_{OS} *is given by*

$$V_{OS}=V_T\left[\frac{\Delta I_{SP}}{I_{SP}}@\frac{\Delta I_{SN}}{I_{SN}}+\frac{2}{\beta}\right]$$

where β *represents the gain of PNP transistor and it is assumed that*
$$\Delta I_{SP}=I_{S3}@I_{S4}$$
$$I_{SP}=\frac{I_{S3}+I_{S4}}{2}$$
$$\Delta I_{SN}=I_{S1}@I_{S2}$$
and
$$I_{SN}=\frac{I_{S1}+I_{S2}}{2}$$

assuming a worst case value of F *4% for* $\frac{\Delta I_s}{I_s}$ *and* β *of 20,*

$$V_{OS} = V_T \left[0.04 + 0.04 + 0.1 \right] = 26 \times 10^{@3} \times 0.18 = 4.68mV$$

Eqn shows that, the offset is higher than that of a resistive loaded differential amplifier.
This can be reduced by the use of emitter resistors
for Q_3 and Q_4, and a transitor Q_5 in the current mirror
load as shown in figure.

CMRR of the differential amplifier using active load:

The differential amplifier using active load provides high voltage gain to the differential input signal and a single – ended output that is referenced to the ground is obtained. The differential amplifier which provides conversion for a differential signal to a single ended signal is necessary in differential input signal ended output amplifiers. The op-amp is one such circuit. The changes in the common-mode signal of the bias current source. This induces a change in I_{C2} and an identical change in I_{C1}. The change in I_{C1} will then produce a change in the PNP load devices, and thereby a change in I_{C4}, which is the collector current Q_4. The current I_{C4} is in such a direction as to cancel the change in I_{C2}. As a result of this, any common mode input does not cause a change in output.

Improved differential circuit using active load
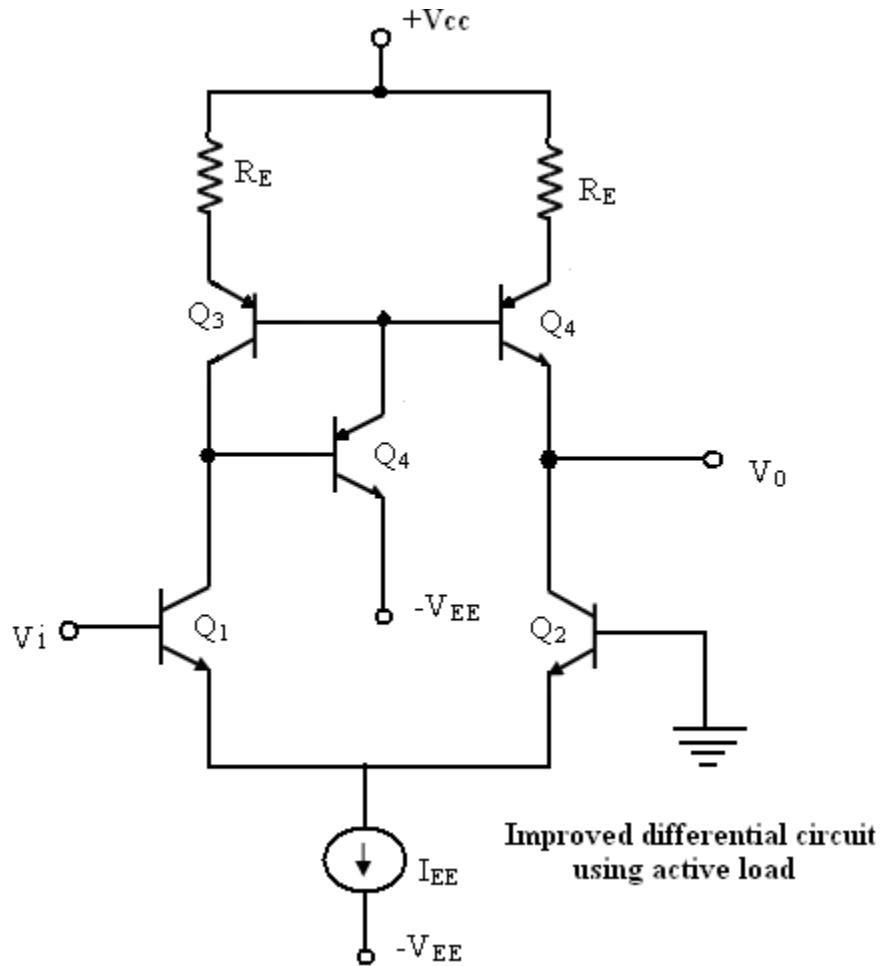
The voltage gain of the differential amplifier is independent of the quiescent current I_{EE}. This makes it possible to use very small value of I_{EE} as low as 20μa, while still maintaining a large voltage gain. Small value of I_{EE} is preferred, since it results in a small value of bias current and a large value for the input resistance. A limitation in choosing a small I_{EE} is, however, the fact that, it will result in a poor frequency response of the amplifier.

When a small value of bias current is required, the best approach is to use a JFET or MOSFET differential amplifier that is operated at comparatively higher values of I_{EE}.

+Vcc

R_{bias}

Q_5 Q_4

IC4

V_0

IC1

IC2

V_1 Q_1

Q_2 V_2

Q_6 Q_3

Differential to single ended
conversion with active load

-V_EE
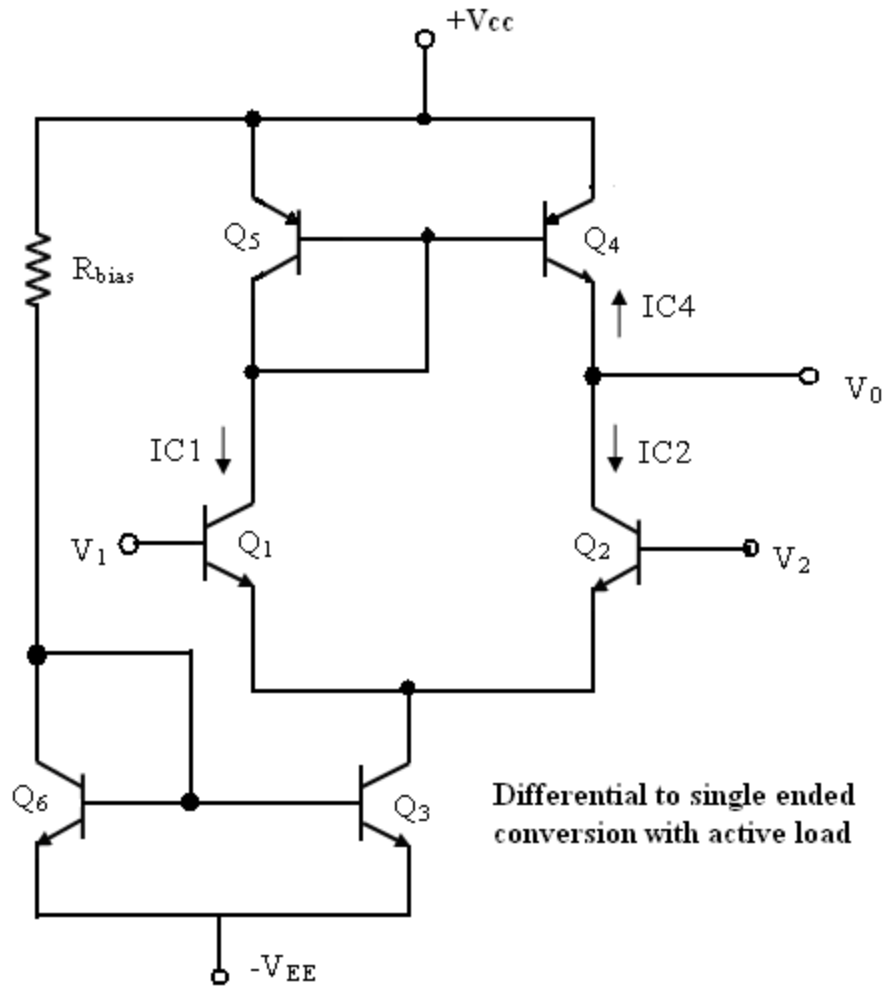
Differential Mode signal analysis:

The ac analysis of the differential amplifier can be made using the circuit model as shown below. The differential input transistor pair produces equal and opposite currents whose amplitude us given by $g_{m2} V_{id}/2$ at the collector of Q_1 and Q_2. The collector current i_{c1} is fed by the transistor Q_3 and it is mirrored at the output of Q_4. Therefore, the total current i_0 flowing through the load resistor R_L is given by

$$i_0 = 2 \frac{g_{m2} V_{id}}{2} = g_{m2} V_{id}$$

Then the output voltage is

$$V_0 = i_0 R_L = g_{m2} R_L V_{id}$$

and the differential mode gain A_{dd} of the differential amplifier is given by

$$A_{dd} = \frac{V_0}{V_{dm}} = g_{m2} R_L$$

This current mirror provides a single ended output which has a voltage equal to the maximum gain of the common emitter amplifier.

The power of the current mirror can be increased by including additional common collector stages at the o/p of the differential input stage. A bipolar differential amplifier structure with additional stages is shown in figure. The resistance at the output of the differential stage is now given by the parallel combination of transistors Q_2 and Q_4 and the input resistance is offered by Q_5. Then, the equivalent resistance is expressed by $R_{eq} = r_{o2} \| r_{o4} \| r_{i5} = r_{i5}$. The gain of the differential stage then

becomes $A_{dm} = g_{m2} R_{eq} = g_{m2} r_{i5} = \beta_{05} \dfrac{I}{I_{C5}}$.

BJT Differential amplifier with differential mode input
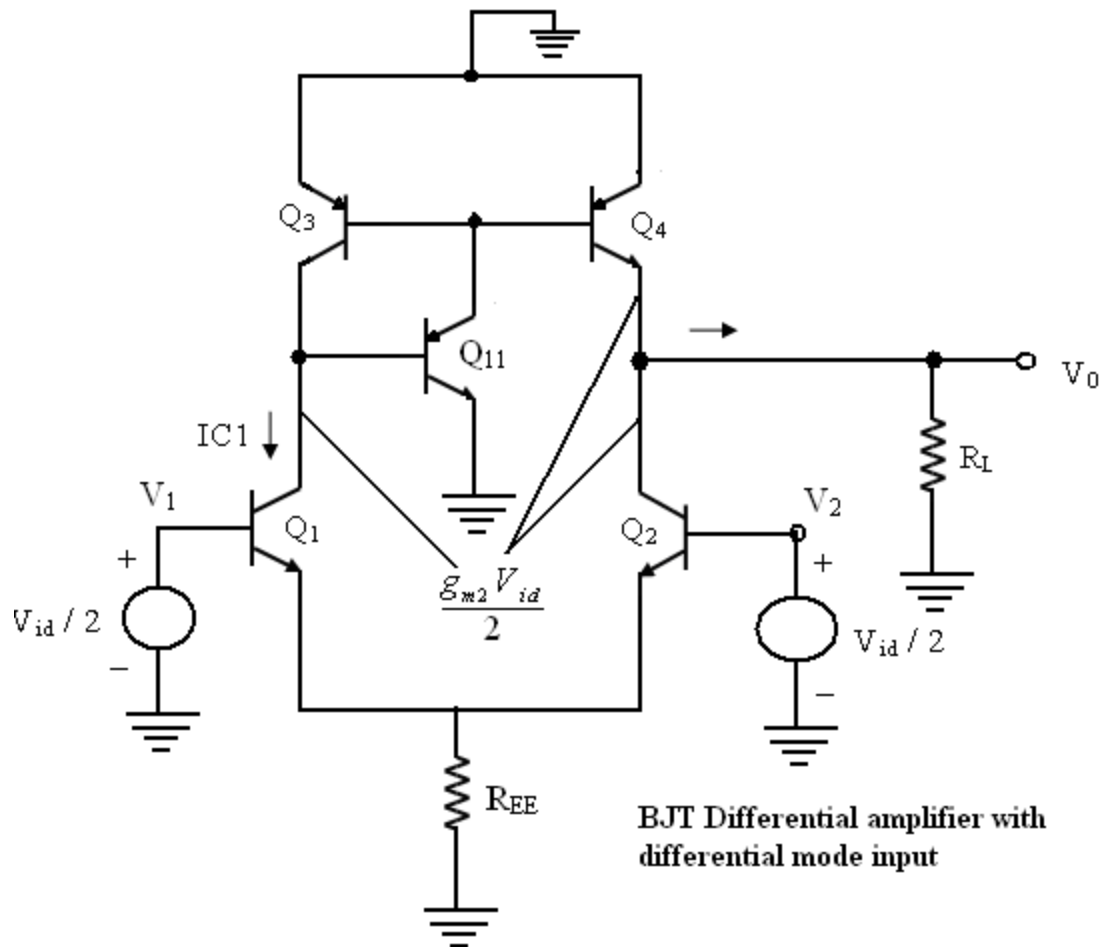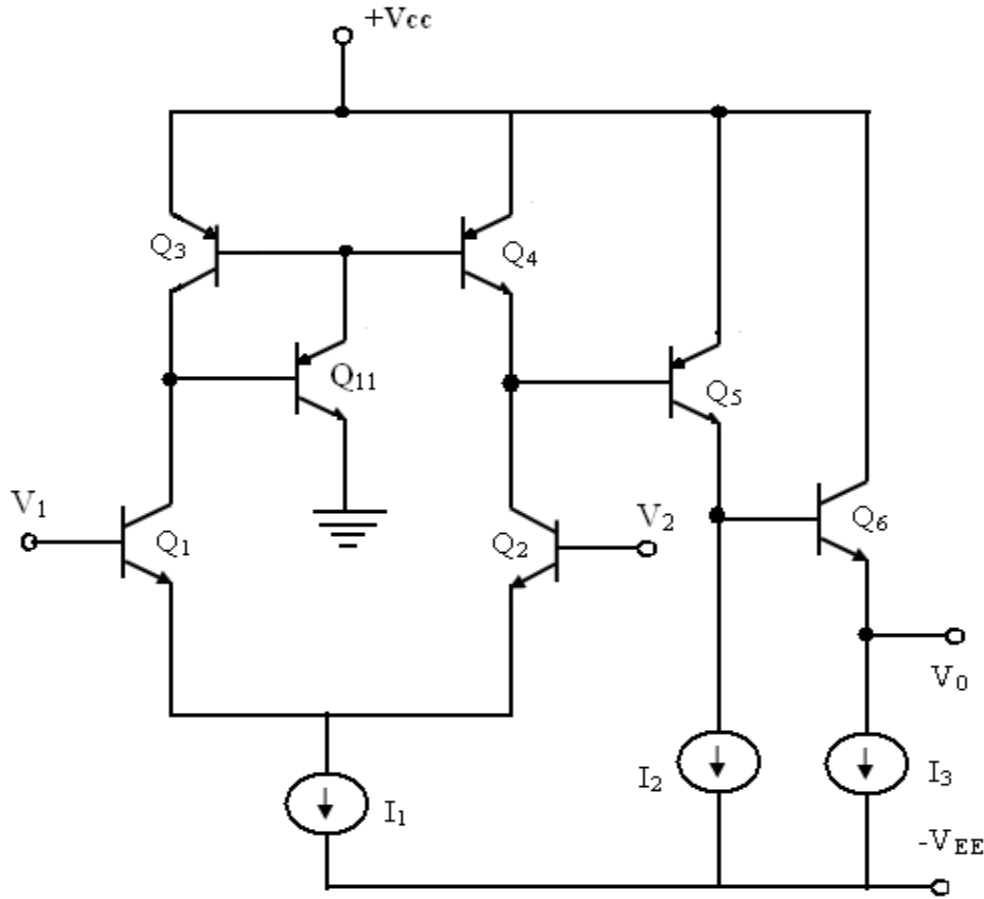
BJT Differential Amplifier with additional output stage

Bipolar differential amplifier with common mode input signals:

The common mode input signal induces a common mode current i_{ic} in each of the differential transistor pair Q_1 and Q_2. The common current i_{ic} is given by

$$i_{ic} = \frac{g_{m2}}{1 + 2g_{m2}R_{EE}} V_{ic} \approx \frac{V_{ic}}{2R_{EE}}$$

The current flow through the transistor Q_1 is supplied by the reference current of transistor Q_3. This current is replicated or mirrored in the transistor Q_4 and it produces exactly the same current needed at the collector of Q_2. Therefore, the output current and hence the output voltage and common mode conversion gain A_{cd} are all zero.

However, for an actual amplifier, the common mode gain is determined by small imbalances generated in the bipolar transistor fabrication and the overall asymmetry in the amplifier. One of the main factors is due to the current gain defect on the active load, and it can be minimized through the use of buffered current mirror using the transistor Q_5 as shown in figure.

BJT Differential Amplifier with common mode input
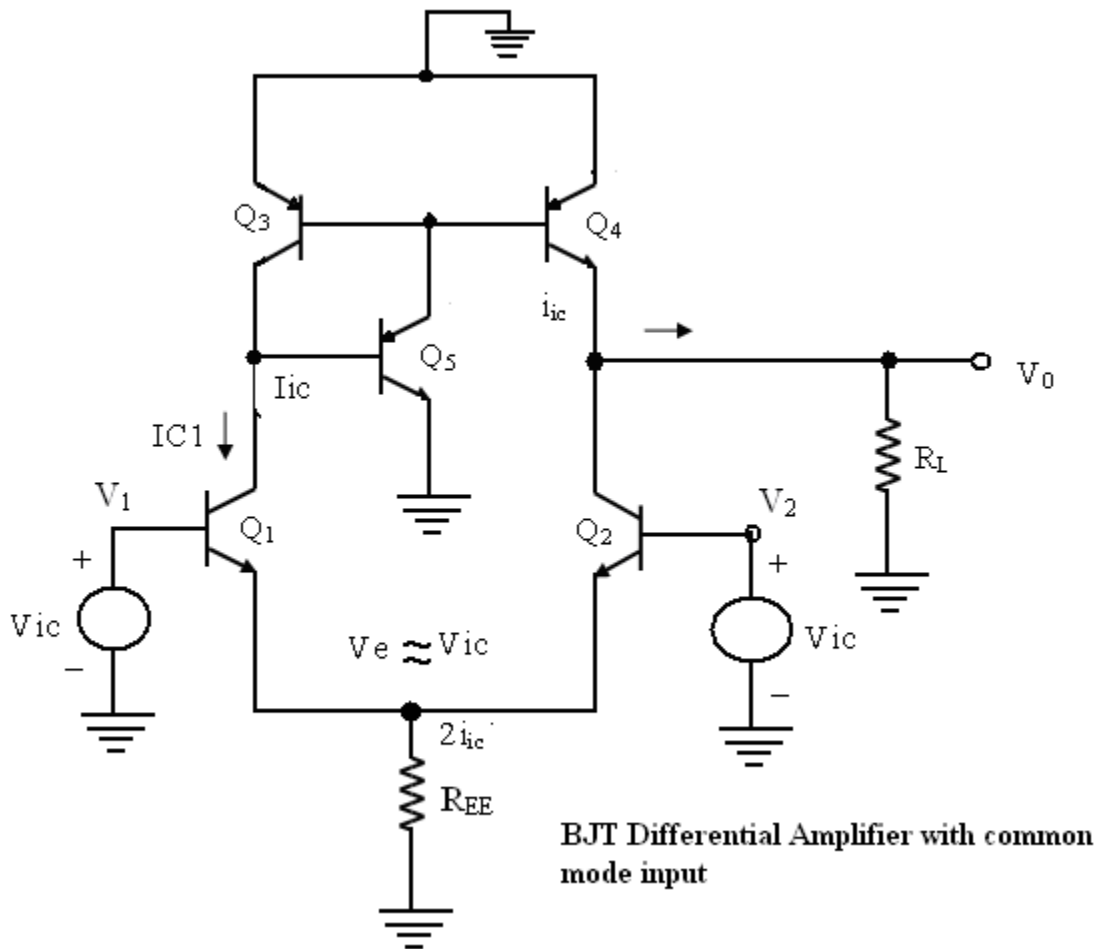
General Operational Amplifier:

An operational amplifier generally consists of three stages, anmely,1. a differential amplifier 2. additional amplifier stages to provide the required voltage gain and dc level shifting 3. an emitter-follower or source follower output stage to provide current gain and low output resistance.

A low-frequency or dc gain of approximately 10^4 is desired for a general purpose op-amp and hence, the use of active load is preferred in the internal circuitry of op-amp. The output voltage is required to be at ground, when the differential input voltages is zero, and this necessitates the use of dual polarity supply voltage. Since the output resistance of op-amp is required to be low, a complementary push-pull emitter – follower or source follower output stage is employed. Moreover, as the input bias currents are to be very small of the order of picoamperes, an FET input stage is normally preferred. The figure shows a general op-amp circuit using JFET input devices.

	V+			

Differential Input stage   Gain stage   Output stage
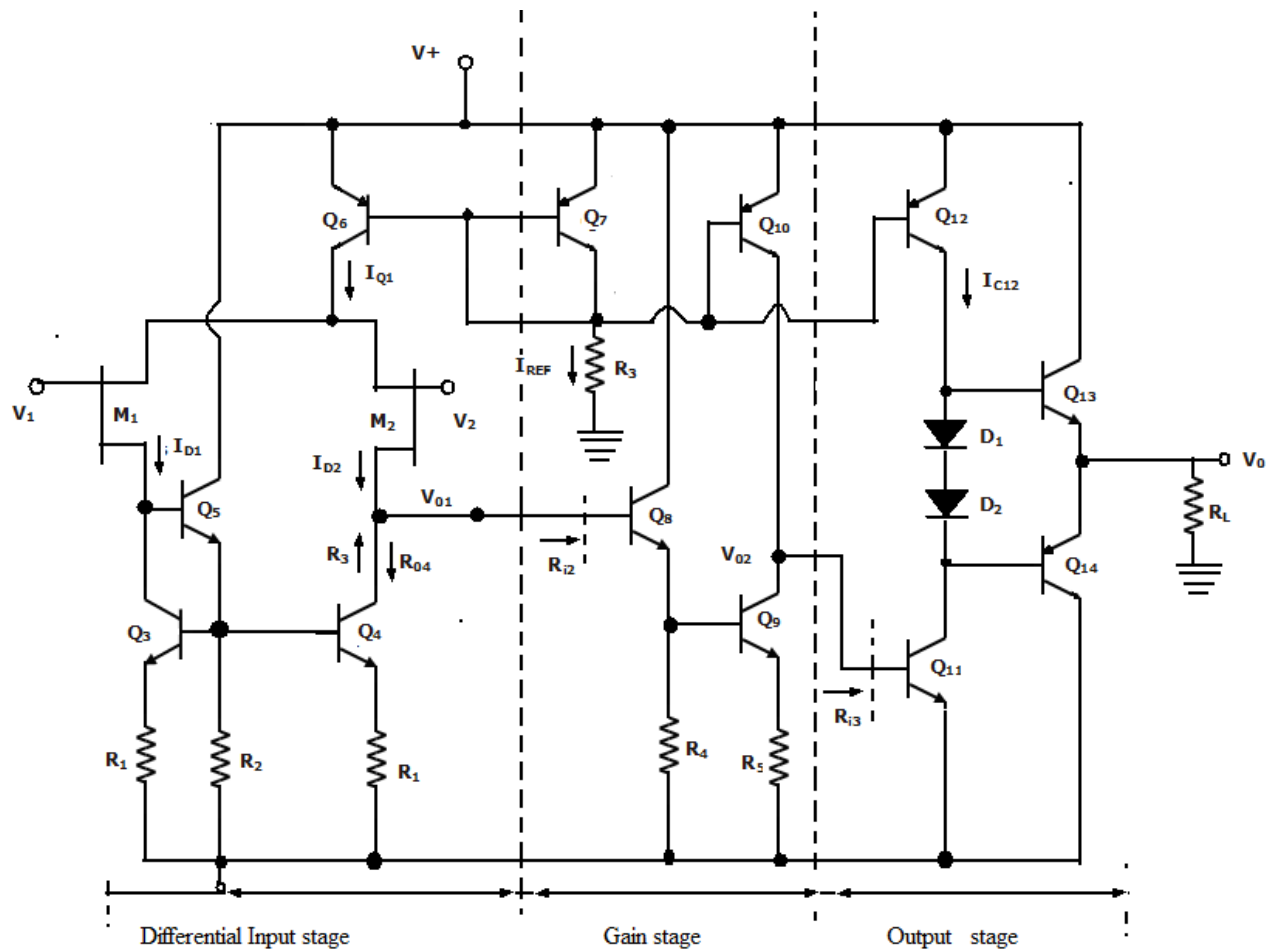
Input stage:

The input differential amplifier stage uses p-channel JFETs M_1 and M_2. It employs a three-transistor active load formed by Q_3, Q_4, and Q_5. the bias current for the stage is provided by a two-transistor current source using PNP transistors Q_6 and Q_7. Resistor R_1 increases the output resistance seen looking into the collector of Q_4 as indicated by R_{04}. This is necessary to provide bias current stability against the transistor parameter variations. Resistor R_2 establishes a definite bias current through Q_5. A single ended output is taken out at the collector of Q_4.

MOSFET's are used in place of JFETs with additional devices in the circuit to prevent any damage for the gate oxide due to electrostatic discharges.

Gain stage:

The second stage or the gain stage uses Darlington transistor pair formed by Q_8 and Q_9 as shown in figure. The transistor Q_8 is connected as an emitter follower, providing large input resistance.

Therefore, it minimizes the loading effect on the input differential amplifier stage. The transistor Q_9 provides an additional gain and Q_{10} acts as an active load for this stage. The current mirror formed by Q_7 and Q_{10} establishes the bias current for Q_9. The V_{BE} drop across Q_9 and drop across R_5 constitute the voltage drop across R_4, and this voltage sets the current through Q_8. It can be set to a small value, such that the base current of Q_8 also is very less.

Output stage:

The final stage of the op-amp is a class AB complementary push-pull output stage. Q_{11} is an emitter follower, providing a large input resistance for minimizing the loading effects on the gain stage. Bias current for Q_{11} is provided by the current mirror formed by Q_7 and $Q_{12,}$ through Q_{13} and Q_{14} for minimizing the cross over distortion. Transistors can also be used in place of the two diodes.

The overall voltage gain A_V of the op-amp is the product of voltage gain of each stage as given by

$A_V = |A_d| \, |A_2||A_3|$

Where A_d is the gain of the differential amplifier stage, A_2 is the gain of the second gain stage and A_3 is the gain of the output stage.

IC 741 Bipolar operational amplifier:

The IC 741 produced since 1966 by several manufactures is a widely used general purpose operational amplifier. Figure shows that equivalent circuit of the 741 op-amp, divided into various individual stages. The op-amp circuit consists of three stages.

1. the input differential amplifier
2. The gain stage
3. the output stage.

A bias circuit is used to establish the bias current for whole of the circuit in the IC. The op-amp is supplied with positive and negative supply voltages of value ± 15V, and the supply voltages as low as ±5V can also be used.

Bias Circuit:

The reference bias current I_{REF} for the 741 circuit is established by the bias circuit consisting of two diodes-connected transistors Q_{11} and Q_{12} and resistor R_5. The widlar current source formed by Q_{11}, Q_{10} and R_4 provide bias current for the differential amplifier stage at the collector of Q_{10}. Transistors Q_8 and Q_9 form another current mirror providing bias current for the differential amplifier. The

reference bias current I_{REF} also provides mirrored and proportional current at the collector of the double –collector lateral PNP transistor Q_{13}. The transistor Q_{13} and Q_{12} thus form a two-output current mirror with Q_{13A} providing bias current for output stage and Q_{13B} providing bias current for Q_{17}. The transistor Q_{18} and Q_{19} provide dc bias for the output stage. Formed by Q_{14} and Q_{20} and they establish two V_{BE} drops of potential difference between the bases of Q_{14} and Q_{18}.

Input stage:

The input differential amplifier stage consists of transistors Q_1 through Q_7 with biasing provided by Q_8 through Q_{12}. The transistor Q_1 and Q_2 form emitter – followers contributing to high differential input resistance, and whose output currents are inputs to the common base amplifier using Q_3 and Q_4 which offers a large voltage gain.

The transistors Q5, Q6 and Q7 along with resistors R_1, R_2 and R_3 from the active load for input stage. The single-ended output is available at the collector of Q_6. the two null terminals in the input stage facilitate the null adjustment. The lateral PNP transistors Q_3 and Q_4 provide additional protection against voltage breakdown conditions. The emitter-base junction Q_3 and Q_4 have higher emitter-base breakdown voltages of about 50V. Therefore, placing PNP transistors in series with NPN transistors provide protection against accidental shorting of supply to the input terminals.

Gain Stage:

The Second or the gain stage consists of transistors Q_{16} and Q_{17}, with Q_{16} acting as an emitter – follower for achieving high input resistance. The transistor Q_{17} operates in common emitter configuration with its collector voltage applied as input to the output stage. Level shifting is done for this signal at this stage.

Internal compensation through Miller compensation technique is achieved using the feedback capacitor C_1 connected between the output and input terminals of the gain stage.

Output stage:

The output stage is a class AB circuit consisting of complementary emitter follower transistor pair Q_{14} and Q_{20}. Hence, they provide an effective loss output resistance and current gain.

The output of the gain stage is connected at the base of Q_{22}, which is connected as an emitter – follower providing a very high input resistance, and it offers no appreciable loading effect on the

gain stage. It is biased by transistor Q_{13A} which also drives Q_{18} and $Q_{19,}$ that are used for establishing a quiescent bias current in the output transistors Q_{14} and $Q_{20.}$

Ideal op-amp characteristics:

1. Infinite voltage gain A.
2. Infinite input resistance R_i, so that almost any signal source can drive it and there is no loading of the proceeding stage.
3. Zero output resistance R_o, so that the output can drive an infinite number of other devices.
4. Zero output voltage, when input voltage is zero.
5. Infinite bandwidth, so that any frequency signals from o to ∞ HZ can be amplified with out attenuation.
6. Infinite common mode rejection ratio, so that the output common mode noise voltage is zero.
7. Infinite slew rate, so that output voltage changes occur simultaneously with input voltage changes.

AC Characteristics:

For small signal sinusoidal (AC) application one has to know the ac characteristics such as frequency response and slew-rate.

Frequency Response:

The variation in operating frequency will cause variations in gain magnitude and its phase angle. The manner in which the gain of the op-amp responds to different frequencies is called the frequency response. Op-amp should have an infinite bandwidth Bw $=\infty$ (i.e) if its open loop gain in 90dB with dc signal its gain should remain the same 90 dB through audio and onto high radio frequency. The op-amp gain decreases (roll-off) at higher frequency what reasons to decrease gain after a certain frequency reached. There must be a capacitive component in the equivalent circuit of the op-amp. For an op-amp with only one break (corner) frequency all the capacitors effects can be represented by a single capacitor C. Below fig is a modified variation of the low frequency model with capacitor C at the o/p.
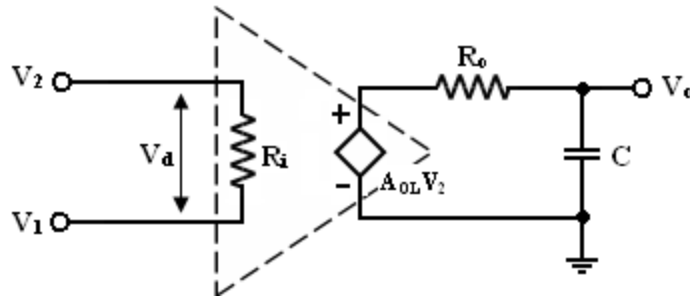
There is one pole due to $R_0 C$ and one -20dB/decade. The open loop voltage gain of an op-amp with only one corner frequency is obtained from above fig.

$$V_0 = \frac{-jX_C}{R_0 - jX_C} A_{OL}\, Vd \qquad @@@@\ 26^a$$

$$or\ A = \frac{V_0}{Vd} = \frac{A_{OL}}{1 + 2j\pi + R_0\, C} \qquad$$

$$or\ A = \frac{A_{OL}}{1 + j\dfrac{f}{f_1}} \qquad @@@@@\ 27^a$$

$$where\ f_1 = \frac{1}{2\pi R_0\, C} \qquad @@@\ 28^a$$

f1 is the corner frequency or the upper 3 dB frequency of the op-amp. The magnitude and phase angle of the open loop volt gain are fu of frequency can be written as,

$$|A| = \sqrt{\frac{A_{OL}}{1 + \left(\dfrac{f}{f_1}\right)^2}} \qquad @@@@@@@\ 29^a$$

$$\phi = -\tan^{-1}\left(\frac{f}{f_1}\right)$$

The magnitude and phase angle characteristics from eqn (29) and (30)

1. For frequency f<< f_1 the magnitude of the gain is 20 log A_{OL} in dB.
2. At frequency f = f_1 the gain in 3 dB down from the dc value of A_{OL} in dB. This frequency f_1 is called corner frequency.
3. For f>> f_1 the fain roll-off at the rate off -20dB/decade or -6dB/decade.
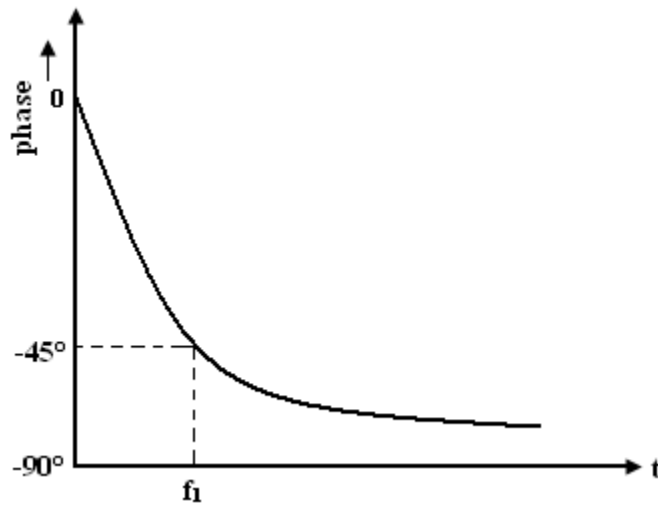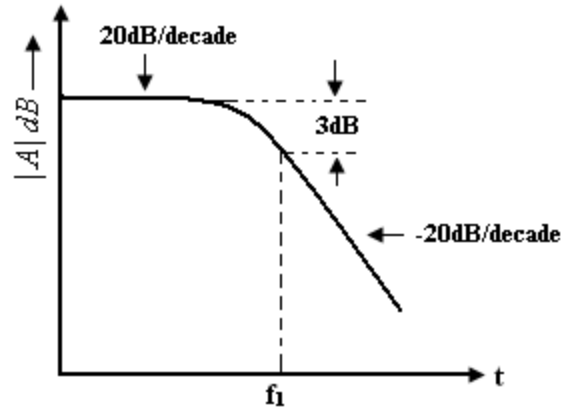
From the phase characteristics that the phase angle is zero at frequency $f = 0$.

At the corner frequency f_1 the phase angle is -45^0 (lagging and a infinite frequency the phase angle is -90^0. It shows that a maximum of 90^0 phase change can occur in an op-amp with a single capacitor C. Zero frequency is taken as te decade below the corner frequency and infinite frequency is one decade above the corner frequency. The voltage transfer in a S-domain can be written as

$$A = \frac{A_{OL}}{1 + j \frac{f}{f_1}} = \frac{A_{OL}}{1 + j \frac{w}{w_1}}$$

$$A = \frac{A_{OL} w_1}{jw + w1} = \frac{A_{OL} W_1}{S + W_1}$$

The transfer f_0 of as op-amp with 3 break frequency can be assumed as,

$$A = \frac{A_{OL}}{\left(1+j\dfrac{f}{f_1}\right)\left(1+j\dfrac{f}{f_2}\right)\left(1+j\dfrac{f}{f_3}\right)} \qquad 0<f_1<f_2<f_3 \qquad @@@@\ 31^a$$

$$A = \frac{A_{OL}}{(s+w_1)\,(s+w_2)\,(s+w_3)} \qquad @@@\ 32^a \quad with\ 0<w_1<w_2<w_3$$
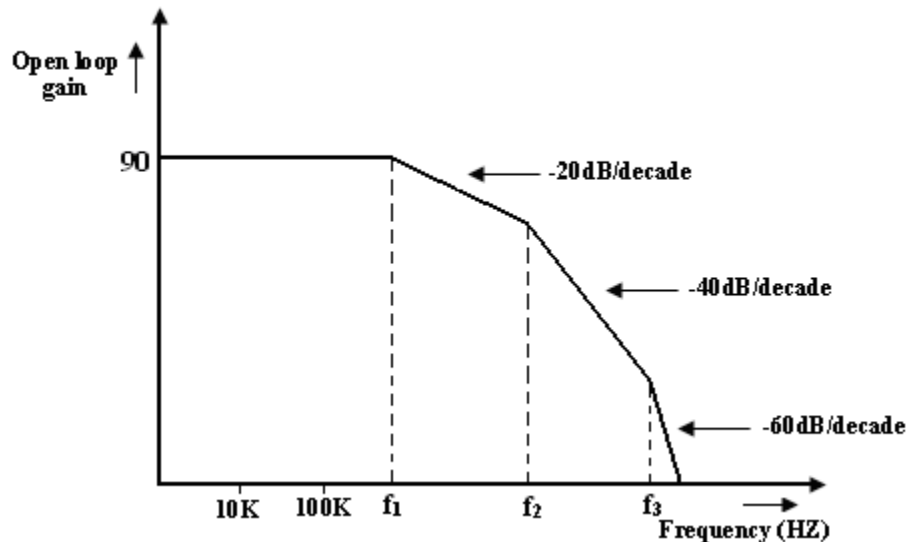
Circuit Stability:

A circuit or a group of circuit connected together as a system is said to be stable, if its o/p reaches a fixed value in a finite time. (or) A system is said to be unstable, if its o/p increases with time instead of achieving a fixed value. In fact the o/p of an unstable sys keeps on increasing until the system break down. The unstable system are impractical and need be made stable. The criterian gn for stability is used when the system is to be tested practically. In theoretically, always used to test system for stability , ex: Bode plots.

Bode plots are compared of magnitude Vs Frequency and phase angle Vs frequency. Any system whose stability is to be determined can represented by the block diagram.
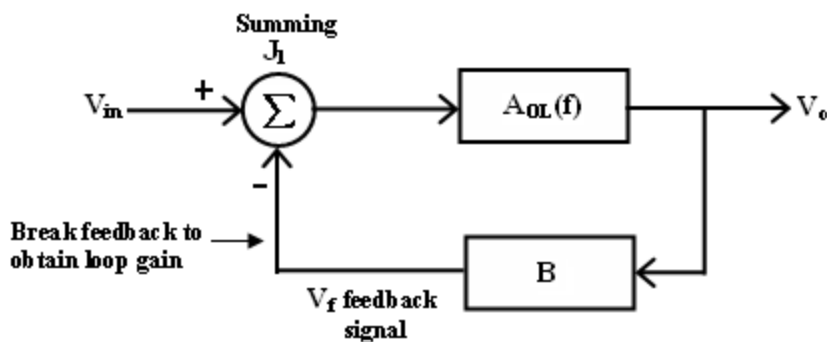
The block between the output and input is referred to as forward block and the block between the output signal and f/b signal is referred to as feedback block. The content of each block is referred "Transfer frequency' From fig we represented it by $A_{OL}(f)$ which is given by

$A_{OL}(f) = V_0/Vin$ if $V_f = 0$. -----(1)

where $A_{OL}(f)$ = open loop volt gain. The closed loop gain A_f is given by

$A_F = V_0/Vin$

$A_F = A_{OL} / (1+(A_{OL})(B)$ ----(2)

B = gain of feedback circuit.

B is a constant if the feedback circuit uses only resistive components. Once the magnitude Vs frequency and phase angle Vs frequency plots are drawn, system stability may be determined as follows

1. Method:1:

Determine the phase angle when the magnitude of $(A_{OL})(B)$ is 0dB (or) 1. If phase angle is > .-180^0, the system is stable. However, the some systems the magnitude may never be 0, in that cases method 2, must be used.

2. Method 2:

Determine the phase angle when the magnitude of $(A_{OL})(B)$ is 0dB (or) 1. If phase angle is > .-180^0, If the magnitude is –ve decibels then the system is stable. However, the some systems the phase angle of a system may reach -180^0, under such conditions method 1 must be used to determine the system stability.

Slew Rate:

Another important frequency related parameter of an op-amp is the slew rate. (Slew rate is the maximum rate of change of output voltage with respect to time. Specified in V/μs).

Reason for Slew rate:

There is usually a capacitor within 0, outside an op-amp oscillation. It is this capacitor which prevents the o/p voltage from fast changing input. The rate at which the volt across the capacitor increases is given by

$dVc/dt = I/C$ --------(1)

I -> Maximum amount furnished by the op-amp to capacitor C. Op-amp should have the either a higher current or small compensating capacitors.

For 741 IC, the maximum internal capacitor charging current is limited to about 15μA. So the slew rate of 741 IC is

$$SR = dV_c/dt \mid max = I_{max}/C \ .$$

For a sine wave input, the effect of slew rate can be calculated as consider volt follower -> The input is large amp, high frequency sine wave .

If $V_s = V_m \, Sinwt$ then output $V_0 = V_m \, sinwt$. The rate of change of output is given by

$$dV_0/dt \ = \ V_m \, w \, coswt.$$
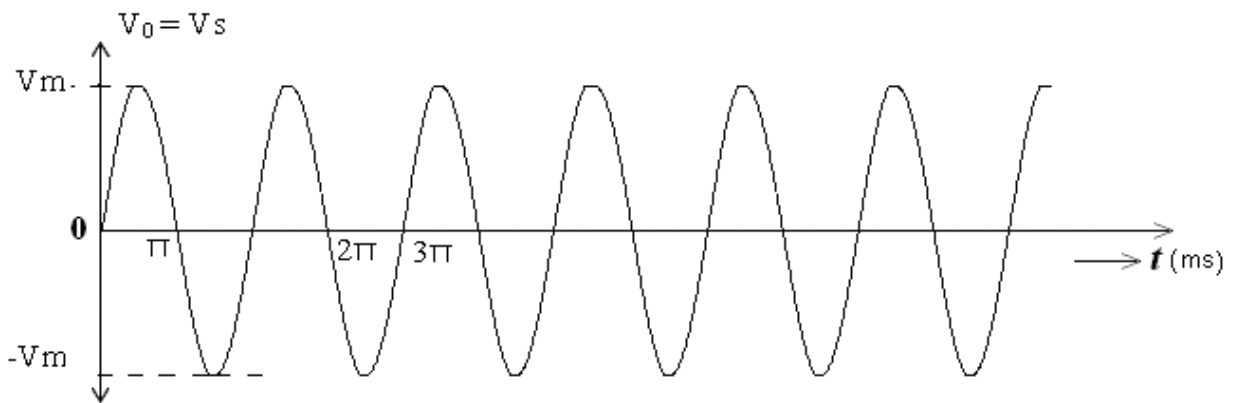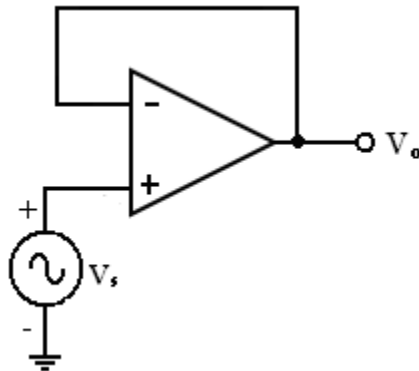
Input and Output Waveforms

The max rate of change of output across when coswt =1

(i.e) SR = $dV_0/dt \mid max = wV_m.$

$SR = 2\prod fV_m \, V/s = 2\prod fV_m$ v/ms.

Thus the maximum frequency fmax at which we can obtain an undistorted output volt of peak value Vm is given by

fmax (Hz) $= $ Slew rate/6.28 * Vm .

called the full power response. It is maximum frequency of a large amplitude sine wave with which op-amp can have without distortion.

DC Characteristics of op-amp:
Current is taken from the source into the op-amp inputs respond differently to current and voltage due to mismatch in transistor.

DC output voltages are,

1. Input bias current
2. Input offset current
3. Input offset voltage
4. Thermal drift

Input bias current:
The op-amp's input is differential amplifier, which may be made of BJT or FET.

➢ In an ideal op-amp, we assumed that no current is drawn from the input terminals.

➢ The base currents entering into the inverting and non-inverting terminals (I_B^- & I_B^+ respectively).

➢ Even though both the transistors are identical, I_B^- and I_B^+ are not exactly equal due to internal imbalance between the two inputs.

➢ Manufacturers specify the input bias current I_B

Input Bias Current

Inverting Amplifier with Bias Current
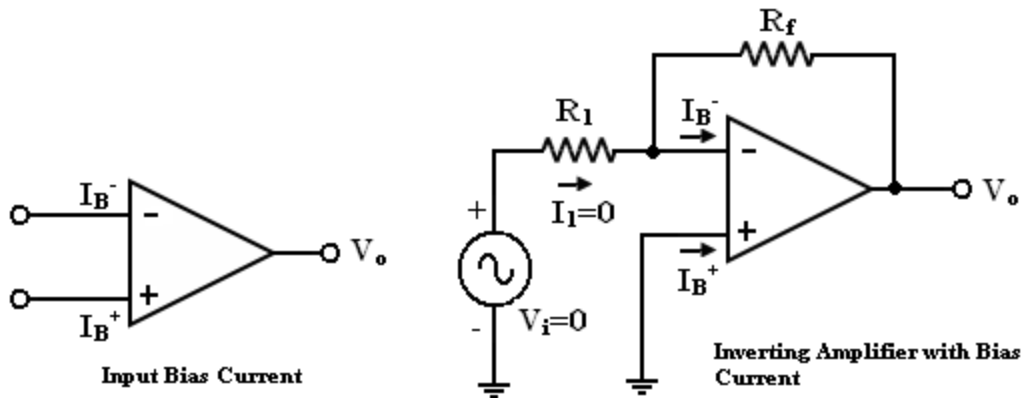
So,
$$I_B = \frac{I_B^+ + I_B^-}{2}$$

If input voltage $V_i = 0V$. The output Voltage V_o should also be ($V_o = 0$)

$I_B = 500nA$

We find that the output voltage is offset by,

$$V_o = I_B R_f \cdot 2^a$$

Op-amp with a 1M feedback resistor

$$V_o = 5000nA \times 1M = 500mV$$

The output is driven to 500mV with zero input, because of the bias currents.

In application where the signal levels are measured in mV, this is totally unacceptable. This can be compensated. Where a compensation resistor R_{comp} has been added between the non-inverting input terminal and ground as shown in the figure below.

Bias Current
Compensation
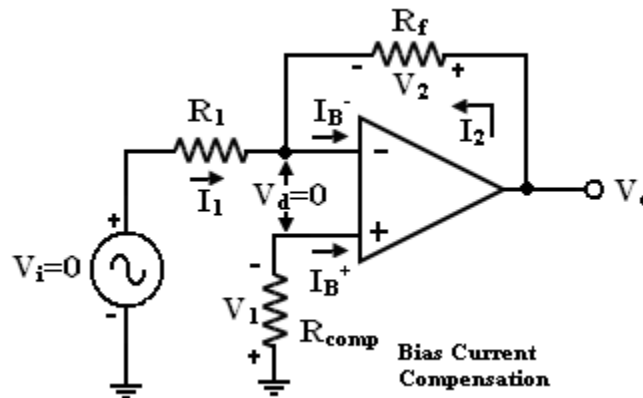
Current I_B^+ flowing through the compensating resistor R_{comp}, then by KVL we get,

$-V_1+0+V_2-V_o = 0$ (or)

$V_o = V_2 - V_1$ ——>(3)

By selecting proper value of R_{comp}, V_2 can be cancelled with V_1 and the $V_o = 0$. The value of R_{comp} is derived a

$V_1 = I_B^+ R_{comp}$ (or)

$I_B^+ = V_1/R_{comp}$ ——>(4)

The node 'a' is at voltage $(-V_1)$. Because the voltage at the non-inverting input terminal is $(-V_1)$. So with $V_i = 0$ we get,

$I_1 = V_1/R_1$ ——>(5)

$I_2 = V_2/R_f$ ——>(6)

For compensation, V_o should equal to zero ($V_o = 0$, $V_i = 0$). i.e. from equation (3) $V_2 = V_1$. So that,

$I_2 = V_1/R_f$ ——>(7)

KCL at node 'a' gives,

$I_B^- = I_2 + I_1$

$$I_B^{@} = \frac{V}{R_f} + \frac{V}{R_1}$$

$$I_B^{@} = V_1 \frac{R_1 + R_f}{R_1 R_f} \qquad (8)$$

Assume $I_B^- = I_B^+$ and using equation (4) & (8) we get

$$V_1 \frac{R_1 + R_f}{R_1 R_f} = \frac{V}{R_{comp}}$$

$$R_{comp} = \frac{R_1 R_f}{R_1 + R_f}$$

$$R_{comp} = R_1 \| R_f \qquad\longrightarrow (9)$$

i.e. to compensate for bias current, the compensating resistor, R_{comp} should be equal to the parallel combination of resistor R_1 and R_f.

Input offset current:

- ➢ Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal.
- ➢ Since the input transistor cannot be made identical. There will always be some small difference between I_B^+ and I_B^-. This difference is called the offset current

$$|I_{os}| = I_B^+ - I_B^- \qquad\longrightarrow (10)$$

Offset current I_{os} for BJT op-amp is 200nA and for FET op-amp is 10pA. Even with bias current compensation, offset current will produce an output voltage when $V_i = 0$.

$$V_1 = I_B^+ R_{comp} \qquad\longrightarrow (11)$$

And $\qquad I_1 = V_1/R_1 \qquad\longrightarrow (12)$

KCL at node 'a' gives,

$$I_2 = (I_B^- - I_1)$$

$$I_2 = I_B^{@} - \left(I_B^+ \frac{R_{comp}}{R_1} \right) \qquad (13)$$

Again

$$V_0 = I_2 R_f - V_1$$

$$V_o = I_2 R_f - I_B^+ R_{comp}$$

$$V_o = \left[I_B^{@} - I_B^+ \frac{R_{comp}}{R_1} \right] R_f - I_B^+ R_{comp} \qquad (14)$$

Substitute equation (9) and after algebraic manipulation ,

$$V_o = R_f \left[I_B^{@} - I_B^{+} \frac{R_{\dots}}{R_1} \right] - I_B^{+} R_{comp}$$

$$V_o = R_{fI_B}^{@} - I_B^{+} \frac{R_{\dots}}{R_1} R_f - I_B^{+} R_{comp}$$

$$V_o = R_f I_B^{@} - I_B^{+} R_{comp} \left[\frac{R_{\dots}}{R_1} + 1 \right]$$

$$V_o = R_f I_B^{@} - I_B^{+} R_{comp} \left[\frac{R_{\dots} + R_{\dots}}{R_1} \right]$$

$$V_o = R_f I_B^{@} - I_B^{+} \frac{R_{\dots} R_{\dots}}{R_1}$$

$$V_o = R_f I_B^{@} - I_B^{+} R_f$$

$$V_o = R_f \left(I_B^{@} - I_B^{+} \right) \qquad (15)$$

$$V_o = R_f I_{os} \qquad (16)$$

So even with bias current compensation and with feedback resistor of 1M, a BJT op-amp has an output offset voltage

$$V_o = 1M \, \Omega \ X \ 200nA$$
$$V_o = 200mV \text{ with } V_i = 0$$

Equation (16) the offset current can be minimized by keeping feedback resistance small.

➢ Unfortunately to obtain high input impedance, R_1 must be kept large.

➢ R_1 large, the feedback resistor R_f must also be high. So as to obtain reasonable gain.

The T-feedback network is a good solution. This will allow large feedback resistance, while keeping the resistance to ground low (in dotted line).

➢ The T-network provides a feedback signal as if the network were a single feedback resistor.

By T to Π conversion,

$$R_f = \frac{R_{\dots}^2 - R_{\dots} R_{\dots}}{R_s} \qquad (17)$$

To design T- network first pick $R_t << R_f/2 \longrightarrow (18)$

Then calculate $R_s = \frac{R_{\dots}^2}{R_f \, 2R_t} \qquad (19)$
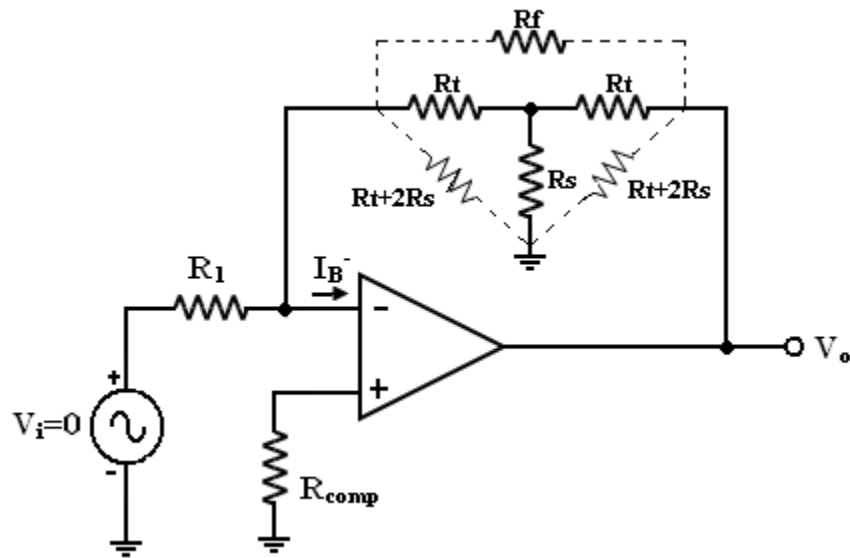
Input offset voltage:

Inspite of the use of the above compensating techniques, it is found that the output voltage may still not be zero with zero input voltage [$V_o \neq 0$ with $V_i = 0$]. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminal to make output (V_o) = 0.

This voltage is called input offset voltage V_{os}. This is the voltage required to be applied at the input for making output voltage to zero ($V_o = 0$).

Input Offset Voltage
Fig (a)

Non-Inverting Amplifier
Fig (b)

Inverting Amplifier
Fig (c)

$V_o = (1+R_f/R_1)V_{os}$

$V_i = 0V$

Equivalent circuit for $V_i = 0V$
Fig (d)
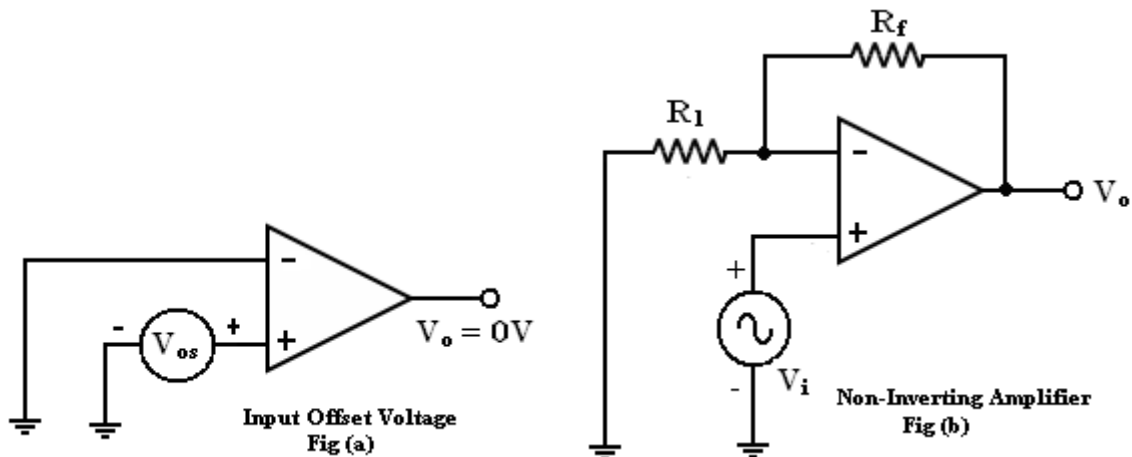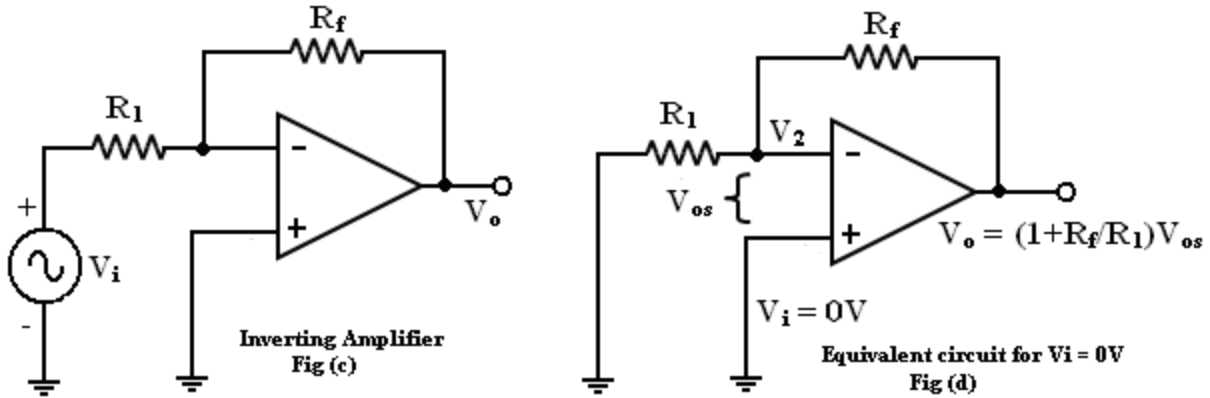
Let us determine the V_{os} on the output of inverting and non-inverting amplifier. If $V_i = 0$ (Fig (b) and (c)) become the same as in figure (d). The voltage V_2 at the negative input terminal is given by

$$V_2 = \left[\frac{R_1}{R_1 + R_f}\right] V_o \qquad \qquad (20) \qquad \text{(or)}$$

$$V_o = \left[\frac{R_1 + R_f}{R_1}\right] V_2 = \left[1 + \frac{R_f}{R_1}\right] V_2 \qquad (21)$$

Since, $\qquad V_{os} = V_i @ V_2 \quad \& \quad V_i = 0$

$$V_{os} = 0 @ V_2 = V_2 \qquad (22) \; or$$

$$V_o = \left[1 + \frac{R_f}{R_1}\right] V_{os} \qquad (23)$$

Thus, the output offset voltage of an op-amp in closed loop is given by equation (23).

Total output offset voltage:

The total output offset voltage V_{OT} could be either more or less than the offset voltage produced at the output due to input bias current (I_B) or input offset voltage alone(V_{os}).

This is because I_B and V_{os} could be either positive or negative with respect to ground. Therefore the maximum offset voltage at the output of an inverting and non-inverting amplifier (figure b, c) without any compensation technique used is given by many op-amp provide offset compensation pins to nullify the offset voltage.

> ➢ 10K potentiometer is placed across offset null pins 1&5. The wipes connected to the negative supply at pin 4.
> ➢ The position of the wipes is adjusted to nullify the offset voltage.
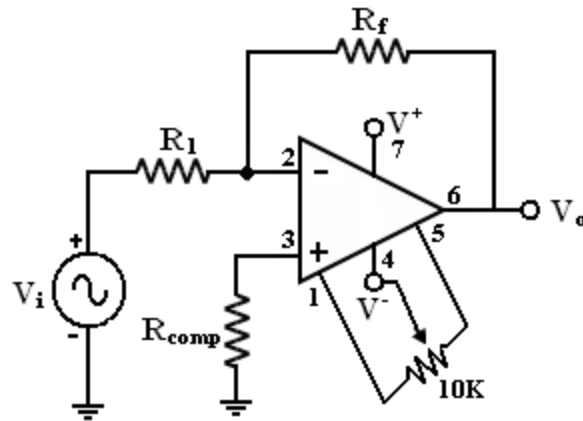
When the given (below) op-amps does not have these offset null pins, external balancing techniques are used.

$$V_{OT} = \left[1 + \frac{R}{R_1} \right] V_{os} + R_f I_B \quad \text{— 24a}$$

With R_{comp}, the total output offset voltage

$$V_{OT} = \left[1 + \frac{R}{R_1} \right] V_{os} + R_f I_{os} \quad \text{— 25a}$$

Balancing circuit:
Inverting amplifier:

$$V_{os} = \pm \frac{VR_4}{R_3 + R_4}$$

Non-inverting amplifier:

$$V_{os} = \pm \frac{VR_4}{R_3 + R_4}$$
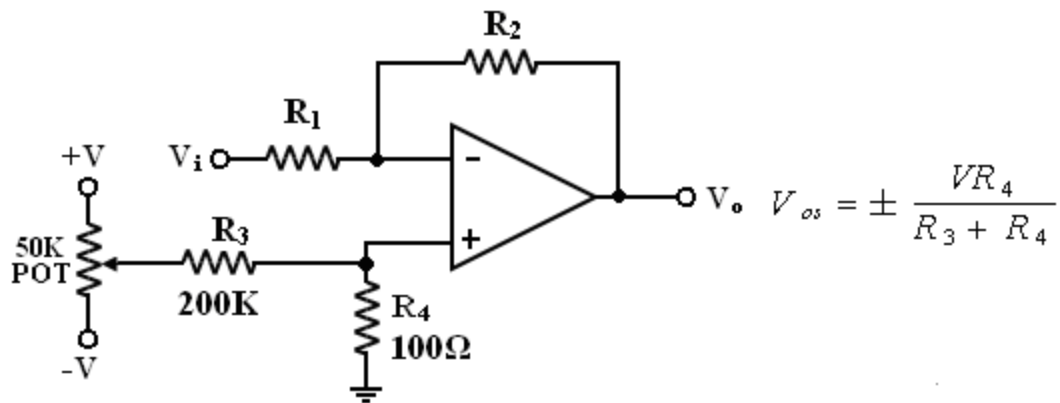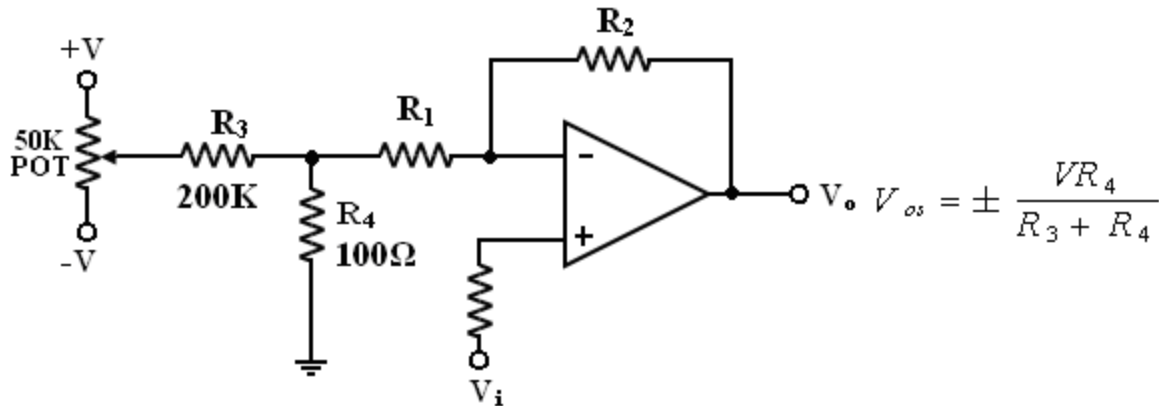
Thermal drift:

➢ Bias current, offset current, and offset voltage change with temperature.

➢ A circuit carefully nulled at 25ºC may not remain. So when the temperature rises to 35ºC. This is called drift.

➢ Offset current drift is expressed in nA/ºC.

➢ These indicate the change in offset for each degree Celsius change in temperature.

Open – loop op-amp Configuration:

The term open-loop indicates that no feedback in any form is fed to the input from the output. When connected in open – loop, the op-amp functions as a very high gain amplifier. There are three open – loop configurations of op-amp namely,

1. differential amplifier
2. Inverting amplifier
3. Non-inverting amplifier

The above classification is made based on the number of inputs used and the terminal to which the input is applied. The op-amp amplifies both ac and dc input signals. Thus, the input signals can be either ac or dc voltage.

Open – loop Differential Amplifier:

In this configuration, the inputs are applied to both the inverting and the non-inverting input terminals of the op-amp and it amplifies the difference between the two input voltages. Figure shows the open-loop differential amplifier configuration.

The input voltages are represented by V_{i1} and V_{i2}. The source resistance R_{i1} and R_{i2} are negligibly small in comparison with the very high input resistance offered by the op-amp, and thus

the voltage drop across these source resistances is assumed to be zero. The output voltage V_0 is given by

$$V_0 = A(V_{i1} - V_{i2})$$

where A is the large signal voltage gain. Thus the output voltage is equal to the voltage gain A times the difference between the two input voltages. This is the reason why this configuration is called a differential amplifier. In open – loop configurations, the large signal voltage gain A is also called open-loop gain A.
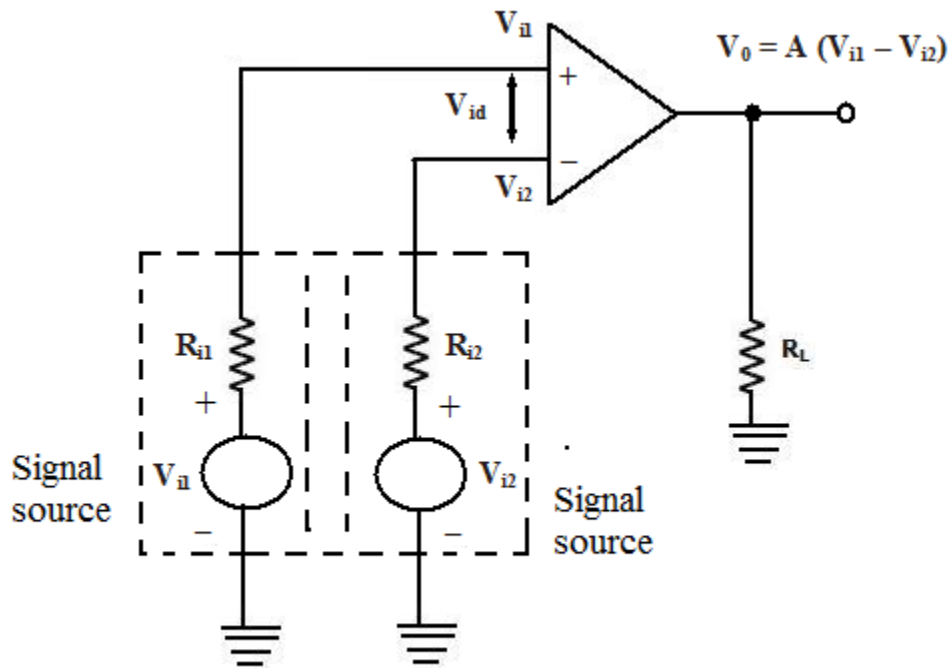
Open - loop Differential Amplifier

Inverting amplifier:

$V_0 = -AV_i$
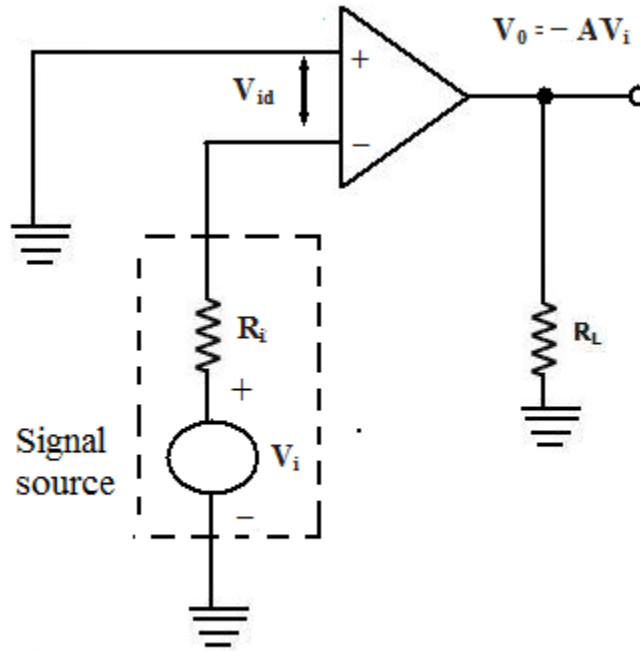
Open - loop Inverting Amplifier

In this configuration the input signal is applied to the inverting input terminal of the op-amp and the non-inverting input terminal is connected to the ground. Figure shows the circuit of an open – loop inverting amplifier.

The output voltage is 180^0 out of phase with respect to the input and hence, the output voltage V_0 is given by,

$V_0 = -AV_i$

Thus, in an inverting amplifier, the input signal is amplified by the open-loop gain A and in phase – shifted by 180^0.

Non-inverting Amplifier:

Open - loop Non - Inverting
Amplifier

$V_0 = AV_i$
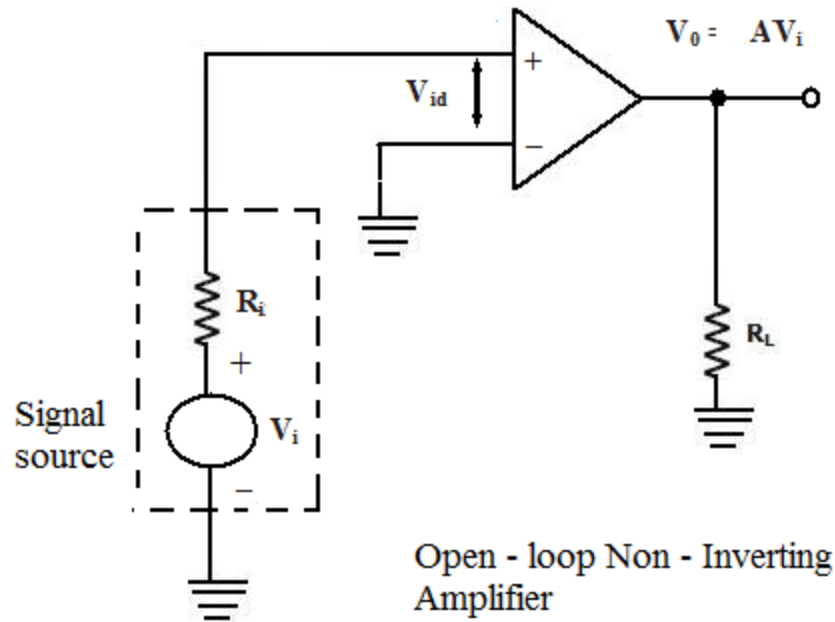
Figure shows the open – loop non- inverting amplifier. The input signal is applied to the non-inverting input terminal of the op-amp and the inverting input terminal is connected to the ground.

The input signal is amplified by the open – loop gain A and the output is in-phase with input signal.

$V_0 = AV_i$

In all the above open-loop configurations, only very small values of input voltages can be applied. Even for voltages levels slightly greater than zero, the output is driven into saturation, which is observed from the ideal transfer characteristics of op-amp shown in figure. Thus, when operated in the open-loop configuration, the output of the op-amp is either in negative or positive saturation, or switches between positive and negative saturation levels. This prevents the use of open – loop configuration of op-amps in linear applications.

Limitations of Open – loop Op – amp configuration:

Firstly, in the open – loop configurations, clipping of the output waveform can occur when the output voltage exceeds the saturation level of op-amp. This is due to the very high open – loop gain of the op-amp. This feature actually makes it possible to amplify very low frequency signal of the order of microvolt or even less, and the amplification can be achieved accurately without any

distortion. However, signals of such magnitudes are susceptible to noise and the amplification for those application is almost impossible to obtain in the laboratory.

Secondly, the open – loop gain of the op – amp is not a constant and it varies with changing temperature and variations in power supply. Also, the bandwidth of most of the open- loop op amps is negligibly small. This makes the open – loop configuration of op-amp unsuitable for ac applications. The open – loop bandwidth of the widely used 741 IC is approximately 5Hz. But in almost all ac applications, the bandwidth requirement is much larger than this.

For the reason stated, the open – loop op-amp is generally not used in linear applications. However, the open – loop op amp configurations find use in certain non – linear applications such as comparators, square wave generators and astable multivibrators.

Closed – loop op-amp configuration:

The op-amp can be effectively utilized in linear applications by providing a feedback from the output to the input, either directly or through another network. If the signal feedback is out- of-phase by 180^0 with respect to the input, then the feedback is referred to as negative feedback or degenerative feedback. Conversely, if the feedback signal is in phase with that at the input, then the feedback is referred to as positive feedback or regenerative feedback.

An op – amp that uses feedback is called a closed – loop amplifier. The most commonly used closed – loop amplifier configurations are 1. Inverting amplifier (Voltage shunt amplifier) 2. Non-Inverting amplifier (Voltage – series Amplifier)

Inverting Amplifier:

The inverting amplifier is shown in figure and its alternate circuit arrangement is shown in figure, with the circuit redrawn in a different way to illustrate how the voltage shunt feedback is achieved. The input signal drives the inverting input of the op – amp through resistor R_1.

The op – amp has an open – loop gain of A, so that the output signal is much larger than the error voltage. Because of the phase inversion, the output signal is 180^0 out – of – phase with the input signal. This means that the feedback signal opposes the input signal and the feedback is negative or degenerative.

Virtual Ground:

A virtual ground is a ground which acts like a ground . It may not have physical connection to ground. This property of an ideal op – amp indicates that the inverting and non – inverting terminals of the op –amp are at the same potential. The non – inverting input is grounded for the inverting amplifier circuit. This means that the inverting input of the op –amp is also at ground potential. Therefore, a virtual ground is a point that is at the fixed ground potential (0V), though it is not practically connected to the actual ground or common terminal of the circuit.

The open – loop gain of an op – amp is extremely high, typically 200,000 for a 741. For ex, when the output voltage is 10V, the input differential voltage V_{id} is given by

$$V_{id} = \frac{V_{out}}{A} = \frac{10}{200,000} = 0.05mV$$

Further more, the open – loop input impedance of a 741 is around 2MΩ. Therefore, for an input differential voltage of 0.05mV, the input current is only

$$I_i = \frac{V_{id}}{R_i} = \frac{0.05mV}{2M\Omega} = 0.25nA$$

Since the input current is so small compared to all other signal currents, it can be approximated as zero. For any input voltage applied at the inverting input, the input differential voltage V_{id} is negligibly small and the input current is ideally zero. Hence, the inverting input acts as a virtual ground. The term virtual ground signifies a point whose voltage with respect to ground is zero, and yet no current can flow into it.
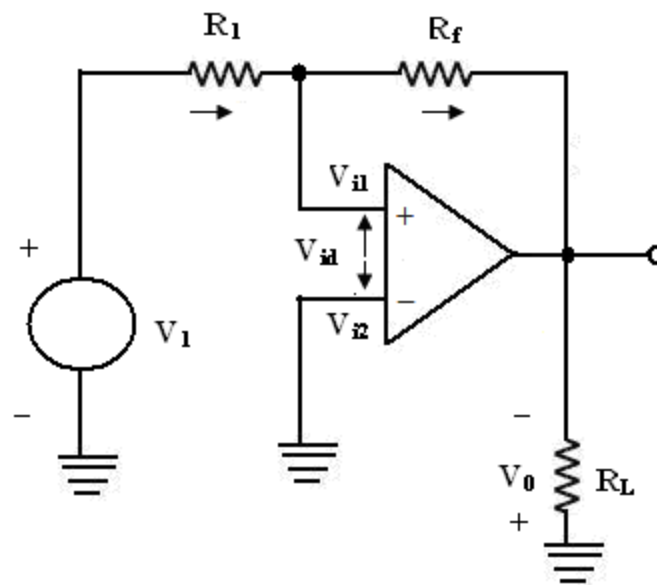
The expression for the closed – loop voltage gain of an inverting amplifier can be obtained from figure. Since the inverting input is at virtual ground, the input impedance is the resistance between the inverting input terminal and the ground. That is, $Z_i = R_1$. Therefore, all of the input voltage appears across R_1 and it sets up a current through R_1 that

equals $I_1 = \dfrac{V_i}{R_1}$. The current must flow through R_f because the virtual ground accepts negligible current. The left end of R_f is ideally grounded, and hence the output voltage appears wholly across it. Therefore, $V_0 = @I_2 R_f = @\dfrac{R_f}{R_1}V_i$. The closed –loop voltage gain A_V is given by

$$A_v = \dfrac{V_0}{V_i} = @\dfrac{R_f}{R_1} .$$

The input impedance can be set by selecting the input resistor R_1 . Moreover, the above equation shows that the gain of the inverting amplifier is set by selecting a ratio of feedback resistor R_f to the input resistor R_1 . The ratio R_f/R_1 can be set to any value less than or greater than unity. This feature of the gain equation makes the inverting amplifier with feedback very popular and it lends this configuration to a majority of applications.

Practical Considerations:

1. Setting the input impedance R_1 to be too high will pose problems for the bias current, and it is usually restricted to 10KΩ.
2. The gain cannot be set very high due to the upper limit set by the fain – bandwidth (GBW = $A_v * f$) product. The A_v is normally below 100.
3. The peak output of the op – amp is limited by the power supply voltages, and it is about 2V less than supply, beyond which, the op – amp enters into saturation.
4. The output current may not be short – circuit limited, and heavy loads may damage the op – amp. When short – circuit protection is provided, a heavy load may drastically distort the output voltage.

Practical Inverting amplifier:

The practical inverting amplifier has finite value of input resistance and input current, its open voltage gain A_0 is less than infinity and its output resistance R_0 is not zero, as against the ideal inverting amplifier with finite input resistance, infinite open – loop voltage gain and zero output resistance respectively.

Figure shows the low frequency equivalent circuit model of a practical inverting amplifier. This circuit can be simplified using the Thevenin's equivalent circuit shown in figure. The signal source

Vi and the resistors R_1 and R_i are replaced by their Thevenin's equivalent values. The closed – loop gain A_V and the input impedance R_{if} are calculated as follows.

The input impedance of the op- amp is normally much larger than the input resistance R_1. Therefore, we can assume $V_{eq} \approx V_i$ and $R_{eq} \approx R_1$. From the figure we get,

$$V_0 = IR_0 + AV_{id}$$
$$and\ V_{id} + IR_f + V_0 = 0$$

Substituting the value of V_{id} from above eqn, we get,

$$V_0\ 1 + A = I\ R_0 @ AR_f$$
$$\overset{a}{}\ \overset{b}{}\ \overset{c}{}$$

Also using the KVL, we get

$$V_i = I\ R_1 + R_f\ + V_0$$
$$\overset{b}{}\ \overset{c}{}$$

Substituting the value of I derived from above eqn and obtaining the closed loop gain A_v, we get

$$A_v = \frac{V_{out}}{V_i} = \frac{R_0 @ AR_f}{R_0 + R_f + R_1\ 1 + A}$$

It can be observed from above eqn that when $A \gg 1$, R_0 is negligibly small and the product $AR_1 \gg R_0 + R_f$, the closed loop gain is given by

$$A_v = @ \frac{R_f}{R_1}$$

Which is as the same form as given in above eqn for an ideal inverter.
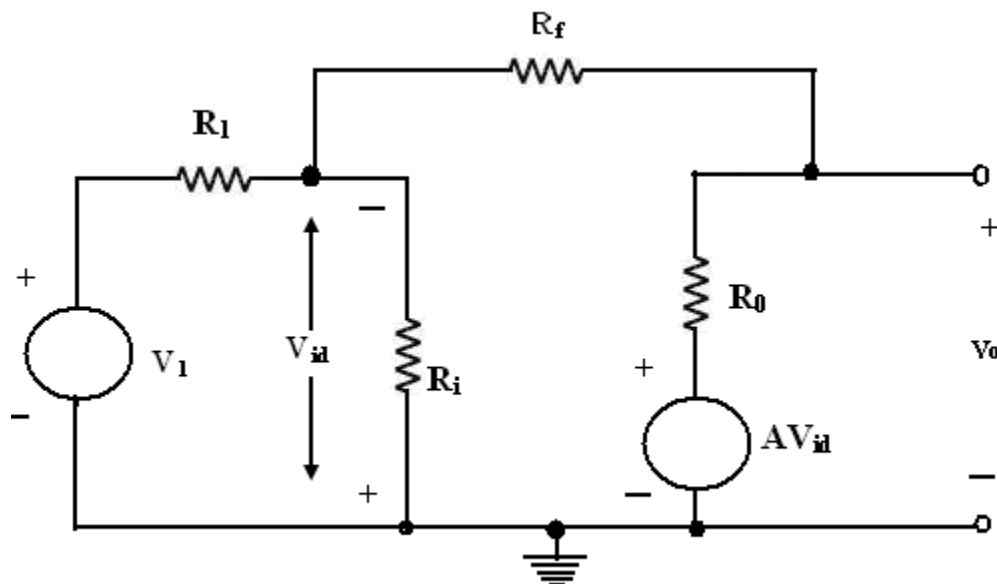
Equivalent Circuit of a Practical Inerting Amplifier

Input Resistance:

From figure we get,

$$R_{if} = \frac{V_{id}}{I_1}$$

Using KVL, we get,

$$V_{id} + I_1 R_f + R_0 + AV_{id} = 0$$

which can be simplified for R_{if} as

$$R_{if} = \frac{V_{id}}{I_1} = \frac{R_0 + R_f}{1 + A}$$

Thevenin's Equivalent Circuit
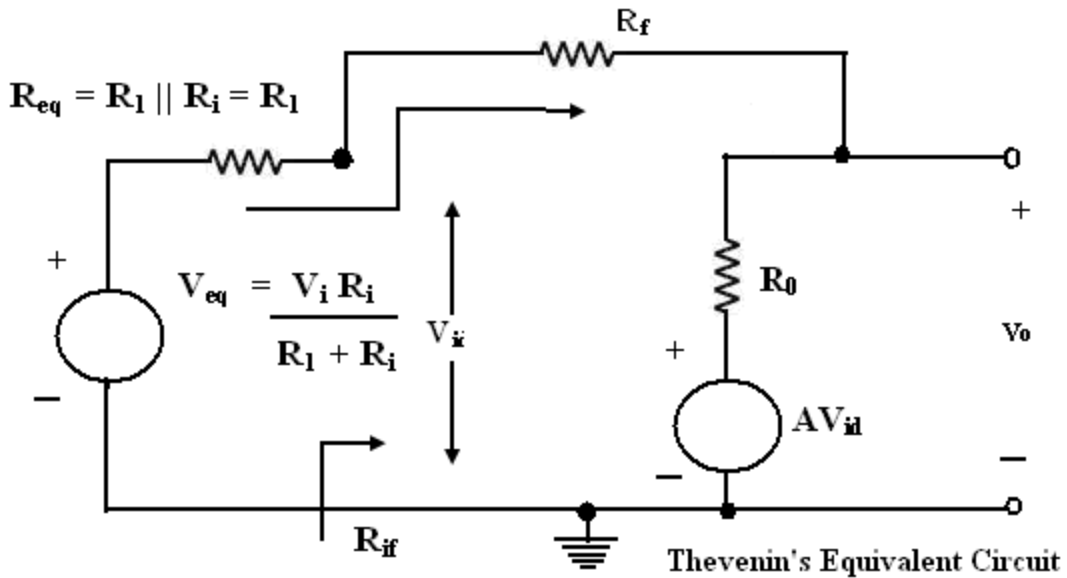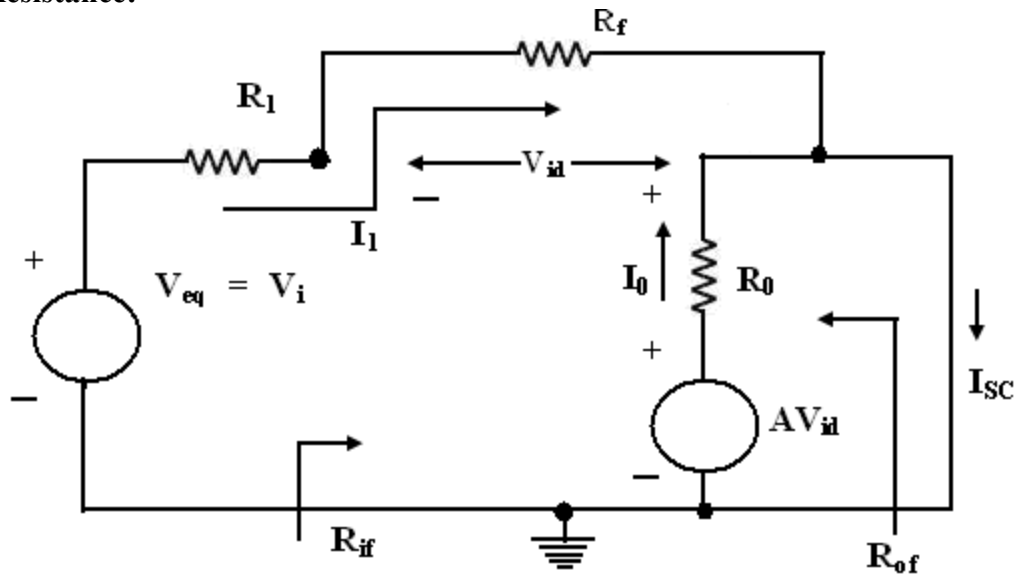
Output Resistance:

Equivalent circuit to determine Rof

Figure shows the equivalent circuit to determine R_{of}. The output impedance R_{of} without the load resistance factor R_L is calculated from the open circuit output voltage V_{oc} and the short circuit output current I_{SC}. From the figure, when the output is short circuited, we get

$$I_1 = \frac{V_i - @V_{id}}{R_1 + R_f}$$

$$and\ I_0 = \frac{AV_{id}}{R_0}$$

$$we\ know\ that\ V_{id} = @I_1 R_f$$

$$Therefore,\ I_0 = @\frac{AI_1 R_f}{R_0}$$

The short circuit current is

$$I_{SC} = I_1 + I_0 = V_i \left[\frac{R_0 @ AR_f}{R_0}\frac{1}{R_1 + R_f} \right]$$

The output resistance $R_{of} = \dfrac{V_{oc}}{I_{sc}}$ and the closed open loop gain $A_v = \dfrac{V_{oc}}{V_i}$

Therefore,

$$R_{of} = \frac{A_v V_i}{V_i \left[\dfrac{R_0 @ AR_f}{R_0}\dfrac{1}{R_1 + R_f} \right]}$$

Substituting the value of A_v from above eqn, we get

$$R_{of} = \frac{R_0}{R_0 + R_f + R_1}\frac{R_1 + R_f}{1 + A}$$

$$= \frac{\dfrac{R_0}{R_0 + R_1 + R_f}\dfrac{R_1 + R_f}{}}{1 + \dfrac{A}{R_0 + R_1 + R_f}}$$

In the above equation, the numerator contains the term $R_0 \| (R_1 + R_f)$ and it is smaller than R_0. The output resistance R_{of} is therefore always smaller than R_0 and from above eqn for $A_v \to \infty$, the output resistance $R_{of} \to 0$.

Non –Inverting Amplifier:

The non – inverting Amplifier with negative feedback is shown in figure. The input signal drives the non – inverting input of op-amp. The op-amp provides an internal gain A. The external resistors R_1 and R_f form the feedback voltage divider circuit with an attenuation factor of β. Since the feedback voltage is at the inverting input, it opposes the input voltage at the non – inverting input terminals, and hence the feedback is negative or degenerative.

The differential voltage V_{id} at the input of the op-amp is zero, because node a is at the same voltage as that of the non- inverting input terminal. As shown in figure, R_f and R_1 form a potential divider. Therefore,

$$V_i = \frac{R_1}{R_1 + R_f} \beta V_0$$

Since no current flows into the op-amp.

Eqn can be written as $\dfrac{V_0}{V_i} = \dfrac{R_1 + R_f}{R_f} = 1 + \dfrac{R_f}{R_1}$

Hence, the voltage gain for the non – inverting amplifier is given by

$$A_V = \frac{V_0}{V_i} = 1 + \frac{R_f}{R_1}$$

Using the alternate circuit arrangement shown in figure, the feedback factor of the feedback voltage divider network is $\beta = \dfrac{R_1}{R_1 + R_f}$

Therefore, the closed loop – gain is

$$A_v = \frac{1}{\beta} = \frac{R_1 + R_f}{R_1}$$
$$= 1 + \frac{R_f}{R_1}$$

From the above eqn, it can be observed that the closed – loop gain is always greater than one and it depends on the ratio of the feedback resistors. If precision resistors are used in the feedback network, a precise value of closed – loop gain can be achieved. The closed – loop gain does not drift with temperature changes or op – amp replacements.
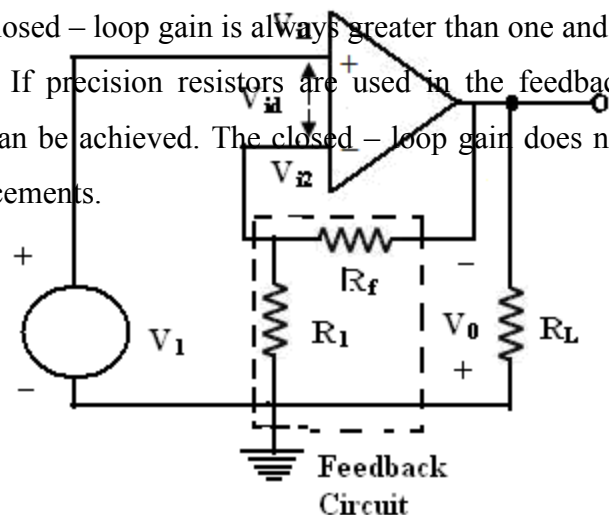
Its alternate Circuit Arrangement
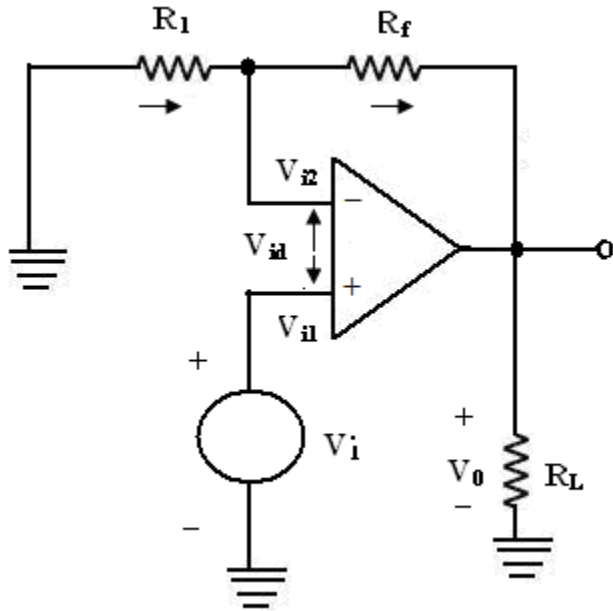
Closed Loop Non – Inverting Amplifier

The input resistance of the op – amp is extremely large (approximately infinity,) since the op – amp draws negligible current from the input signal.

Practical Non –inverting amplifier:

The equivalent circuit of a non- inverting amplifier using the low frequency model is shown below in figure. Using Kirchoff's current law at node a,

$$\tilde{V}_i @ V_{id} \tilde{Y}_1 + V_{id} Y_i + \tilde{V}_i @ V_{id} @ V_0 \tilde{Y}_f = 0$$

That is,

$$@ \overset{b}{Y_1} @ Y_i + Y_f \overset{c}{V_{id}} + \overset{b}{Y_1} + Y_f \overset{c}{V_i} = Y_f V_0$$

Similarly KCL at the output node gives,

$$\overset{b}{V_i} @ V_{id} @ V_0 \overset{c}{Y_f} + \overset{b}{AV_{is}} @ V_0 \overset{c}{Y_0} = 0$$

That gives $@ \overset{b}{Y_f} @ AY_0 \overset{c}{V_{id}} + Y_f V_i = \overset{b}{Y_f} + \overset{c}{Y_0} V_0$

Using this eqn for $\dfrac{V_{0}}{V_i}$ *we get*

$$A_v = \frac{V_0}{V_i} = \frac{\overset{b}{AY \ Y + Y} \overset{c}{@Y \ Y}}{A + 1 \overset{a}{Y_0} Y_f + \overset{b}{Y_1 @ Y_i} \overset{c}{Y_f + Y_0}}$$

when the open @loop gain A approaches infinity, the eqn becomes

$$A_v = \frac{\overset{b}{AY \ Y + Y}}{AY_0 Y_f} = \frac{Y + Y}{Y_f} = 1 + \frac{Y}{Y_f}$$
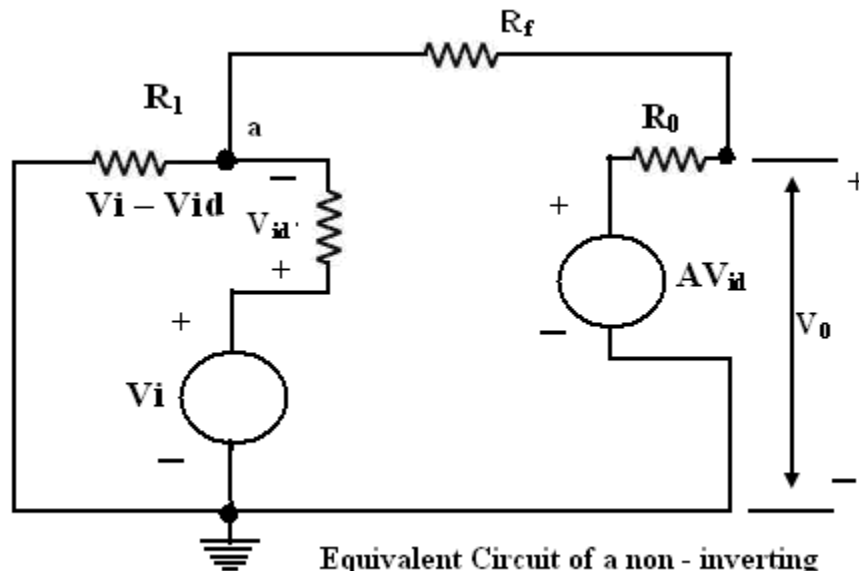
Equivalent Circuit of a non - inverting Amplifier using low frequency

Feedback amplifier:

An op-amp that was feedback is called as feedback amplifier. A feedback amplifier is sometimes referred to as closed loop amplifier because the feedback forms a closed loop between the input and output. A closed loop amplifier can be represented by using 2 blocks.

1. One for an op-amp
2. another for an feedback circuit.

There are 4 ways to connect these 2 blocks according to whether volt or current.

1. Voltage Series Feedback
2. Voltage Shunt feedback
3. Current Series Feedback
4. Current shunt Feedback

Voltage series and voltage shunt are important because they are most commonly used.
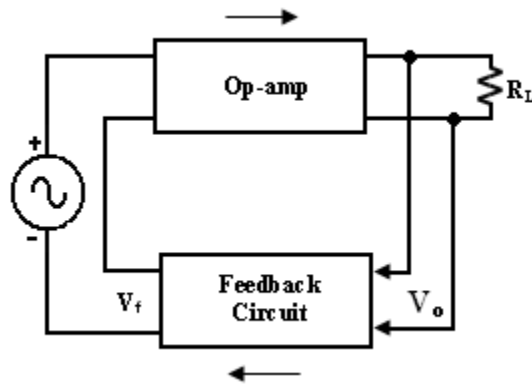
Voltage Series Feedback Amplifier
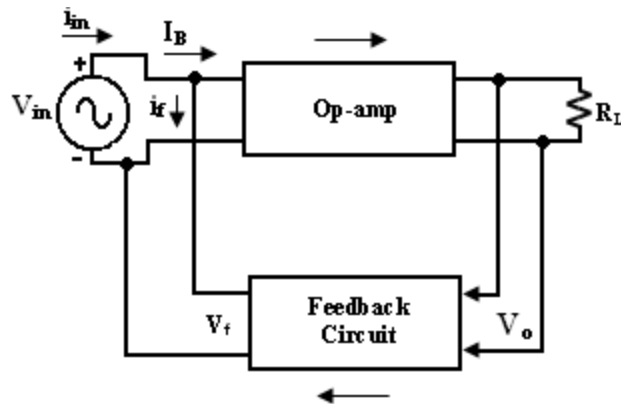
Voltage shunt feedback Amplifier

Voltage Series Feedback Amplifier:
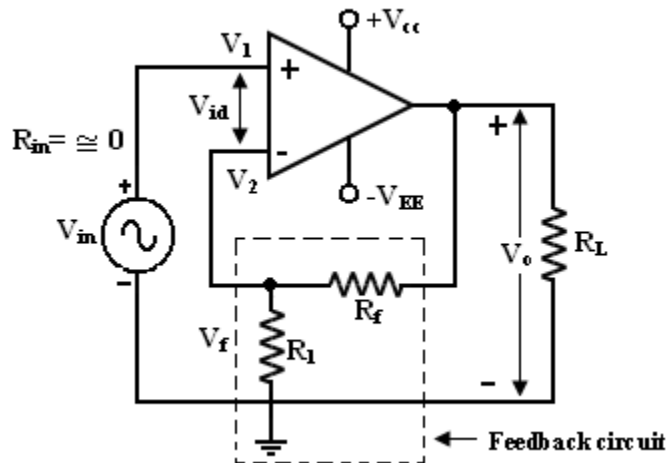
Before Proceeding, it is necessary to define some terms.

Voltage gain of the op-amp with a without feedback:

Gain of the feedback circuit are defined as open loop volt gain (or gain without feedback) $A = V_0 / V_{id}$

Closed loop volt gain (or gain with feedback) $A_F = V_0 / V_{in}$

Gain of the feedback circuit => $B = V_F / V_0$.

1. Negative feedback:

   KVL equation for the input loop is,

$Vid = Vin - V_f$ -----(1)

Vin = input voltage.

V_f= feedback voltage.

Vid = difference input voltage.

The difference volt is equal to the input volt minus the f/b volt. (or) The feedback volt always opposes the input volt (or out of phase by 180^0 with respect to the input voltage) hence the feedback is said to be negative.

It will be performed by computing

 1. Closed loop volt gain
 2. Input and output resistance

3. Bandwidth

1. Closed loop volt gain:

        The closed loop volt gain is $A_F = V_0/Vin$

$V_0 = Avid = A(V_1 - V_2)$
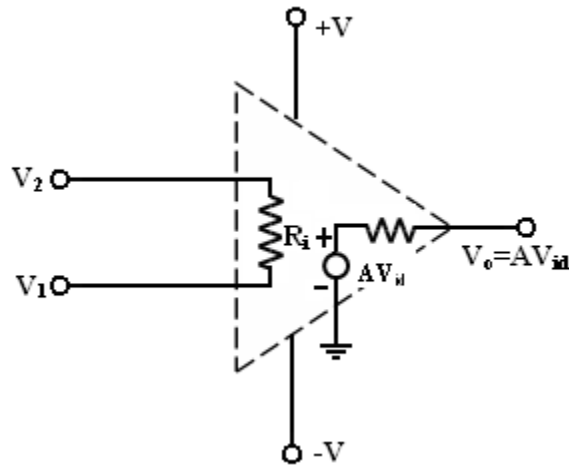
A = large signal voltage gain.

From the above eqn, $V_0 = A(V_1 - V_2)$

Refer fig, we see that, $V_1 = Vin$

$V_2 = V_f = R_1 V_0$

        $R_1 + R_f$ Since $Ri \gg R_1$

$V_0 = AVin -$ $R_1 V_0$

        $R_1 + R_f$

$V_0 +$ A $R_1 V_0$ = AVin

$$R_1 + R_f$$

Rearranging, we get,

$$\frac{V_0}{V_{in}} = \frac{A}{1 + \frac{AR_1}{R_1 + R_F}} = \frac{A(R_1 + R_F)}{R_1 + R_F + AR_1}$$

$$V_0 = \frac{A(R_1 + R_F)V_{in}}{R_1 + R_F + AR_1}$$

Thus

$$A_F = \frac{V_0}{V_{in}} = \frac{A(R_1 + R_F)}{R_1 + R_F + AR_1} \qquad @@@ \ (2)$$

Generally, A is large typically 10^5,

$$AR_1 >> R_1 + R_F \quad and \quad R_1 + R_F + AR_1 \approx AR_1$$

Thus $A_F = \dfrac{V_0}{V_{in}} = 1 + \dfrac{R_F}{R_1}$ *Ideal* $@@@@ \ (3)$

The gain of the feedback circuit B *is the ratio of* V_F *and* V_0,

$$B = \frac{V_F}{V_0} \qquad @@@ \ (4)$$

$$B = \frac{R_1}{R_1 + R_F}$$

Compare eqn 3 and 4 we can conclude

$$A_F = \frac{1}{B} \quad ideal \qquad @@@ \ (5)$$

This means that gain of the feedback circuit in the reciprocal of the closed loop volt gain A_F

In other words for given R_1 and R_F the values of A_F and B are fixed. Eqn (5) is an alternative to eqn (3)

Finally, the closed loop voltage gain A_F can be expressed in terms of open loop gain A and feedback circuit gain B as follows,

From eqn (2),

$$A_F = \frac{V_{out}}{V_{in}} = \frac{A\,R + R}{R_1 + R_F + AR_1}$$

Rearranging the Eqn A

$$A_F = \frac{A\,\dfrac{R + R}{\ }}{\dfrac{R + R}{R_1 + R_F} + \dfrac{AR}{R_1 + R_F}}$$

$$using\ eqn\ 4^a\ B = \frac{V}{V_0} = \frac{R}{R_1 + R_F}$$

$$A_F = \frac{A}{1 + AB}\ @@@\ 6^a$$

where A_F = closed loop voltage gain

A = open loop voltage gain

B = Gain of the circuit

AB = loop gain

3. Difference input voltage ideally zero (Vid)

Reconsider eqn $V_0 = A\ Vid$

$Vid = V_0/A$

Since A is very large (ideally α)

$Vid \cong 0$ ---(7.a)

(i.e) $V_1 \cong V_2$ --(7.b)

Eqn (7.b) says that the volt at the Non-inverting input terminal of an op-amp is approximately equal to that at the inverting input terminal provided that A, is vey large.

From the circuit diagram,

$V_1 = Vin$

$V_2 = V_F = R_1 V_0 / R_1 + R_F$

Sub these values of V_1 and V_2 in eqn (7.b) we get

$Vin = R_1 V_0 / R_1 + R_F$ (i.e) $A_F = V_0/Vin = 1 + R_F/R_1$

4. Input Resistance with feedback:

From the below circuit diagram Ri -> input resistance

Rif -> input resistance of an op-amp with feedback

Derivation of input resistance with Feedback:
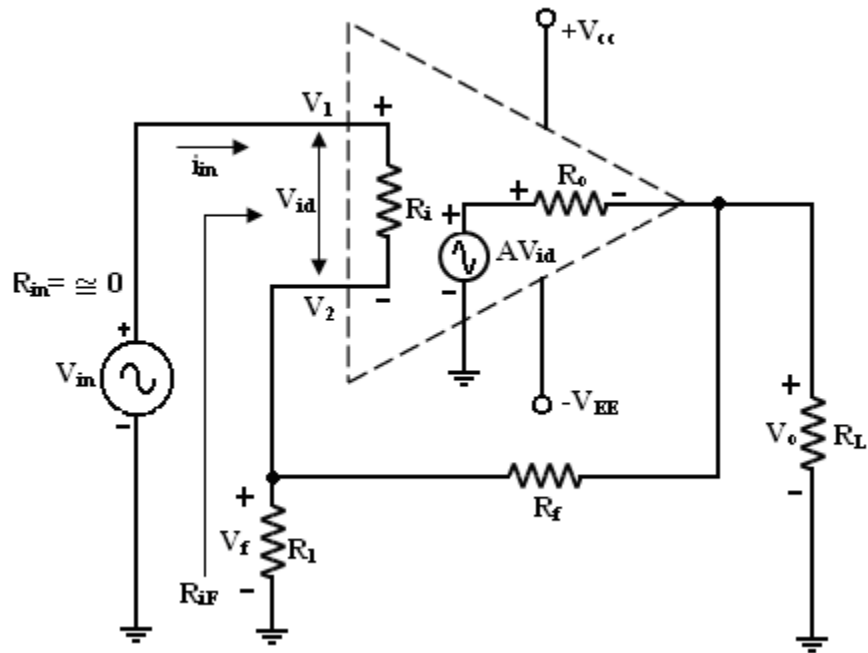
The input resistance with feedback is defined as,

$$R_{if} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{\dfrac{V_{in}}{R_i}}$$

However,

$$V_{id} = \frac{V_{in}}{A_h} \quad and \quad V_0 = \frac{1}{1+AB} V_{in}$$

$$R_{if} = R_i \frac{V_{in}}{V_{in}} R$$

$$= AR_i \frac{V_{in}}{V_{in}}$$

$$1 + AB$$

$$= AR_i \frac{V_{in}}{A} V_{in} = R_i \ \grave{}\ 1 + AB^a$$

$$R_{if} = R_i \ \grave{}\ 1 + AB^a \ @@ \ 8^a$$

This means that the input resistance of the op-amp with feedback is (i+AB) times that without feedback.

5. Output Resistance with feedback:
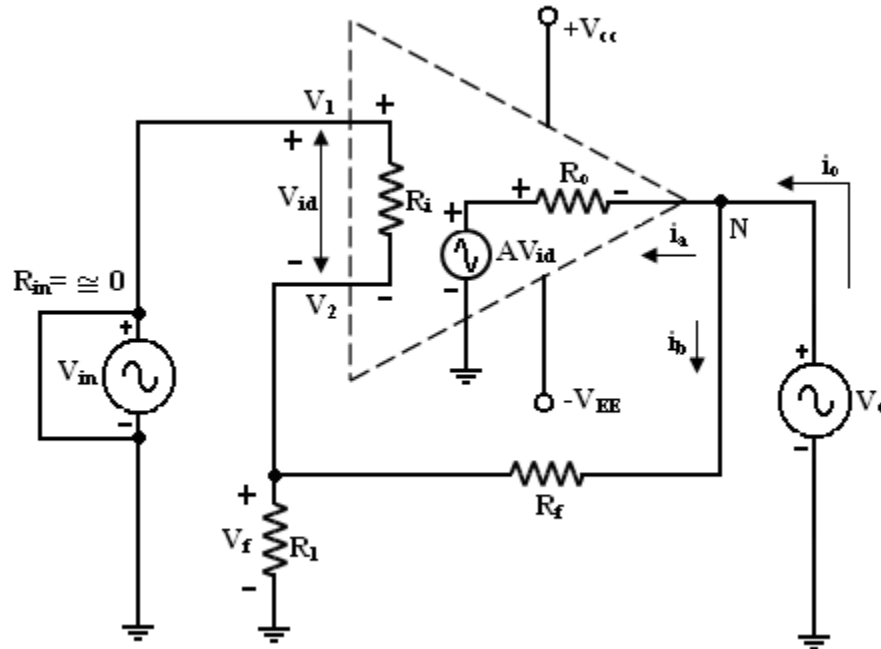
This resistance can be obtained by using Thevenin's theorem. To find out o/p resistance with feedback R_{OF} reduce independent source Vin to zero, apply an external voltage V_0, and calculate the resulting current i_0.

The R_{OF} is defined as follows,

$R_{OF} = V_0 / i_0$ ---(9.a)

KCL at o/p node 'N' we get,

$i_0 = i_a + i_b$

Since $((R_F + R_1) || R_i >> R_0$ and $i_0 >> i_b$.

$i_0 ≈ i_a$

The current i_0 can be found by writing KVL eqn for the o/p loop

$V_0 - R_0 i_0 - AVid = 0$

$i_0 = V_0 - AVid$

R_0

$Vid = V_1 - V_2$

$$= 0 - V_F$$

$$V_{id} = @\frac{R_1 V_0}{R_1 + R_F} = @BV_0$$

$$i_0 = \frac{V_0 + ABV_0}{R_0}$$

Sub the value of input is in eqn `9α^a

$$R_{OF} = \frac{V_0}{V_0 + \frac{ABV_0}{R_0}}$$

$$= R_0 \frac{V_0}{V_0 + ABV_0}$$

$$R_{OF} = \frac{R_0}{1 + AB} @@@@ `9A^a$$

This result shows that the output resistance of the voltage series feedback amplifier is 1/(1+AB) the output resistance of R_0 the op-amp. (i.e) The output resistance of the op-amp with feedback is much smaller than the output resistance without feedback.

6. Bandwidth with feedback:

The bandwidth of the amplifier is defined as the band (range of frequency) for which the gain remains constant. The Frequency at which the gain equals 1 is known as unity gain bandwidth (UGB). The relationship between the breakfrequency f_0 , open loop volt gain A, bandwidth with feedback f_F and closed loop gain A_F .

For an op-amp with a single break frequency f_0 , the gain bandwidth product is constant and equal to the unity-gain bandwidth. (UGB).

UGB = (A) (f_0) ----(10.a)

A = open loop volt gain

f_0 = break frequency of an op-amp ((or) only for a single break frequency op-amp UGB = $A_F f_F$ ----(10.b)

A_F = closed loop volt gain

f_F = bandwidth with feedback.

Equating eqn 10.a and 10.b

$Af_0 = A_F f_F$

$f_F = Af_0 / A_F$ -----(10.c)

For the non-inverting amplifier with feedback

$A_F = A/(1+AB)$

Sub the value of A_F in eqn 10.c, we get

$f_F = Af_0 / A/(1+AB)$

$f_F = (1+AB) f_0$ ----(10.d)

eqn 10.d -> bandwidth of the non-inverting amplifier with feedback is = bandwidth of the with feedback f_0 times $(1+AB)$

7. Total o/p offset voltage with feedback (Vout)

In an open loop op-amp the total o/p offset voltage is equal to either the +ve or –ve saturation volt.

Vout = +ve (or) –ve saturation volt.

With feedback the gain of the Non-inverting amplifier changes from A to $A/(1+AB)$, the total output offset voltage with feedback must also be $1/(1+AB)$ times the voltage without feedback. (i.e)

$$\text{Total o/p offset Vout with feedback} = \frac{\text{Total o/p offset volt without feedback}}{1+AB}$$

$$\text{Vout} = \frac{\pm \text{Vsat}}{1+AB} \quad ----(11)$$

$1/(1+AB)$ is < I and $\pm$Vsat = Saturation voltages. The maximum voltages the output of an op-amp can reach.

Note:

Open-loop even a very small volt at the input of an op-amps can cause to reach maximum value (+ Vsat)because of its very high volt gain. According to eqn for a gain op-amp circuit the Vout is either +ve or –ve volt because Vsat can be either +ve or –ve.

Conclusion of Non-Inverting Amplifier with feedback:

The char of the perfect volt Amplifier:

1. It has very high input resistamce.
2. Very low output resistance
3. Stable volt gain
4. large bandwidth

8. Voltage Follower: [Non-Inverting Buffer]
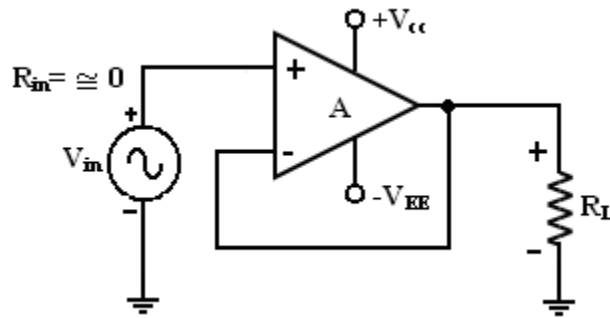
  The lowest gain that can be obtained from a non-inverting amplifier feedback is 1. When the Non-Inverting amplifier is designed for unity and it is called a voltage follower, because the output voltage is equal to and inphase with the input or in volt follower the output follows the input.

It is similar to discrete emitter follower, the volt follower is preferred, because it had much higher input resistance and output amplitude is exactly equal to input.

To obtain the voltage follower, from this circuit simply open R_1 and short R_F.

In this figure all the output volt is fed back into the inverting terminal of the op-amp.

The gain of the feedback circuit is 1 ($B = A_F = 1$)

$A_F = 1$

$R_{iF} = AR_i$

$R_{OF} = R_0/A$

$f_F = Af_0$

$Vout = \pm Vsat$

    A

Since $1 + A \, ᵗ \, A$.

Voltage Shunt Feedback Amplifier:[Inverting Amplifier]
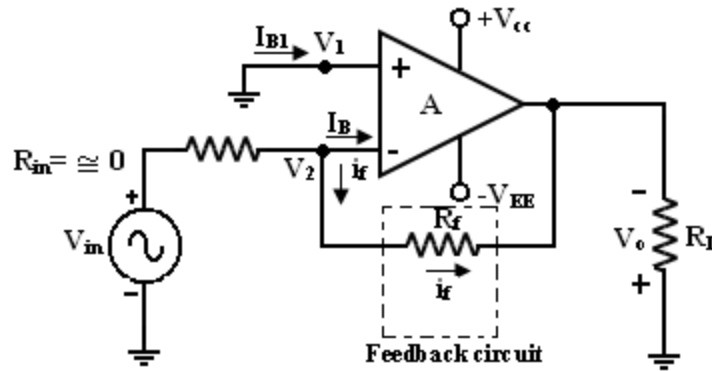
The input voltage drives the inverting terminal, and amplified as well as inverted output signal also applied to the inverting input via feedback resistor R_F.

Note:

Non-inverting terminal is grounded and feedback circuit has R_F and extra resistor R_1 is connected in series with the input signal source Vin.

We derive the formula for

1. Voltage gain
2. Input and output resistance
3. Bandwidth
4. Total output offset voltage.

1. Closed – loop voltage gain A_F :

A_F of volt shunt feedback amplifier can be obtained by writhing KCL eqn at the input node V_2.

$i_{in} = i_F + I_B$ ----(12.a)

Since R_i is very large, the input bias current is negligibly small.

$i_{in} ₵ i_F$

(i.e) $\dfrac{Vin - V_2}{R_i} = \dfrac{V_2 - V_0}{R_F}$ ----(12.b)

Consider, from eqn,

$V_1 - V_2 = - V_0/A$

Since $V_1 = 0V$

$V_2 = -V_0 /A$

Sub this value of V_2 in eqn (12.b) and rearranging,

$$\frac{Vin + V_0/A}{R_i} = \frac{-(V/A) - V_0}{R_F}$$

$$A_F = \frac{V_0}{Vin} = - \frac{AR_F}{R_1 + R_F + AR_1} \quad \text{(exact)} \quad \text{-----(13)}$$

The −ve sign indicates that the input and output signals are out of phase 180^0. (or opposite polarities).

Because of this phase inversion the diagram is known as Inverting amplifier with feedback. Since the internal gain A of the op-amp is very large (α), $AR_1 \gg R_1 + R_F$, (i.e) eqn (13)

$A_F = V_0/Vin = -R_F/R_1$ (Ideal)

To express eqn (13) in terms of eqn(6). To begin with, we divide both numerator and denominator of eqn (13) by $(R_1 + R_F)$

$$A_F = \frac{AR_F/R_1 + R_F}{1 + AR_1(R_1 + R_F)} \quad \text{---(15)}$$

$A_F = -AR/1 + AB)$

Where $K = R_F/(R_1 + R_F)$

$B = R_1/(R_1 + R_F)$ Gain of feedback.
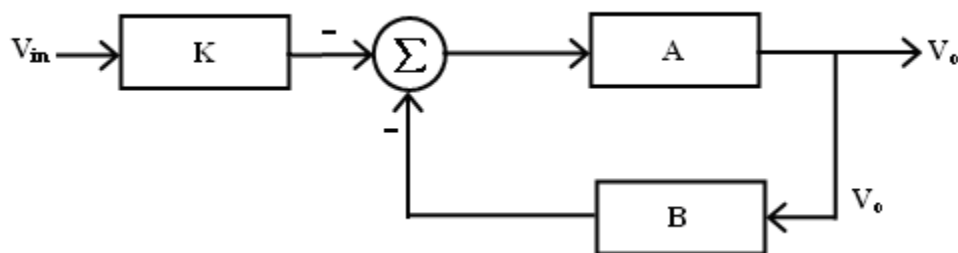
The comparison of eqn (15) with feedback (6) indicates that in addition to the phase inversion (-sign), the closed loop gain of the inverting amplifier in K times the closed loop gain of the Non-inverting amplifier where K< 1. To derive a ideal closed loop gain, we can use Eqn 15 as follows,

If AB >> 1, then (1+AB) = AB and A_F= K/B = $-R_F/R_1$ ----(16)

2. Input Resistance with feedback:

Easiest method of finding the input resistance is to millerize the feedback resistor R_F.

(i.e) Split R_F in to its 2 Miller components as shown in fig.

In this circuit, the input resistance with feedback Rif is then

Rif = R_1 + R_F

$$----- \qquad || \quad (Ri) \qquad -----(18)$$

1+A

Since Ri and A are very large.

R_1 + R_F

$$----- \qquad || \quad (R_1) \qquad \text{τ} \qquad 0Ω$$

1+A
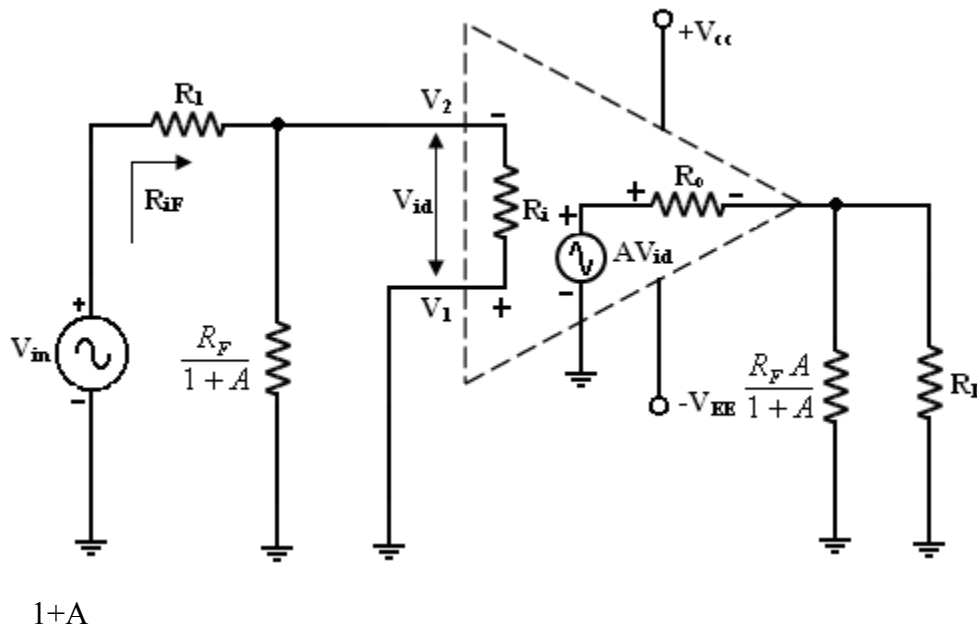
3. Output Resistance with feedback:

The output resistance with feedback R_{OF} is the resistance measured at the output terminal of the feedback amplifier. Thevenin's circuit is exactly for the same as that of Non-

inverting amplifier because the output resistance R_{OF} of the inverting amplifier must be identical to that of non – inverting amplifier.
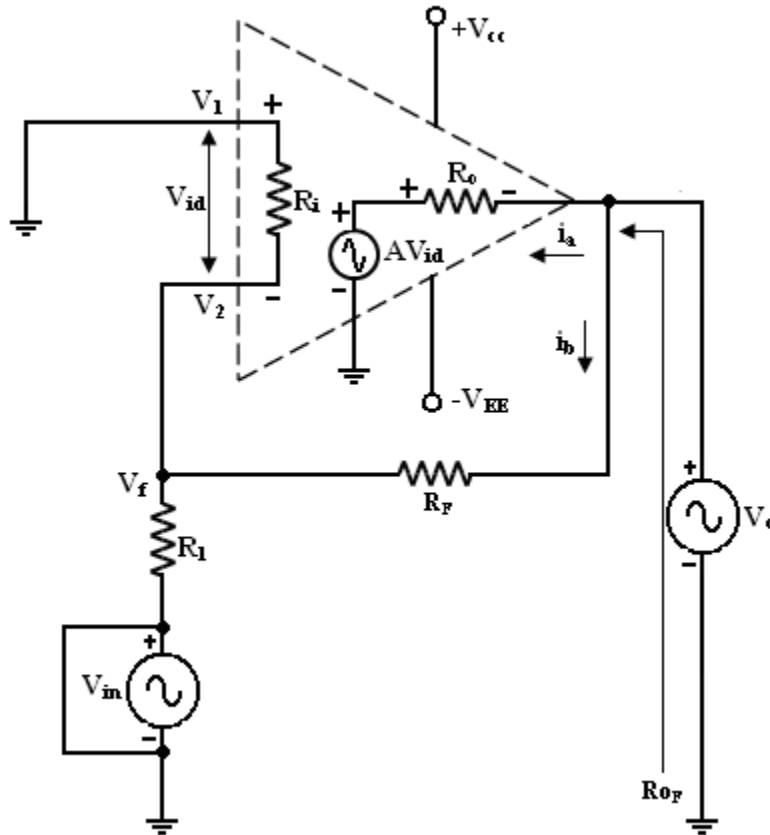
R_0 = Output Resistance of the op-amp

A = Open loop volt gain of the op-amp

B = Gain of the feedback circuit.

4. Bandwidth with Feedback:

        The gain Bandwidth product of a single break frequency op-amp is always constant.

Gain of the amplifier with feedback < gain without feedback

The bandwidth of amplifier with feedback f_F must be larger than that without feedback.

$f_F = f_0(1+AB)$ ----(21.a)

f_0 = Break frequency of the op-amp

$$\frac{\text{= unity gain Bandwidth}}{\text{Open- loop voltage gain}} = \frac{\text{UGB}}{\text{A}}$$

Sub this value of f_0 in eqn (21.a)

$$f_F = \frac{\text{UGB}}{\text{A}} (1+AB)$$

$$f_F = \frac{\text{UGB (K)}}{A_F} \quad -----(21.b)$$

Where $K = R_F /(R_1 + R_F)$; $A_F = AK/1+AB$

Eqn 10.b and 21.b => same for the bandwidth.

Same closed loop gain the closed loop bandwidth for the inverting amplifier is < that of Non – inverting amplifier by a factor of $K(<1)$

5. Total output offset voltage with feedback:

When the temp & power supply are fixed, the output offset voltage is a function of the gain of an op-amp.

Gain of the feedback < gain without feedback.

The output offset volt with feedback < without feedback.

$$\text{Total Output offset Voltage with f/b} = \frac{\text{Total output offset volt without f/b}}{1+AB}$$

$$\text{Vout} = \pm\frac{\text{Vsat}}{1+AB} \quad ----(22)$$

$\pm$Vsat = Saturation Voltage

A = open-loop volt gain of the op-amp

B = Gain of the f/b circuit

$B= R_1 /(R_1 + R_F)$

In addition, because of the –ve f/b,

1. Effect of noise

2. Variations in supply voltages

3. Changes in temperature on the output voltage of inverting amplifier are reduced.

Differential amplifier:

We will evaluate 2 different arrangements of the differential amplifier with -ve feedback. Classify these arrangements according to the number of op-amps used. i.e

1. Differential amplifier with one op-amp
2. Differential amplifier with two op-amps.

Differential amplifier are used in instrumentation and industrial applications to amplify differences between 2 input signals such as output of the wheat stone bridge circuit.

Differential amplifier preferred to these application because they are better able to reject common mode (noise) voltages than single input circuit such as inverting and non-inverting amplifier.

1. Differential Amplifier with one op-amp:
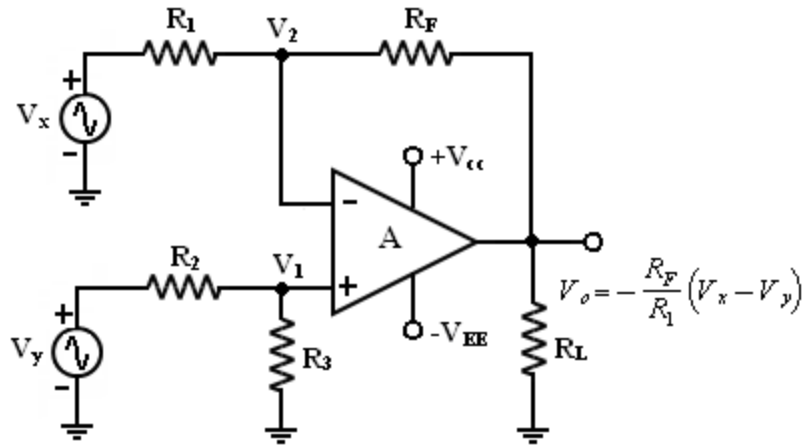
To analyse this circuit by deriving voltage gain and input resistance. This circuit is a combination of inverting and non-inverting amplifier. (i.e) When V_x is reduced to zero the circuit is non-inverting amplifier and when V_y is reduced to zero the circuit is inverting amplifier.

Voltage Gain:

The circuit has 2 inputs V_x and V_y. Use superposition theorem, when $V_y = 0V$, becomes inverting amplifier. Hence the o/p due to V_x only is

$$V_{ox} = \frac{-R_F (V_x)}{R_1} \qquad -----(24.a)$$

Similarly, when $V_x = 0V$, becomes Non-inverting amplifier having a voltage divider network composed of R_2 and R_3 at the Non – inverting input.

$$V_1 = \frac{R_3 V_y}{R_2 + R_3}$$

and the output due to V_y then is

$$V_{oy} = \left(1 + \frac{R_f}{R_1}\right) V_1$$

$$i.e. \quad V_{oy} = \frac{R_3}{R_2 + R_3} \cdot \frac{R_1 + R_F}{R_1} V_y$$

Since $R_1 = R_2$ & $R_F = R_3$,

$$V_{oy} = \frac{R_F V_y}{R_1} \quad @@@@@ \ 24\ Ab$$

From eqn 24 Aa and 24 Ab, the net ouput volt is,

$$V_o = V_{ox} + V_{oy}$$

$$V_o = @\frac{R_F}{R_1} V_x @ V_y = @\frac{R_F V_y}{R_1}$$

or the voltage gain

$$A_D = \frac{V_o}{V_{xy}} = @\frac{R_F}{R_1} \quad @@@@@@ \ 25\ a$$

Note : the gain of the differential amplifier is same as that of inverting amplifier.

Input Resistance:

The input resistance R_{if} of the differential amplifier is resistance determined looking into either one of the 2 input terminals with the other grounded,

With $V_y = 0V$,

Inverting amplifier, the input resistance which is,

RiFx ≈ R_1 -----------------(26.a)

Similarly, ,$V_x = 0V$,

Non-inverting amplifier, the input resistance which is,

RiFy ≈ $(R_2 + R_3)$ ------(26.b)

V_x and V_y are not the same. Both the input resistance can be made equal, if we modify the basic differential amplifier. Both R_1 and $(R_2 + R_3)$ can be made much larger than the source resistances. So that the loading of the signal sources does not occur.

Note: If we need a variable gain, we can use the differential amplifier. In this circuit $R_1 = R_2$, $R_F = R_3$ and the potentiometer $R_p = R_4$.

Depending on the position of the wiper in R voltage can be varied from the closed loop gain of - $2R_F /R_1$ to the open loop gain of A.

$$V_o = - \frac{2R_F}{R_1} \text{ if } R_4 = R_p$$
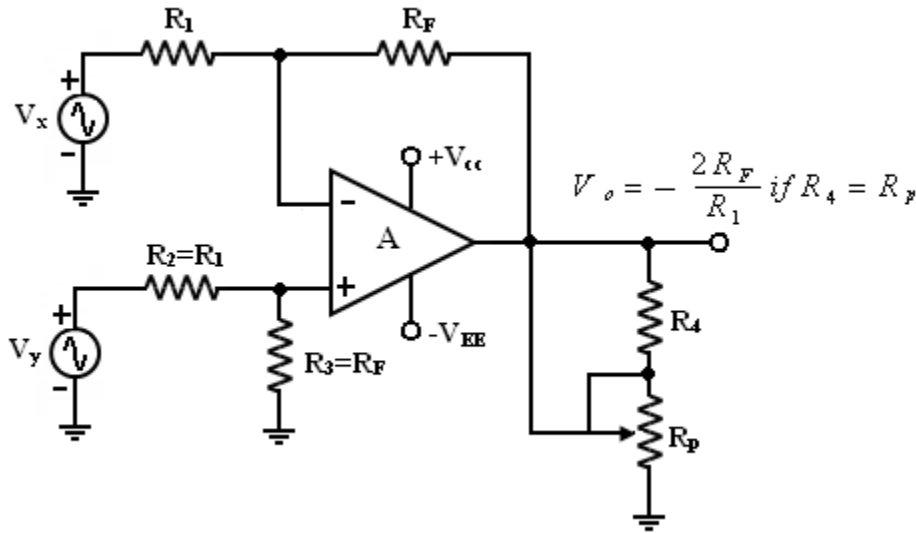
2. Differential Amplifier with 2 op-amps:

We can increase the gain of the differential amplifier and also increase the input resistance R_{if} if we use 2 op-amps.

Voltage gain:

It is compares of 2 stages 1. Non-inverting

2. Differential amplifier with gain.

$$V_o = \left(1 + \frac{R_F}{R_1}\right)$$
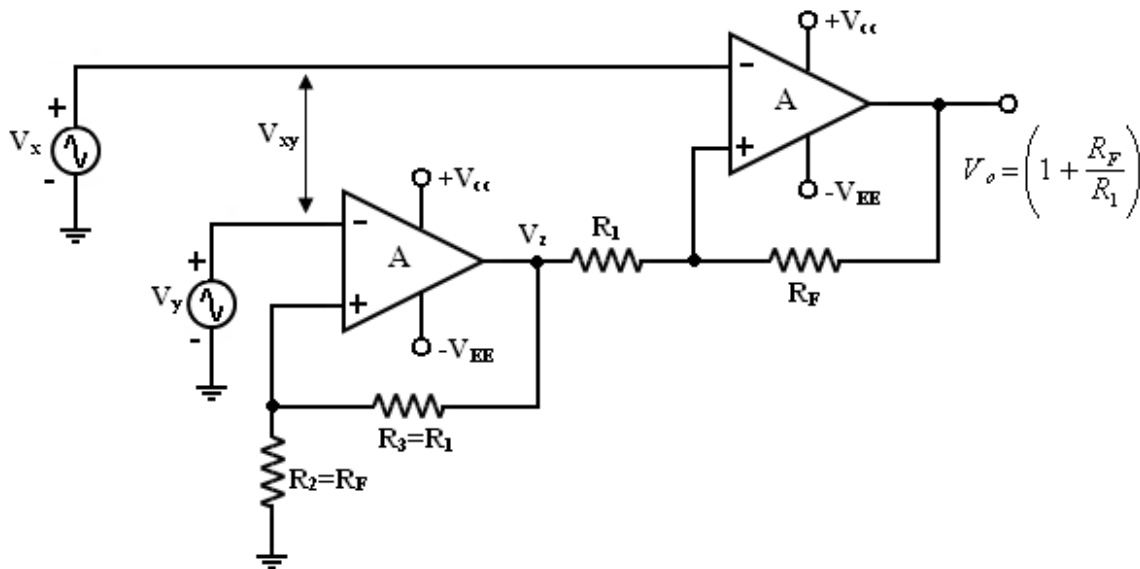
By finding the gain of these 2 stages, we can obtain the overall gain of the circuit, The o/p

$$V_2 = \left[1 + \frac{R_F}{R_2}\right] V_y \quad @@@@\ 27\ Aa$$

By applying superposition theorem to the second stage, we can obtain the output voltage,

$$V_0 = \left[-\frac{R_F V_z}{R_1} + \left[1 + \frac{R_F}{R_1}\right] V_x \right] \quad @@@@\ 27\ Ab$$

Sub the values of the V_z *from eqn* $27\ Aa$

$$V_0 = -\frac{R_F}{R_1}\left[1 + \frac{R_F}{R_2}\right] V_y + \left[1 + \frac{R_F}{F_1}\right] V_x$$

Since $R_1 = R_3$ *and* $R_F = R_2$,

$$V_0 = \left[1 + \frac{R_F}{R_1}\right] V_x @ V_y$$

$$A_D = \frac{V_0}{V_{xy}} = 1 + \frac{R_F}{R_1} \quad @@@@\ 28\ Where\ V_{xy} = V_x @ V_y$$

Input Resistance:

The input resistance Rif of the differential amplifier is the resistance determined from either one of the two non-inverting terminals with the other grounded. The first stage A_1 is the non-inverting amplifier, its input resistance is

RiFy = Ri (1+AB)   -----(29. a)

Where Ri = open loop input resistance of the op-amp.

B = $R_2 / R_2 + R_3$

Similarly, with V_y shorted to ground ($V_y = 0$ V), the 2nd stage (A_2) also becomes non-inverting amplifier, whose input resistance is

RiFx = Ri (1+AB)   -----(29. b)

Where Ri = open loop input resistance of the op-amp

B = $R_1 / (R_1 + R_F)$

Since $R_1 = R_3$ and $R_F = R_2$, the Rify $\neq$ RiFx because the loading of the input sources V_x and V_y may occur. (Or)

The output signal may be smaller in amplitude than expected. This possible reduction in the amplitude of the output signal is drawback of differential amplifier.

To overcome this:

With proper selection of components, both RiFy and RiFx can be made much larger than the sources resistance so that the loading of the input sources does not occur.

Output resistance and Bandwidth of differential amplifier with feedback:

The output resistance of the differential amplifier should be the same as that of the non-inverting amplifier expect that $B = 1/A_D$ (i.e)

$R_{OF} = R_0/(1+A/A_D)$ ----- (30)

A_D = closed loop gain of the differential amplifier

R_0 = output resistance of the op-amp

A = open – loop volt gain of the op-amp

Remember that A_D is different for differential amplifier.

In the case of Inverting and Non-inverting amplifier, the bandwidth of the differential amplifier also depends on the closed loop gain of the amplifier and is given by,

$f_F = \dfrac{\text{Unity gain Bandwidth}}{\text{closed loop gain } A_D}$ ------(31.a)

(or)

$f_F = \dfrac{(A)(f_0)}{A_D}$ ------(31.b)

Where f_0 is the open loop break frequency of op-amp.

Applications of Operational Amplifier

SIGN CHANGER (PHASE INVERTER)

I1

I1

Vi

Z1

Z2

-

+

V$_0$
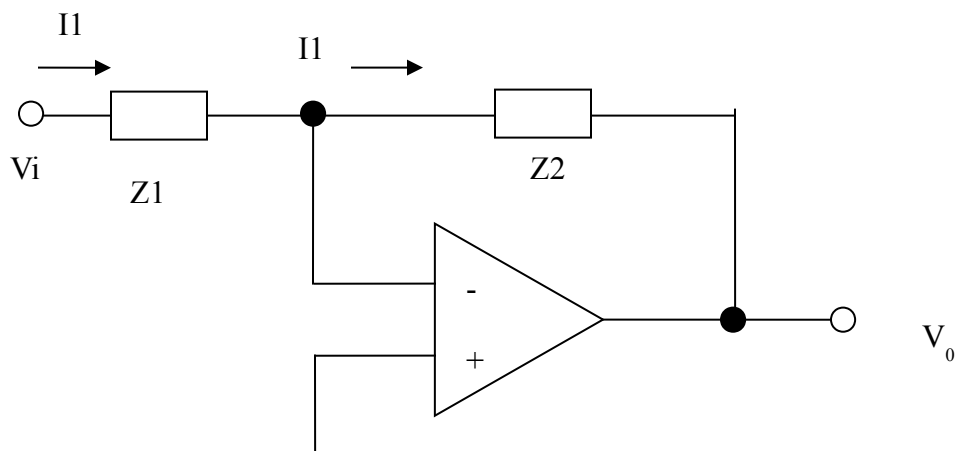
The basic inverting amplifier configuration using an op-amp with input impedance Z_1 and feedback impedance Z_f.

If the impedance Z_1 and Z_f are equal in magnitude and phase, then the closed loop voltage gain is -1,and the input signal will undergo a 180^0 phase shift at the output. Hence, such circuit is also called phase inverter. If two such amplifiers are connected in cascade, then the output from the second stage is the same as the input signal without any change of sign.

Hence, the outputs from the two stages are equal in magnitude but opposite in phase and such a system is an excellent paraphase amplifier.

Scale Changer:

Referring the above diagram, if the ratio $Z_f / Z_1 = k$, a real constant, then the closed loop gain is –k, and the input voltage is multiplied by a factor –k and the scaled output is available at the output. Usually, in such applications, Z_f and Z_1 are selected as precision resistors for obtaining precise and scaled value of input voltage.

PHASE SHIFT CIRCUITS

The phase shift circuits produce phase shifts that depend on the frequency and maintain a constant gain. These circuits are also called constant-delay filters or all-pass filters. That constant delay refers to the fact the time difference between input and output remains constant when frequency is changed over a range of operating frequencies.

This is called all-pass because normally a constant gain is maintained for all the frequencies within the operating range. The two types of circuits, for lagging phase angles and leading phase angles.

Phase-lag circuit:

Phase log circuit is constructed using an op-amp, connected in both inverting and non inverting modes. To analyze the circuit operation, it is assumed that the input voltage v1 drives a simple inverting amplifier with inverting input applied at(-)terminal of op-amp and a non inverting amplifier with a low-pass filter.

It is also assumed that inverting gain is -1 and non-inverting gain after the low-pass circuit

is $1 + \dfrac{R_f}{R_1}$ =1+1=2, Since R$_f$=R$_1$

$R_f = R_1$

Vi

R$_1$

R

C

V$_0$

Phase - Lag Circuit

$\left|\dfrac{V_0}{V_i}\right|$

1

0

-90

-180

f(log)

fo   f(log)
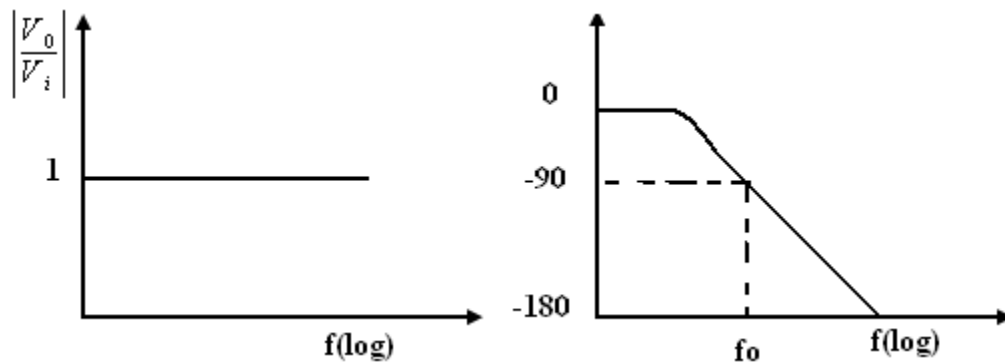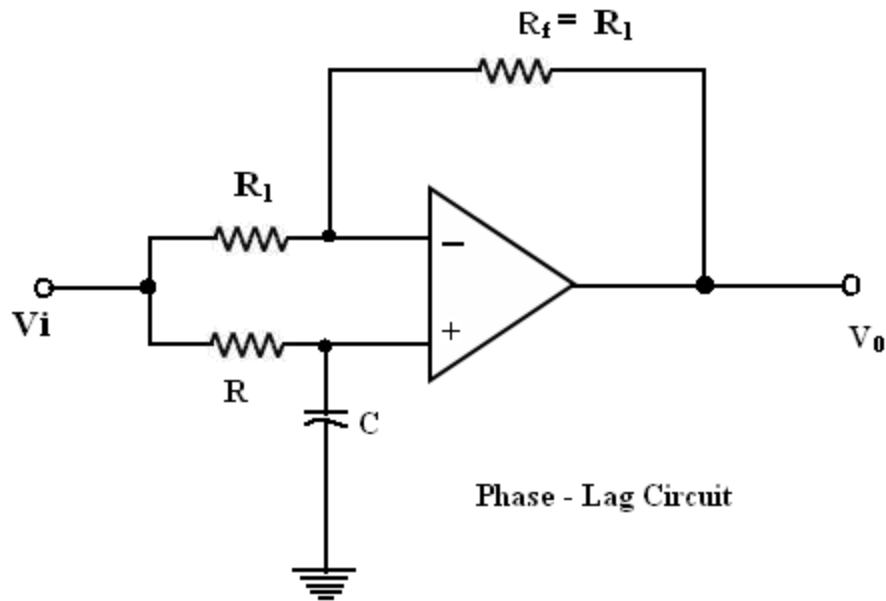
For the circuit fig a ,it can be written as

$$V_o \; jA\omega = @V_{i \; j\omega}^{b \; c} + 2 \; \dfrac{1}{1 + j\omega Rc} V_{i \; j\omega}^{b \; c}$$

Therefore,

$$V_o \, j A\omega = V_i \, j\omega + j @1 + 2 \frac{1}{1+j\omega Rc} \quad V_{i \, j\omega}^{b} k = V_{i \, jw}^{b} \frac{1}{1+jwRC}$$

The relationship between output and input can be expressed by

$$\frac{V_{jw}}{V_1 \, jw} = F \frac{1}{1+jwRC}$$

The relationship is complex as defined above equation and it shows that it has both magnitude and phase. Since the numerator and denominator are complex conjugates, their magnitudes are identical and the overall phase angle equals the angle of numerator less the angle of the denominator.

The phase angle is than given by

$$\theta = @\tan^{@1} wRC \, @\tan^{@1} wRC = @2 \tan^{@1} wRC \qquad @@@@ 3$$

Hence, when w=0, the phase angle approaches zero. When w=∞, the phase angle approaches -180⁰ . The Equation (3) becomes as

$$\theta = @2\tan^{@1} \frac{k}{f_0} \qquad @@@@@ 4 \quad \text{Where the frequency } f_0 \text{ is given by}$$

$$f_0 = \frac{1}{2\pi RC} \qquad @@@ 5 \quad \text{Here, when f=f}_0 \text{ in eq.4, the phase angle } \theta = -90^0 . \text{ The Bode plot}$$

for the phase-lag circuit is shown in fig.b

Phases-lead circuit:

Phase lag circuit
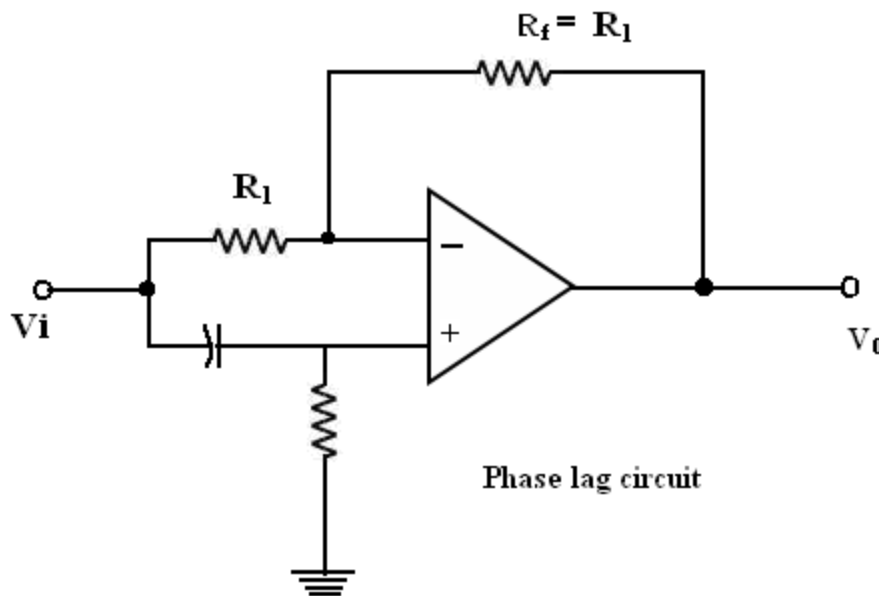
The phase lead circuit in fig a.in which the RC circuit forms a high pass network.The output voltage is derived and expressed by,

$$V_0(j\omega) = \left[-V_i(j\omega) + 2 \frac{j\omega RC}{1 + j\omega RC} V_i(j\omega) \right]$$

Therefore,

$$\frac{V_0(j\omega)}{V_i(j\omega)} = \frac{1 - j\omega RC}{1 + j\omega RC} \qquad @@@@@ 5$$

Frrom Equation 5 signifies that the ratio of magnitude is constant and phase is obtained as shown in equation 3.

It is to noted that the numerator has a negative real part and overall phase is given by

$$\theta = 180^0 - \tan^{-1} wRC - \tan^{-1} wRC = 180^0 - 2\tan^{-1} wRC \qquad @@@@ 3$$

When the frequency approaches zero,the phase angle approaches 180° As the frequency is increased, the leading phase decrease and it finally approaches zero at high frequencies. Hence can be written as

$$\theta = 180^° - 2\tan^{-1} \left(\frac{f}{f_o} \right)$$

Where $f_o = \frac{1}{2\Pi RC}$

Bode plot for the phase-lead circuit of below fig
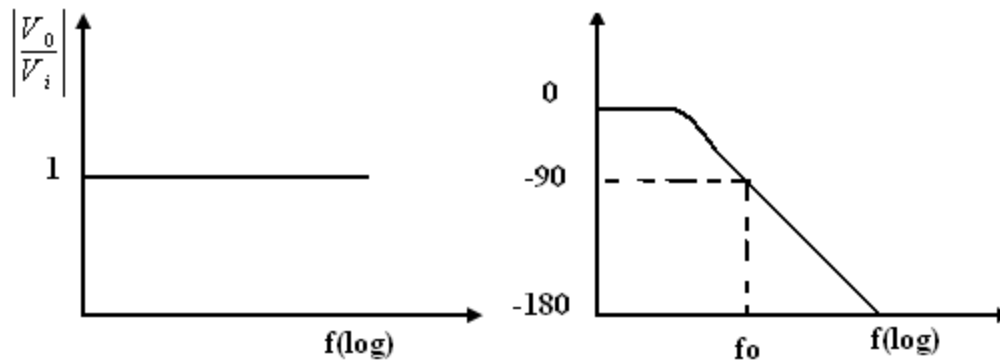
Voltage follower:

        If $R_1 = \infty$ and Rf=0 in the non inverting amplifier configuration .

The amplifier act as a unity-gain amplifier or voltage follower.

That is

$$A_v = 1 + \frac{R_f}{R_1} \ or \ \frac{R_f}{R_1} = A_v \ @1$$

Since $\frac{R_f}{R_1} = 0 \ A_v = 1$

The circuit consist of an op-amp and a wire connecting the output voltage to the input ,i.e the output voltage is equal to the input voltage, both in magnitude and phase. $V_0 = V_i$

Since the output voltage of the circuit follows the input voltage, the circuit is called voltage follower. It offers very high input impedance of the order of MΩ and very low output impedance.

Therefore, this circuit draws negligible current from the source. Thus, the voltage follower can be used as a buffer between a high impedance source and a low impedance load for impedance matching applications.

Voltage Follower
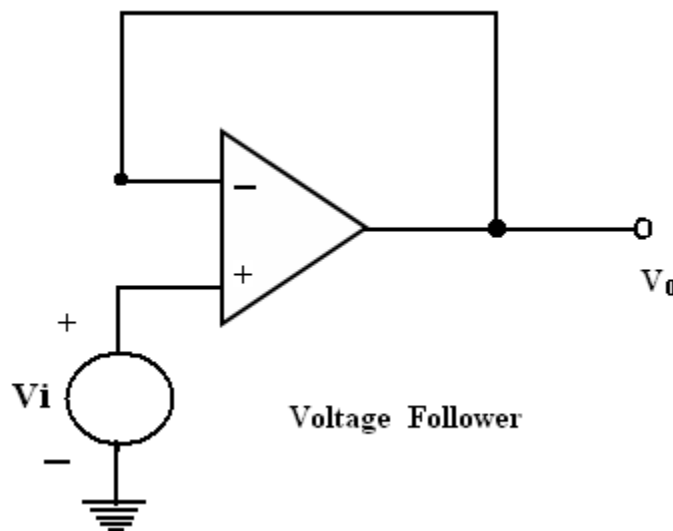
Voltage to Current Converter with floating loads (V/I):
1. Voltage to current converter in which load resistor R_L is floating (not connected to ground).
2. Vin is applied to the non inverting input terminal, and the feedback voltage across R_1 devices the inverting input terminal.
3. This circuit is also called as a current – series negative feedback amplifier.
4. Because the feedback voltage across R_1 (applied Non-inverting terminal) depends on the output current i_0 and is in series with the input difference voltage V_{id}.
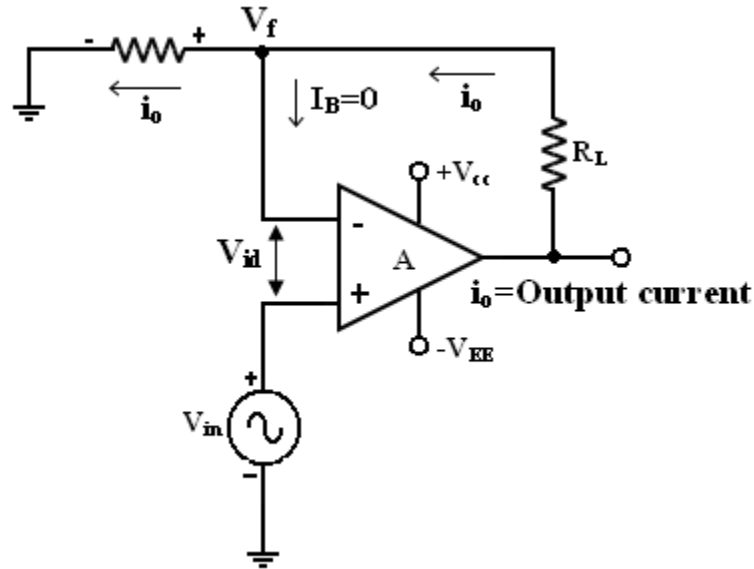
Writing KVL for the input loop,

$$Vin = V_{id} + V_f$$
$$V_{id} \doteq 0v, \text{ since } A \text{ is very large } A$$
$$Vin = V_f$$
$$Vin = R_1 i_0 \quad or \quad i_0 = \frac{Vin}{R_1}$$

From the fig input voltage Vin is converted into output current of Vin/R$_1$ [Vin -> i$_0$] . In other words, input volt appears across R$_1$. If R$_1$ is a precision resistor, the output current (i$_0$ = Vin/R$_1$) will be precisely fixed.

Applications:

1. Low voltage ac and dc voltmeters
2. Diode match finders
3. LED
4. Zener diode testers.

Voltage – to current converter with Grounded load:

This is the other type V – I converter, in which one terminal of the load is connected to ground.
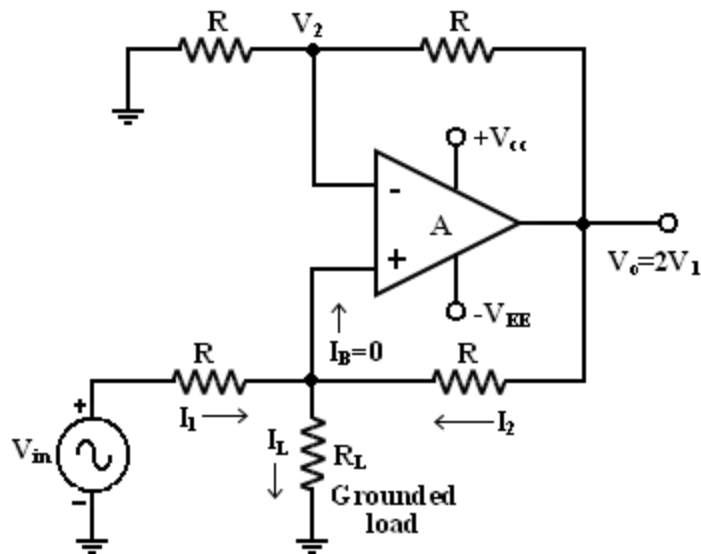
Analysis of the circuit:

The analysis of the circuit can be done by following 2 steps.

1. To determine the voltage V_1 at the non-inverting (+) terminals and
2. To establish relationship between V_1 and the load current I_L.

Applying KCL at node V_1 we can write that,

$$I_L = I_1 + I_2 \qquad @@@@\ 1$$

$$\text{But } I_1 = \frac{V_{in} @ V_1}{R} \text{ and } I_2 = \frac{V_0 @ V_1}{R}$$

Sub these values into eqn 1

$$I_L = \frac{V_{in} @ V_1}{R} + \frac{V_0 @ V_1}{R}$$

$$I_L = \frac{V_{in} R @ V_1 R + V_0 R @ V_1 R}{R^2}$$

$$= \frac{V_{in} + V_0 R @ 2V_1 R}{R^2}$$

$$= \frac{R\,V_{in} + V_0 @ 2V_1 R}{R^2}$$

$$I_L = \frac{V_{in} + V_0 @ 2V_1}{R}$$

$$RI_L = V_{in} + V_0 @ 2V_1 \qquad @@@@\ 2$$

$$V_1 = \frac{V_{in} + V_0 @ I_L R}{2} \qquad @@@@@\ 3$$

the op @amp is connected in the non @inverting mode A
gain f the circuit is

$$A_F = A + \frac{R}{R} = 2$$

The output voltage is given by

$$V_0 = A_F \, B \, V_1$$

$$V_0 = 2V_1 \qquad @@@@@\ 4$$

Sub V_1 eqn 3 into 4 we get

$$V_0 = \frac{2\,V_{in} + V_0 @ I_L R}{2}$$

$$V_0 = V_{in} + V_0 @ I_L R \qquad @@@@\ 5$$

$$V_{in} = I_L R$$

$$I_L = \frac{V_{in}}{R} \qquad @@@@\ 6$$

eqn 6 gives that the load current I_L is dependent on the input voltage V_{in} and Resistor R A

Current to Voltage Converter (I –V):
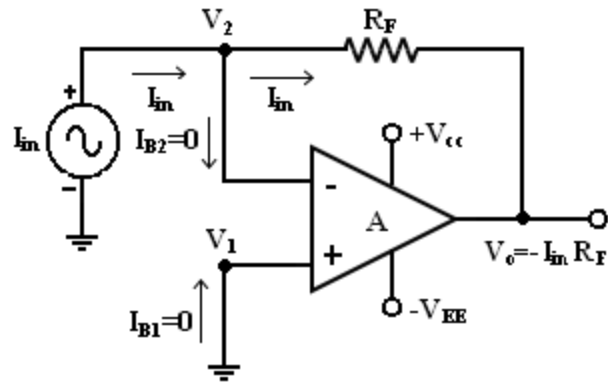
1. Open – loop gain a of the op-amp is very large. $V_1 \approx V_2$ @@@@ 1ᵕ

2. Input impedance of the op-amp is very high. (i.e) the currents entering into the 2 input terminals is very small. $I_{B_1} = I_{B_2} = 0$ ---(2)

3. Gain of the inv-amp is given by

$$A_F = @ \frac{R_{\#\#\#}}{R_1} = \frac{V_{\#\#\#}}{V_{in}} @@@ 3^a$$

$$V_0 = @ \frac{R_{\#\#\#}}{F_1} V_{in} @@@ 4^a$$

But $V_1 \approx V_2$ @@@@ 1ᵕ and $V_1 = 0$ as the non-inve(+) terminal is connected to ground. $V_2 = 0$.

Thus the inv –terminal (-) also is at ground and the entire input volt appears across R_1

.

$I_{in} = V_{in}/R_1$ -----(5)

$V_{in} = I_{in}/R_1$

Substituting this expression into eqn (4)

$$V_0 = @ \frac{R_{\#\#\#}}{R_1} I_{in} R_1 @@@@ 6^a$$

Eqn 96) indicates that the output volt (V_0) is proportional to the input current (I_{in}).

Sensitivity of the I – V converter:

1. The output voltage $V_0 = -R_F I_{in}$.

2. Hence the gain of this converter is equal to $-R_F$. The magnitude of the gain (i.e) is also called as sensitivity of I to V converter.

3. The amount of change in output volt ΔV_0 for a given change in the input current ΔI_{in} is decide by the sensitivity of I-V converter.

4. By keeping R_F variable, it is possible to vary the sensitivity as per the requirements.

Applications of V-I converter with Floating Load:

1. Diode Match finder:
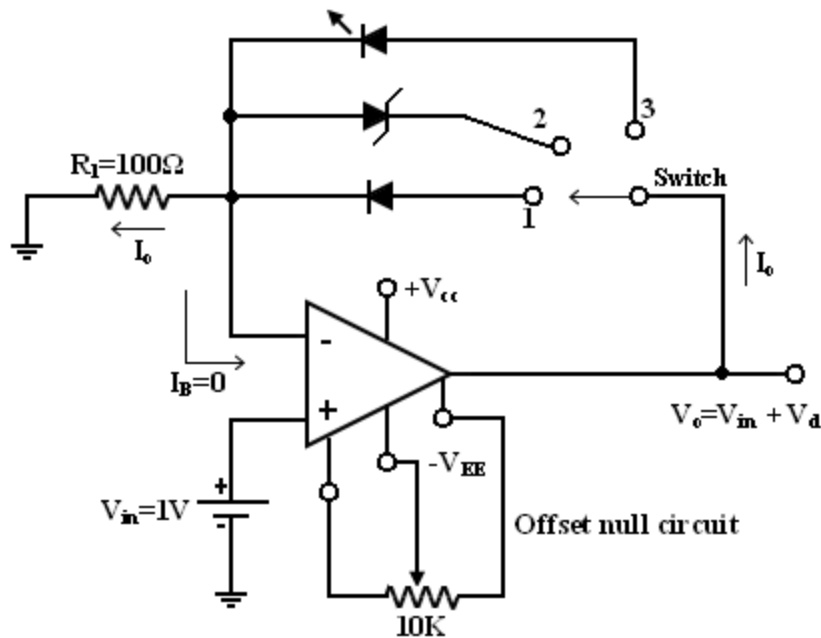
In some applications, it is necessary to have matched diodes with equal voltage drops at a particular value of diode current. The circuit can be used in finding matched diodes and is obtained from fig (V-I converter with floating load) by replacing R_L with a diode. When the switch is in position 1: (Diode Match Finder) Rectifierr diode (IN 4001) is placed in the f/b loop, the current through this loop is set by input voltage Vin and Resistor R_1. For Vin = 1V and R_1= 100Ω, the current through this

$I_0 = Vin/R_1 = 1/100 = 10mA$.

As long as V_0 and R_1 constant, I_0 will be constant. The Voltage drop across the diode can be found either by measuring the volt across it or o/p voltage. The output voltage is equal to (Vin + V_D) V_0 = Vin + V_D. To avoid an error in output voltage the op-amp should be initially nulled. Thus the matched diodes can be found by connecting diodes one after another in the feedback path and measuring voltage across them.

2. Zener diode Tester:

(When the switch position 2)

when the switch is in position 2, the circuit becomes a zener diode tester. The circuit can be used to find the breakdown voltage of zener diodes. The zener current is set at a constant value by Vin and R_1. If this current is larger than the knee current (I_{ZK}) of the zener, the zenerr blocks (V_z) volts.

For Ex:

I_{ZK} = 1mA , V_Z = 6.2V, Vin = 1v , R_1 = 100Ω Since the current through the zener is , I_0 = Vin/R_1 = 1/100 =10mA > I_{ZK} the voltage across the zener will be approximately equal to 6.2V.

3. When the switch is in position 3: (LED)

The circuit becomes a LED when the switch is in position 3. LED current is set at a constant value by Vin and R_1. LEDs can be tested for brightness one after another at this current. Matched LEDs with equal brightness at a specific value of current are useful as indicates and display devices in digital applications.

Applications of I – V Converter:
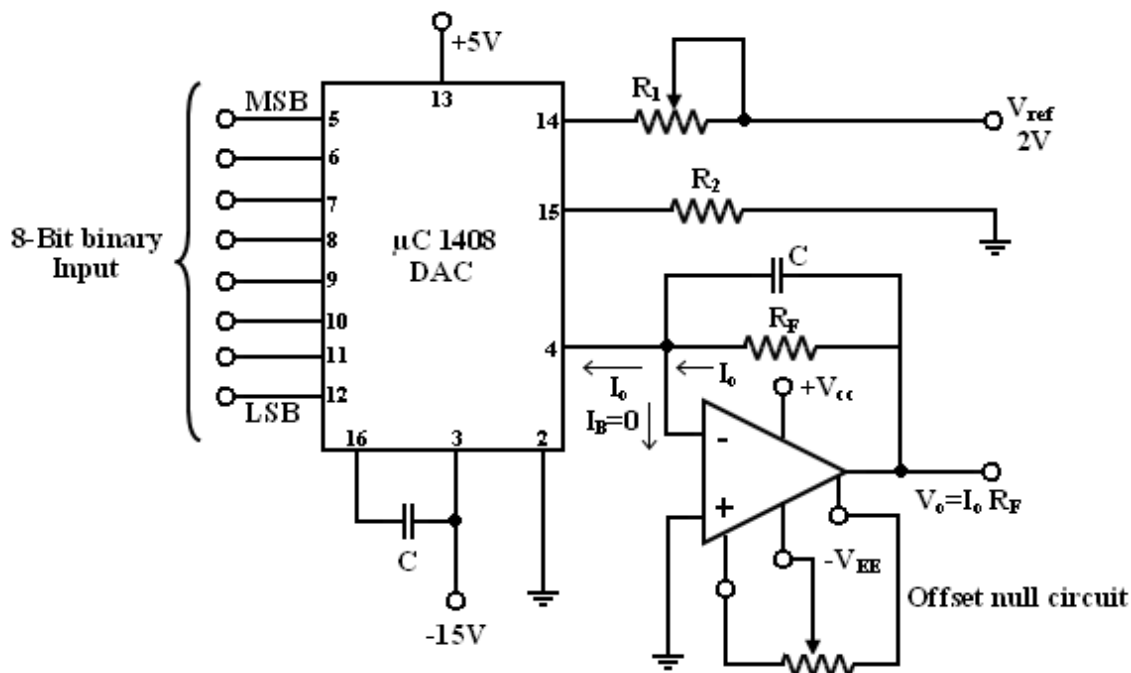
One of the most common use of the current to voltage converter is

1. Digital to analog Converter (DAC)

2. Sensing current through Photodetector. Such as photocell, photodiodes and photovoltaic cells.

Photoconductive devices produce a current that is proportional to an incident energy or light (i.e) It can be used to detect the light.

1. DAC using I – V converter:

It shows a combination of a DAC and current to voltage converter. The 8 digit binary signal is the input to the DAC and V_0 is the corresponding analog output of the current to voltage converter. The outputu of the DAC is current I_0, the value of which depends on the logic state (0 or 1), of the binary inputs as indicated by the following eqn.

$$I_0 = \frac{V_{ref}}{R_1}\left[\frac{D_7}{2} + \frac{D_6}{4} + \frac{D_5}{8} + \frac{D_4}{16} + \frac{D_3}{32} + \frac{D_2}{64} + \frac{D_1}{128} + \frac{D_0}{256}\right] \qquad (1)$$

$I_0 \Rightarrow \text{current of the DAC} \quad mA$

$R_1 \Rightarrow \text{Resistance} \quad k\Omega$

$V_{ref} \Rightarrow \text{Reference Voltage} \quad Volts$

$D_0 \, thro. \, D_7 \Rightarrow \text{Eight binary inputs}$

This means I_0 is zero when all inputs are logic 0.

I_0 is max when all inputs are logic 1.

The variations in I_0 can be converted into a desired o/p voltage range by selecting a proper value for R_F since, $V_0 = I_0 \, R_F$

Where I_0 is given by eqn (1). It is common to parallel R_F with capacitance C to minimize the overshoot. In the fig the o/p voltage of the current to voltage converter is positive because the direction of input current I_0 is opposite to that in the basic I – V Converter.

2. Detecting current through photosensitive devices:
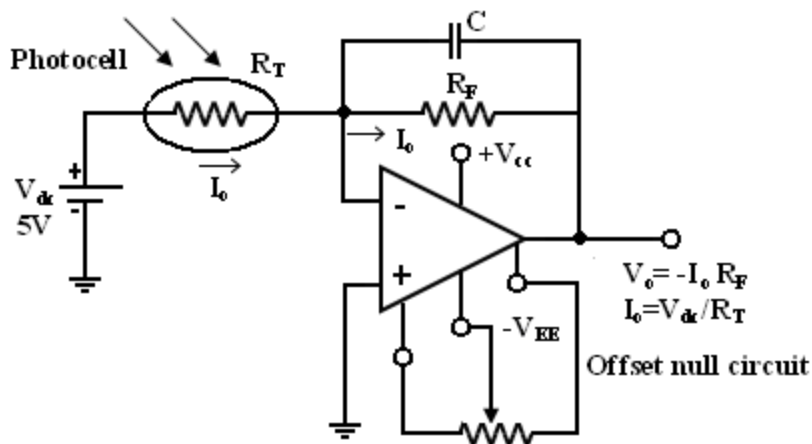
Photocells, photodiodes, photovoltaic cells give an output curren that depends on the intensity of light and independent of the load. The current through this devices can be converted to voltage by I – V converter and it can be used as a measure of the amount of light. In this fig photocell is connected to the I – V Converter. Photocell is a passive transducer, it requires an external dc voltage(Vdc). The dc voltage can be eliminated if a photovoltaic cell is used instead of a photocell. The Photovoltaic Cell is a semiconductor device that converts the radiant energy to electrical power. It is a self generating circuit because it doesnot require dc voltage externally. Ex of Photovoltaic Cell : used in space applications and watches.

Summing Amplifier:

Op-amp may be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or a summer.

An inverting summer or a non-inverting summer may be discussed now.

Inverting Summing Amplifier:

Fig 2
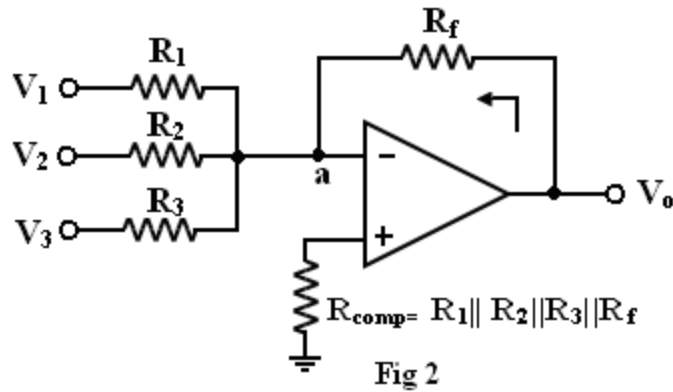
A typical summing amplifier with three input voltages V_1, V_2 and V_3 three input resistors R_1, R_2, R_3 and a feedback resistor R_f is shown in figure 2.

The following analysis is carried out assuming that the op-amp is an ideal one, that is, $A_{OL} = \infty$. Since the input bias current is assumed to be zero, there is no voltage drop across the resistor R_{comp} and hence the non-inverting input terminal is at ground potential.

The voltage at nod 'a' is zero as the non-inverting terminal is grounded. The nodal equation be KCL at node 'a' is

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_o}{R_f} = 0$$

Or,

$$V_o = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3 \right]$$

Thus the output in an inverted, weighted sum of the inputs. In the special case, when $R_1 = R_2 = R_3 = R_f$, we have

$$V_o = -\left[V_1 + V_2 + V_3 \right]$$

in such case the output V_o is the inverted sum of the input signals. We may also set

$$R_1 = R_2 = R_3 = 3R_f$$

in which case

$$V_o = -\left[\frac{V_1 + V_2 + V_3}{3} \right]$$

Thus the output is the average of the input signals (inverted). In a practical circuit, input bias current compensating resistor R_{comp} should be provided.

To find R_{comp}, make all inputs $V_1 = V_2 = V_3 = 0$. So the effective input resistance $R_i = R_1 \parallel R_2 \parallel R_3$. Therefore, $R_{comp} = R_i \parallel R_f = R_1 \parallel R_2 \parallel R_3 \parallel R_f$.

Non-Inverting Summing Amplifier:
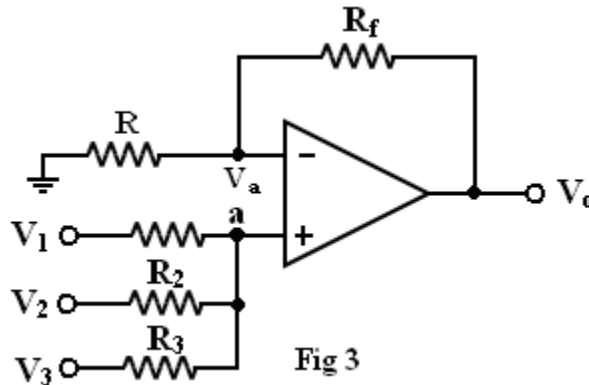
Fig 3

A summer that gives a non-inverted sum is the non-inverting summing amplifier of figure 3. Let the voltage at the (-) input teriminal be V_a.

The voltage at (+) input terminal will also be V_a. The nodal equation at node 'a' is given by

$$\frac{V_1 - V_a}{R_1} + \frac{V_2 - V_a}{R_2} + \frac{V_3 - V_a}{R_3} = 0$$

from which we have,

$$V_a = \frac{\dfrac{V_1}{R_1} + \dfrac{V_2}{R_2} + \dfrac{V_3}{R_3}}{\dfrac{1}{R_1} + \dfrac{1}{R_2} + \dfrac{1}{R_3}}$$

The op-amp and two resistors and R constitute a non-inverting amplifier with

$$V_o = \left(1 + \frac{R_f}{R}\right) V_a$$

Therefore, the output voltage is,

$$V_o = \left(1 + \frac{R_f}{R}\right)\frac{\dfrac{V_1}{R_1} + \dfrac{V_2}{R_2} + \dfrac{V_3}{R_3}}{\dfrac{1}{R_1} + \dfrac{1}{R_2} + \dfrac{1}{R_3}}$$

which is a non-inverting weighted sum of inputs.

Let $R_1 = R_2 = R_3 = R = R_f/2$, then $V_o = V_1 + V_2 + V_3$

Subtractor:

Fig 4
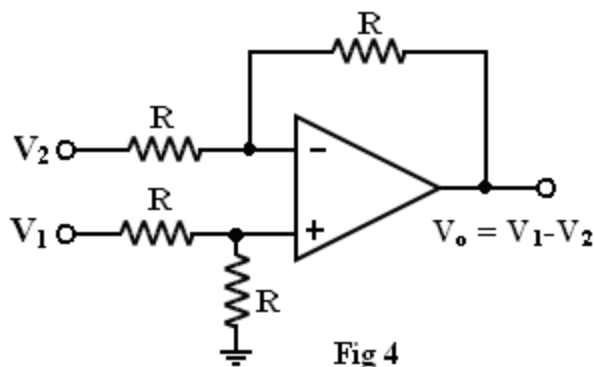
A basic differential amplifier can be used as a subtractor as shown in the above figure. If all resistors are equal in value, then the output voltage can be derived by using superposition principle.

To find the output V_{01} due to V_1 alone, make $V_2 = 0$.

Then the circuit of figure as shown in the above becomes a non-inverting amplifier having input voltage $V_1/2$ at the non-inverting input terminal and the output becomes

$$V_{01} = \frac{V_1}{2}\left(1 + \frac{R}{R}\right) = V_1$$

Similarly the output V_{02} due to V_2 alone (with V_1 grounded) can be written simply for an inverting amplifier as

$$V_{02} = -V_2$$

Thus the output voltage V_o due to both the inputs can be written as

$$V_o = V_{01} + V_{02} = V_1 - V_2$$

Adder/Subtractor:

$V_o = (V_3 + V_4) - (V_1 + V_2)$

Fig 5(a)

$V_{01} = -V_1$
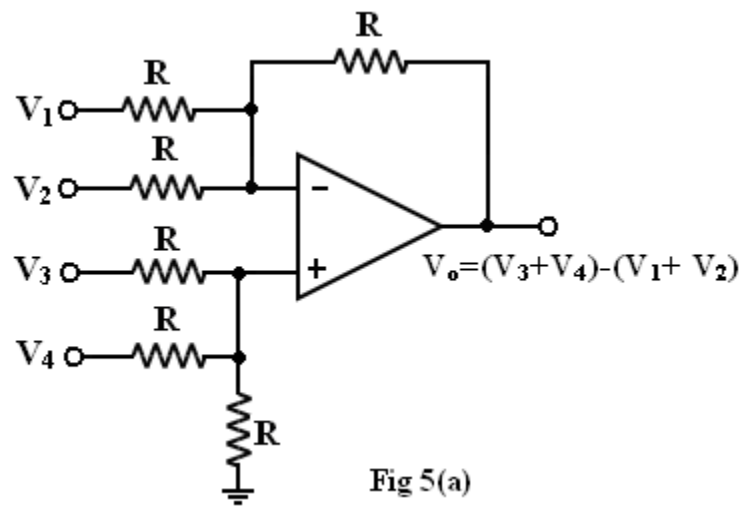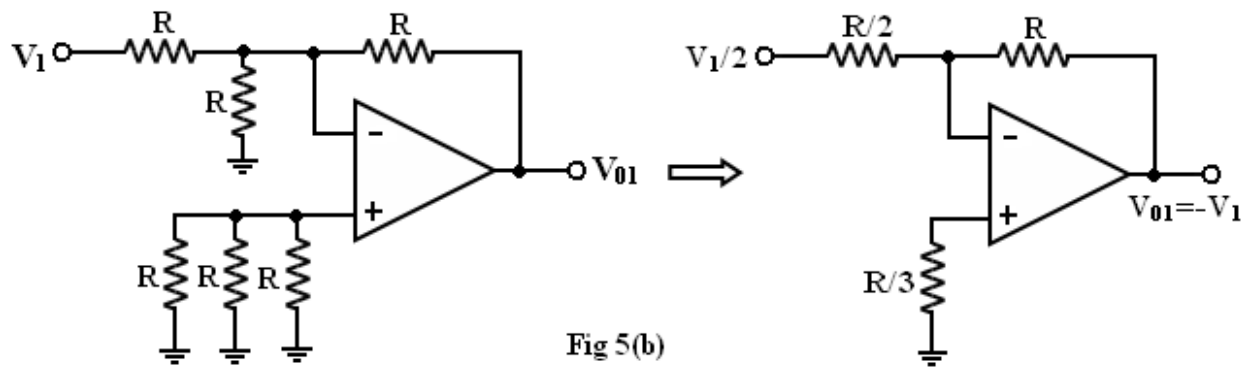
Fig 5(b)
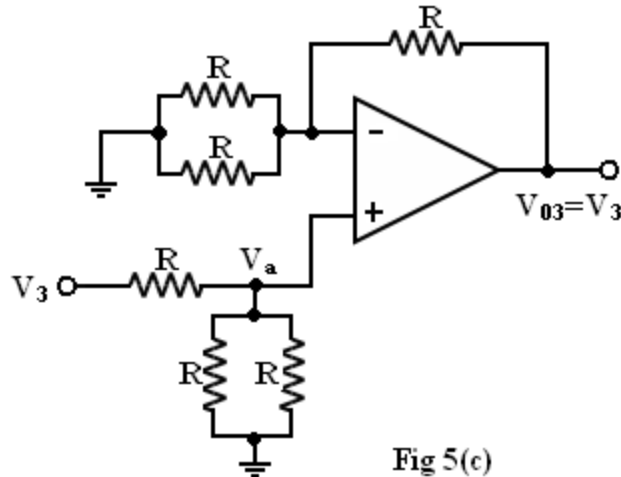
Fig 5(c)

It is possible to perform addition and subtraction simultaneously with a single op-amp using the circuit shown in figure 5(a).

The output voltage V_o can be obtained by using superposition theorem. To find output voltage V_{01} due to V_1 alone, make all other input voltages V_2, V_3 and V_4 equal to zero.

The simplified circuit is shown in figure 5(b). This is the circuit of an inverting amplifier and its output voltage is,

$$V_{01} = @ \frac{R \| R}{\frac{R}{2}} = @1$$

(by Thevenin's equivalent circuit at inverting input terminal).

Similarly, the output voltage V_{02} due to V_2 alone is,

$$V_{02} = @ V_2$$

Now, the output voltage V_{03} due to the input voltage signal V_3 alone applied at the (+) input terminal can be found by setting V_1, V_2 and V_4 equal to zero.

The circuit now becomes a non-inverting amplifier as shown in figure 5(c). The voltage V_a at the non-inverting terminal is

$$V_a = \frac{\frac{R}{2}}{R + \frac{R}{2}} V_3 = \frac{V_3}{3}$$

So, the output voltage V_{03} due to V_3 alone is

$$V_{03} = \left(1 + \frac{R_f}{R_2}\right)V_a = 3\,\frac{V_3}{3} = V_3$$

Similarly, it can be shown that the output voltage V_{04} due to V_4 alone is

$$V_{04} = V_4$$

Thus, the output voltage V_o due to all four input voltages is given by

$$V_o = V_{01} + V_{02} + V_{03} + V_{04}$$

$$V_o = @V_1 @V_2 + V_3 + V_4$$

$$V_o = V_3 + V_4 @ V_1 + V_2$$

So, the circuit is an adder-subtractor.

Instrumentation Amplifier:

Fig 6(a)

Fig 6(b)

Resistive transducer $R_T \pm \Delta R$
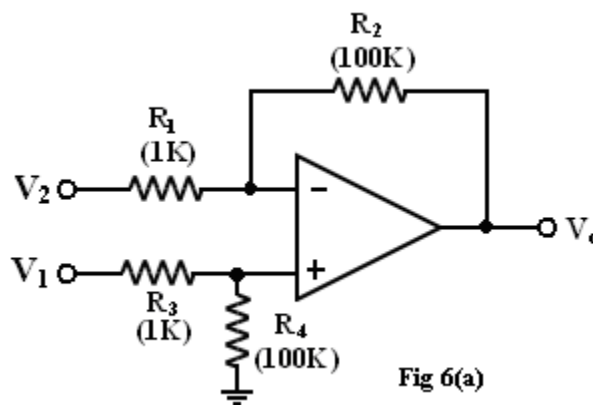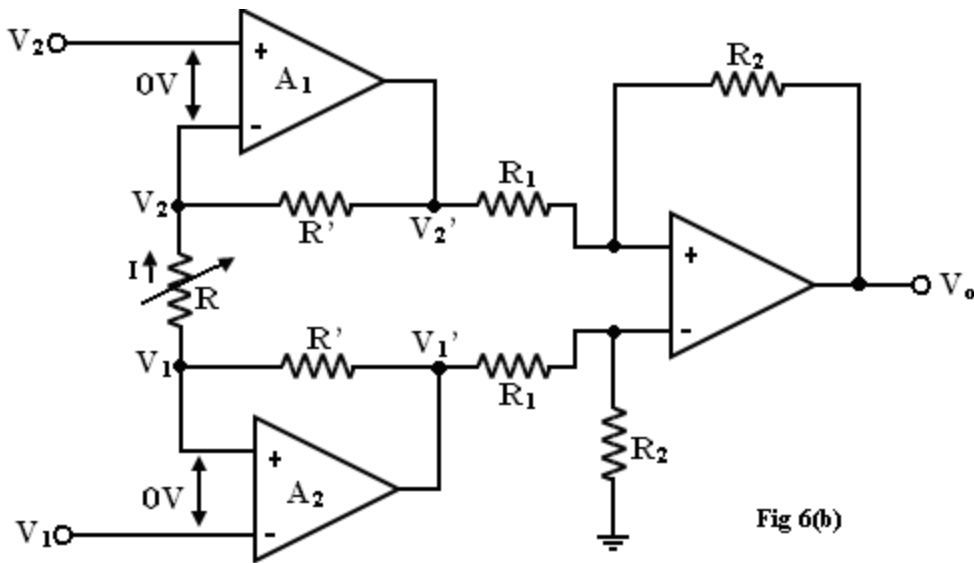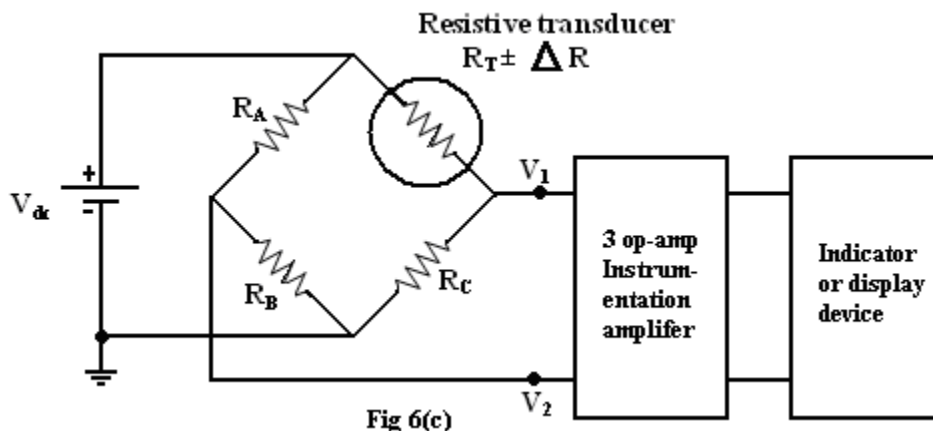
Fig 6(c)

In a number of industrial and consumer applications, one is required to measure and control physical quantities.

Some typical examples are measurement and control of temperature, humidity, light intensity, water flow etc. these physical quantities are usually measured with help of transducers.

The output of transducer has to be amplified so that it can drive the indicator or display system. This function is performed by an instrumentation amplifier. The important features of an instrumentation amplifier are

1. high gain accuracy

2. high CMRR

3. high gain stability with low temperature coefficient

4. low output impedance

There are specially designed op-amps such as µA725 to meet the above stated requirements of a good instrumentation amplifier. Monolithic (single chip) instrumentation amplifier are also available commercially such as AD521, AD524, AD620, AD624 by Analog Devices, LM363.XX (XX -->10,100,500) by National Semiconductor and INA101, 104, 3626, 3629 by Burr Brown.

Consider the basic differential amplifier as shown in figure 6(a). It can be easily seen that the output voltage V_o is given by,

$$V_o = -\frac{R_2}{R_1}V_2 + \frac{1}{1+\frac{R_2}{R_4}}V_1\left(1+\frac{R_2}{R_1}\right) \qquad V^+ = \frac{R_4}{R_3+R_4}V_1$$

Or,
$$V_o = -\frac{R_2}{R_1}V_2 - \frac{1}{1+\frac{R_2}{R_4}}\left(\frac{R_2}{R_2}+1\right)V_1$$

For $R_1/R_2 = R_3/R_4$, we obtain

$$V_o = \frac{R_2}{R_1}V_1 - V_2$$

In the circuit of figure 6(a), source V_1 sees an input impedance $= R_3+R_4$ (=101K) and the impedance seen by source V_2 is only R_1 (1K). This low impedance may load the signal source heavily.

Therefore, high resistance buffer is used preceding each input to avoid this loading effect as shown in figure 6(b).

The op-amp A_1 and A_2 have differential input voltage as zero. For $V_1=V_2$, that is, under common mode condition, the voltage across R will be zero. As no current flows through R and R' the non-inverting amplifier.

A_1 acts as voltage follower, so its output $V_2'=V_2$. Similarly op-amp A_2 acts as voltage follower having output $V_1'=V_1$. However, if $V_1 \neq V_2$, current flows in R and R', and $(V_2'-V_{1'})>(V_2-$

V_1). Therefore, this circuit has differential gain and CMRR more compared to the single op-amp circuit of figure 6(a).

The output voltage V_o can be calculated as follows

The voltage at the (+) input terminal of op-amp A_3 is $\dfrac{R_2 V_1'}{R_1 + R_2}$. Using superposition theorem, we have,

$$V_o = -\frac{R_f}{R_1} V_2' + \left(1 + \frac{R_g}{R_1}\right)\frac{R_2 V_1'}{R_1 + R_2}$$

$$V_o = \frac{R_b}{R_1}\left(V_1' - V_2'\right) \qquad \cdots (1)$$

Since, no current flows into op-amp, the current I flowing (upwards) in R is $I = (V_1 - V_2)/R$ and passes through the resistor R'.

$$V_1' = R'I + V_1 = \frac{R'}{R}\left(V_1 - V_2\right) + V_1$$

and

$$V_2' = -R'I + V_2 = -\frac{R'}{R}\left(V_1 - V_2\right) + V_2$$

Putting the values of V_1' and V_2' in equation (1), we obtain,

$$V_o = \frac{R}{R_1}\left[\frac{2R'}{R}\left(V_1 - V_2\right) + \left(V_1 - V_2\right)\right]$$

Or,

$$V_o = \frac{R}{R_1}\left(1 + \frac{2R'}{R}\right)\left(V_1 - V_2\right) \qquad \cdots (2)$$

In equation (2), if we choose $R_2 = R_1 = 25K$ (say) and $R' = 25K$; $R = 50\Omega$, then a gain of

$$\left[1 + 2 + \frac{25K}{50\Omega}\right] = 1001$$ can be achieved.

The difference gain of this instrumentation amplifier R, however should never be made zero, as this will make the gain infinity. To avoid such a situation, in a practical circuit, a fixed resistance in series with a potentiometer is used in place of R.

Figure 6(c) shows a differential instrumentation amplifier using Transducer Bridge. The circuit uses a resistive transducer whose resistance changes as a function of the physical quantity to be measured.

The bridge is initially balanced by a dc supply voltage V_{dc} so that $V_1 = V_2$. As the physical quantity changes, the resistance R_T of the transducer also changes, causing an unbalance in the bridge ($V_1 \neq V_2$). This differential voltage now gets amplified by the three op-amp differential instrumentation amplifier.

There are number differential applications of instrumentation amplifier with the transducer bridge, such as temperature indicator, temperature controller, and light intensity meter to name a few.

Differentiator:

One of the simplest of the op-amp circuits that contains capacitor in the differentiating amplifier.

Differentiator:

As the name implies, the circuit performs the mathematical operation of differentiation (i.e) the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor R_1 is replaced by a capacitor C_1.

The expression for the output voltage can be obtained KCL eqn written at node V_2 as follows,

$$i_c = I_B + i_F \qquad @@@@\ 1$$

$$Since\ I_B \ t\ 0$$

$$i_c = i_f$$

$$C_1 \frac{d\ b}{dt} V_{in} @V_2{}^c = \frac{V}{R_F}$$

$$But\ V_1 = V_2\ t\ 0V,\ because\ A\ is\ very\ large\ A Therefore,$$

$$C_1 \frac{d}{dt} = @ \frac{V}{R_F}$$

$$or$$

$$V_0 = @^b\ R_F\ C_1{}^c \frac{d}{dt} \qquad @@@\ 2\ ^a$$

Since the differentiator performs the reverse of the integrator function.

Thus the output V_0 is equal to $R_F C_1$ times the negative rate of change of the input voltage Vin with time.

The –sign => indicates a 180^0 phase shift of the output waveform V_0 with respect to the input signal.

The below circuit will not do this because it has some practical problems.

The gain of the circuit (R_F/XC_1) R with R in frequency at a rate of 20dB/decade. This makes the circuit unstable.

Also input impedance XC_1 S with R in frequency which makes the circuit very susceptible to high frequency noise.
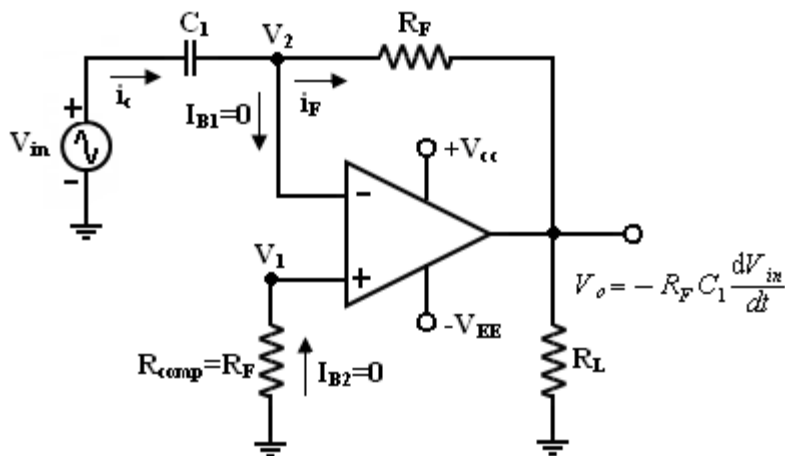
Basic Differetntiator
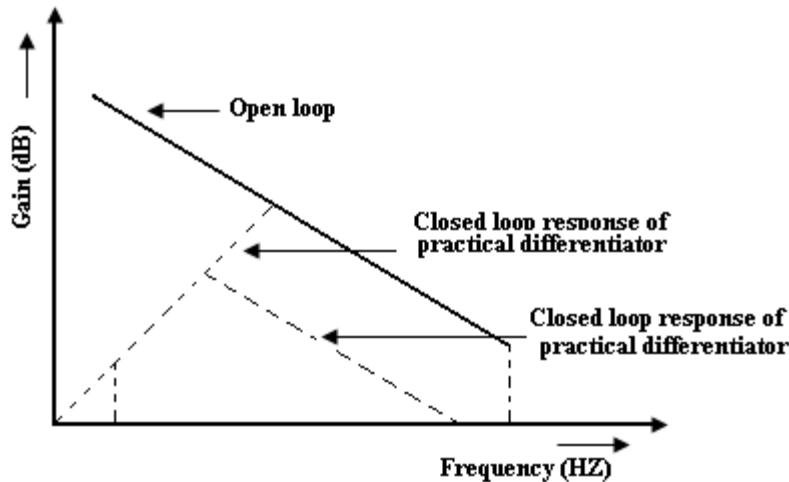
From the above fig, f_a = frequency at which the gain is 0dB and is given by,

$$f_a = \frac{1}{2\pi R_F C_1} \quad @@@@ \; 3^a$$

f_C @> Unity @gain bandwidth of the op @amp and f =relative operating frequency A

Both stability and high frequency noise problems can be corrected by the addition of 2 components. R_1 and C_F. This circuit is a practical differentiator.

From Frequency f to feedback the gain R_S at 20dB/decade after feedback the gain S at 20dB/decade. This 40dB/ decade change in gain is caused by the $R_1 C_1$ and $R_F C_F$ combinations.

The gain limiting frequency f_b is given by,

$$f_b = \frac{1}{2\pi R_F C_1} \quad @@@@ \; 4^a$$

Where $R_1 C_1 = R_F C_F$

$R_1 C_1$ and $R_F C_F$ => helps to reduce the effect of high frequency input, amplifier noise and offsets.

All $R_1 C_1$ and $R_F C_F$ make the circuit more stable by preventing the R in gain with frequency.

Generally, the value of Feedback and in turn $R_1 C_1$ and $R_F C_F$ values should be selected such that

$$f_a < f_b < f_c \quad @@@@ \; 2^{\smile}$$

where

$$f_a = \frac{1}{2\pi R_F C_1}$$

$$f_b = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_F C_F}$$

f_c = unity gain bandwidth

The input signal will be differentiated properly, if the time period T of the input signal is larger than or equal to $R_F C_1$ (i.e) $T > R_F \; C_1$
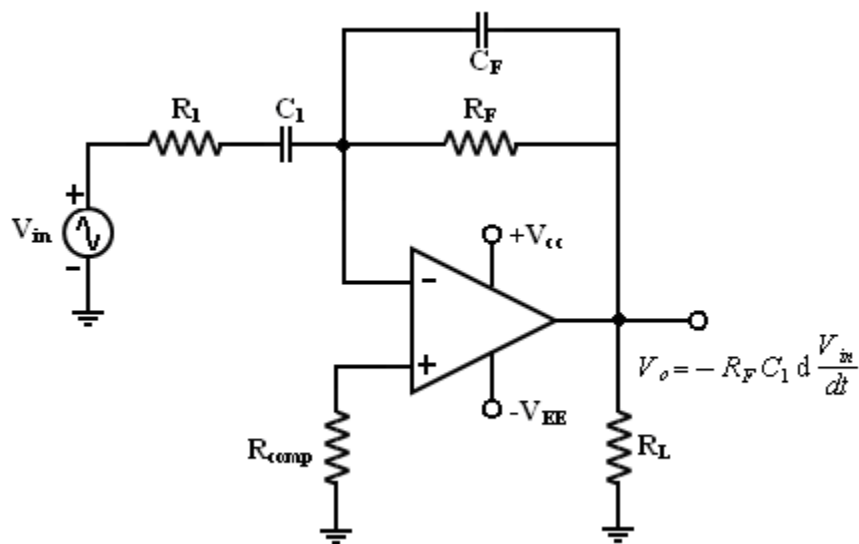
Practical Differentiator

A workable differentiator can be designed by implementing the following steps.

1. Select fa equal to the highest frequency of the input signal to be differentiated then assuming a value of $C_1 < 1\mu f$. Calculate the value of R_F.

2. Choose fb = 20fa and calculate the values of R_1 and C_F so that $R_1 C_1 = R_F C_F$.

Uses:

Its used in waveshaping circuits to detect high frequency components in an input signal and also as a rate of change and detector in FM modulators.

(a) Square wave input

(b) Output for (a)

(c) Sinusoidal input

(d) Output for (c)
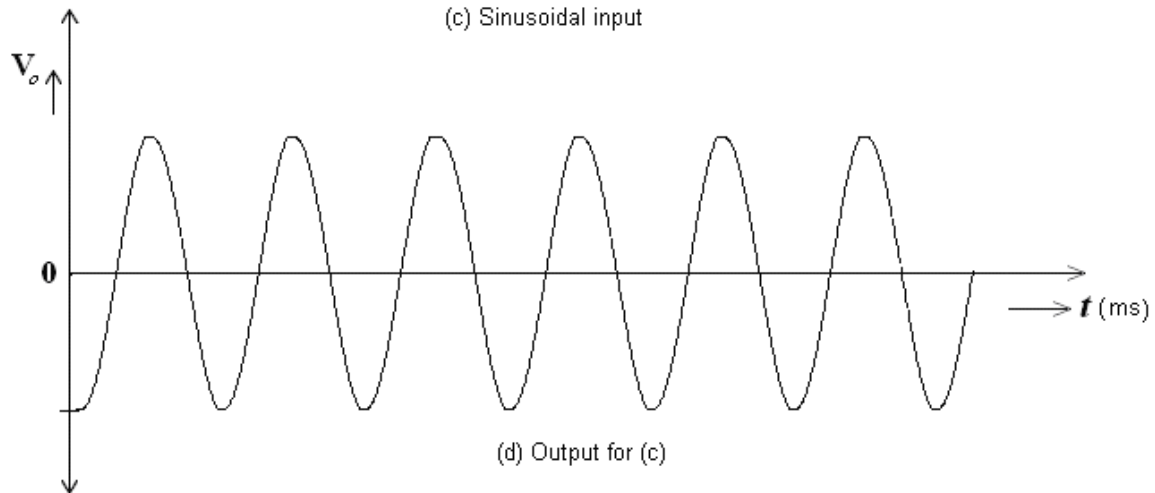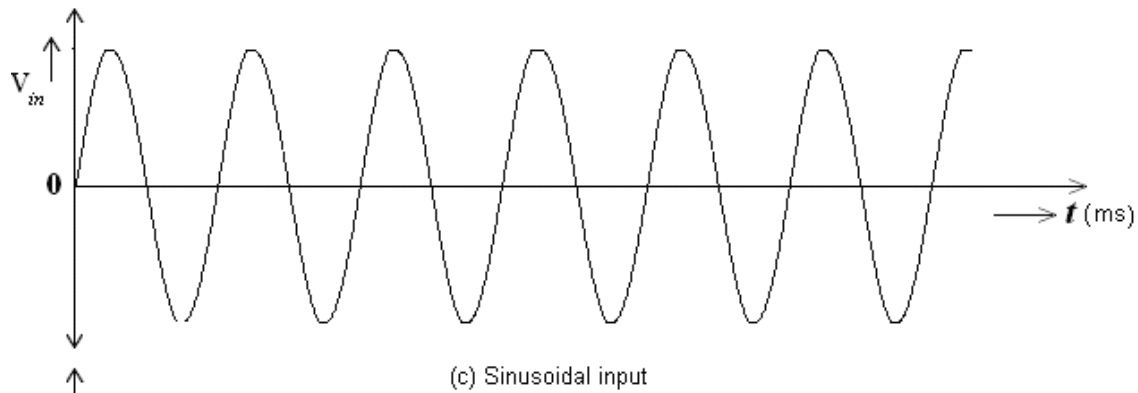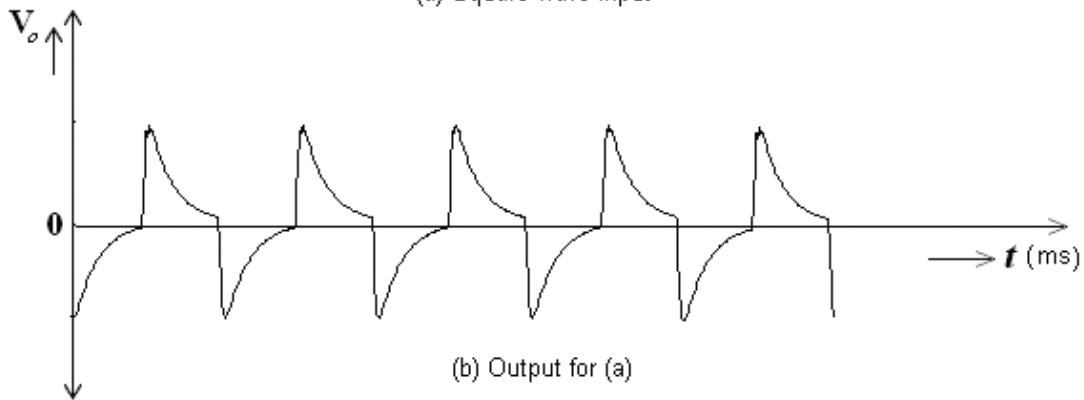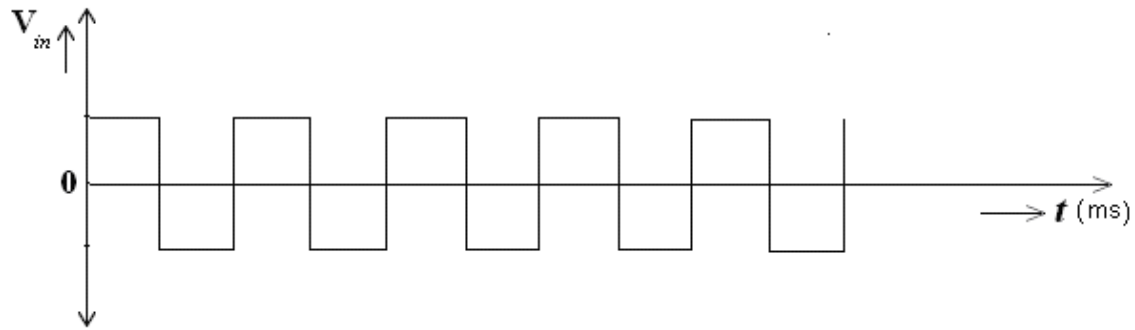
This o/p for practical differentiator.

Integrator:

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator or Integration Amplifier. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_F is replaced by a capacitor C_F.

The expression for the output voltage V_0 can be obtained by KVL eqn at node V_2.

$$V_o = -\frac{1}{R_1 C_F} \int_0^t V_{in} \, dt + C$$
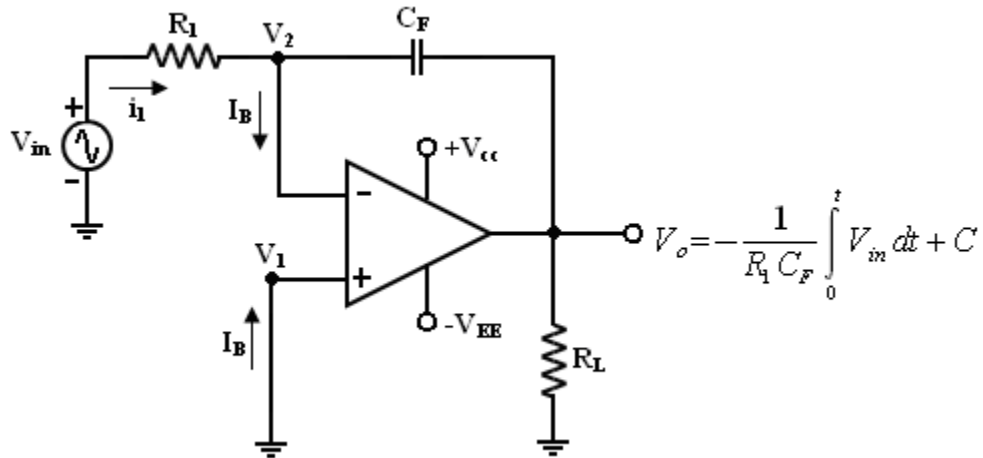
$$i_1 = I_B + i_f \quad @@@@@@@ \; (1)$$

Since I_B is negligible small,

$$i_1 \approx i_F$$

Relation between current through and voltage across the capacitor is

$$i_C = C \frac{dV}{dt} \quad @@ \; (2a)$$

$$\frac{V_{in} - V_1}{R_1} = C_F \frac{d(V_1 - V_0)}{dt} \qquad (2b)(2c)$$

However, $V_1 = V_2 \approx 0$ because A is very large,

$$\frac{V_{in}}{R_1} = C_F \frac{d(-V_0)}{dt} \qquad (2b)(2c)$$

The output voltage can be obtained by integrating both sides with respect to time:

$$\int_0^t \frac{V_{in}}{R_1} dt = \int_0^t C_F \frac{d(-V_0)}{dt} dt$$

$$= C_F(-V_0) + \frac{V_0}{t}\Big|_{t} = 0$$

$$V_0 = -\frac{1}{R_1 C_F} \int_0^t V_{in}\, dt + C \qquad @@@@ \; (3a)(3c)$$

where C @ integration constant A

eqn (3) indicates that the output is directly proportional to the negative integral of the input volts and inversely proportional to the time constant $R_1 C_F$.

Ex: If the input is sine wave -> output is cosine wave.

If the input is square wave -> output is triangular wave.

(a) Square Wave input

(b) Output for (a)

(c) sinusodial input

(d) Output for (c)

These waveform with assumption of $R_1 C_f = 1$, Vout =0V (i.e) C =0.

When Vin = 0 the integrator works as an open loop amplifier because the capacitor C_F acts an open circuit to the input offset voltage Vio.

Or

The Input offset voltage Vio and the part of the input are charging capacitor C_F produce the error voltage at the output of the integrator.

Practical Integrator:

$$V_o = -\frac{1}{R_1 C_F} \int_0^1 V_{in} dt \text{ with } V_{ooT} = 0$$
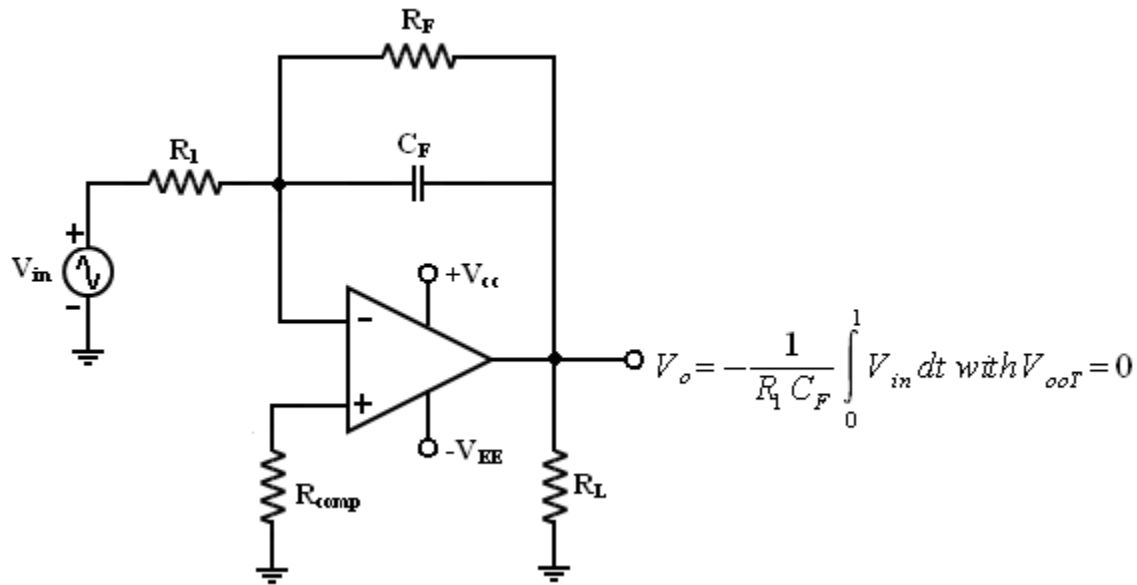
Practical Integrator to reduce the error voltage at the output, a resistor R_F is connected across the feedback capacitor C_F.

Thus R_F limits the low frequency gain and hence minimizes the variations in the output voltages. The frequency response of the basic integrator, shown from this fb is the frequency at which the gain is dB and is given by,

$$f_b = \frac{1}{2\pi R_F C_1} @@@@ 4^a$$

Both the stability and low frequency roll-off problems can be corrected by the addition of a resistor R_F in the practical integrator.

Stability -> refers to a constant gain as frequency of an input signal is varied over a certain range.

Low frequency -> refers to the rate of decrease in gain roll off at lower frequencies.

From the fig of practical Integrators,

f is some relative operating frequency and for frequencies f to fa to gain R_F / R_1 is constant. After fa the gain decreases at a rate of 20dB/decade or between fa and fb the circuit act as an integrator.

The gain limiting frequency fa is given by $f_a = \dfrac{1}{2\pi R_F C_F}$ @@@ 5

Generally the value of fa and in turn $R_1 C_F$ and $R_F C_F$ values should be selected such that fa<fb. In fact, the input signal will be integrated properly if the time period T of the signal is larger than or equal to $R_F C_F$, (i.e)

$$T \geq R_F C_F \quad @@@@ \; 6$$

Where

$$R_F C_F = \dfrac{1}{2\pi f_a}$$

Uses:

Most commonly used in analog computers.

ADC

Signal wave shaping circuits.

Log and Antilog Amplifier:

There are several applications of log and antilog amplifiers. Antilog computation may require functions such as ln x, log x or Sinhx.

These can be performed continusely with log amps, and also used for direct dB display on a digital Voltmeter and Spectrum analyzer.

Log-amp can also be used to compress the dynamic range of a signal.

Log Amplifier:

The fundamental log amp circuit shown in fig

Fig a. Fundamental log-amp Circuit

Where a grounded base transistor is placed in the feedback path. Since the collector is placed in the feedback path.

Since the collector is held at virtual ground and the base is also grounded, the transistor's voltage-current relationship becomes that of a diode and is given by,

$$I_E = I_s\, e^{\frac{q V_E}{kT}} @ 1 \quad \text{---------------(1)}$$

Since, I c = I_E for a grounded base transistor.

$$I_C = I_s\, e^{\frac{q V_E}{kT}} @ 1 \quad \text{--------------} \quad (2)$$

Is-emitter saturation current $\approx 10^{-13}$A

k=Boltzmann's constant

T=absolute temperature(in $^\circ$K)

Therefore $\dfrac{I_C}{I_s} = e^{\frac{q V_E}{kT}} @ 1 \quad \text{----------(3)}$

Or

$$e^{\frac{q V_E}{kT}} = \frac{I_C}{I_s} + 1$$

$$\approx I_c/I_s \qquad\qquad (\text{as Is} \approx 10^{-13}\text{A}, I_c >> I_s)$$

Taking natural log on both sides, we get

$$v_E = \frac{kT}{q} \ln \frac{I_C}{I_s} \quad \text{----------------(4)}$$

Also in fig a

Ic= V_i/R_1

$V_E = -V_o$

So
$$V_o = -\frac{KT}{q} \ln\frac{V_{in}}{R_1 I_s} = -\frac{KT}{q} \ln\frac{V_{in}}{V_{ref}} \qquad\text{---------------(5)}$$

Where $V_{ref} = R_1 I_s$

The output voltage is thus proportional to the logarithm of input voltage.

Although the circuit gives natural log (ln),one can find $\log_{10}$ by proper scaling

$$\text{Log}10X = 0.4343 \ln X \text{----------------------(6)}$$

The circuit have one problem.

The emitter saturation current Is varies from transistor to transistor and with temperature. Thus a stable reference voltage V ref cannot be obtained

This is eliminated by the circuit given in fig(b)

The input is applied to one log-amp, while a reference voltage is applied to one log-amp,while a reference voltage is applied to another log-amp.

The two transistors are integrated close together in the same silicon wafer. This provides a close match of saturation currents and ensures good thermal tracking.

Fig(b)Log-amp with saturation current and temperature compensation

$$\text{Assume} \quad I_{S1} = I_{S2} = I_S \text{------------------------(7)}$$

And then ,
$$V_1 = \frac{KT}{q} \ln\frac{V_{in}}{R_1 I_s} \qquad\text{--------------(8)}$$

And
$$V_2 = \frac{KT}{q} \ln\frac{V_{ref}}{R_1 I_s} \qquad\text{--------------------(9)}$$

Now,
$$V_o = V_2 - V_1 = \frac{KT}{q}\left[\ln\frac{V_{ref}}{R_1 I_s} - \ln\frac{V_{in}}{R_1 I_s}\right] \qquad\text{----------(10)}$$

$$V_o = \frac{KT}{q} \ln\frac{V_{in}}{V_{ref}} \qquad\text{-------------------(11)}$$

Thus the reference level is now set with a single external voltage source. Its dependence on device and temperature has been removed. The voltage vo is still dependent upon temperature and is directly proportional to T. This is compensated by the last op-amp stage A_4 which provides a non-inverting gain of $(1+R_2/R_{TC})$. Now, the output voltage is

$$v_o\,comp = \left(1 + \frac{R_2}{R_{TC}}\right)\frac{kT}{q}\ln\left(\frac{V}{V_{ref}}\right) \qquad\text{----------------------(12)}$$

Where R_{TC} is a temperature-sensitive resistance with a positive coefficient of temperature (sensor) so that the slope of the equation becomes constant as the temperature changes.

Antilog Amplifier

The Circuit is shown in fig .The input Vi for the antilog-amp is fed into the temperature compensating voltage divider R_2 and R_{TC} and then to the base of Q_2. The output V_o of the antilog-amp is fed back to the inverting input of A_1 through the resistor R_1. The base to emitter voltage of transistors Q_1 and Q_2 can be written as

$$V_{Q1\,B@E} = \frac{kT}{q}\ln\left(\frac{V_o}{R_1 I_s}\right) \qquad\text{------------------(!3)}$$

And

$$V_{Q2\,B@E} = \frac{kT}{Q}\ln\left(\frac{V_i}{R_1 I_s}\right) \qquad\text{--------------------(14)}$$

Since the base of Q_1 is tied to ground, we get

$$V_{A=}\ @V_{Q1\,B\,@E} = @\frac{kT}{q}\ln^{\Gamma}\frac{g}{R_1 I_s} \qquad\text{-----------------------(15)}$$

The base voltage V_B of Q_2 is

$$V_B = \frac{R}{R2 + R_{TC}}\,V_i$$

The voltage at the emitter of Q_2 is

$$V_{Q2B@E} = V_B + V_{Q2E@B}$$

Or

$$V_{Q2B@E} = \frac{R}{R_2 + R_{TC}}\,V_i\ @\frac{kT}{q}\ln\frac{V}{R_1 I_s} \qquad\text{-------------------(16)}$$

But the emitter voltage of Q_2 is V_A, that is

$$V_A = V_{Q2B\text{-}E}$$

Or,
$$@\frac{kT}{q}\ln\frac{V}{R_1 I_s} = b\frac{R}{R_2 + R_{TC}}\,c\,V_i\ @\frac{kT}{q}\ln\frac{V}{R_1 I_s} \qquad\text{----------------(17)}$$

Or,
$$\frac{R}{R_2 + R_{TC}}\,V_i = @\frac{kT}{q}\ln\frac{V}{R_1 I_s}\ @\ln\frac{V}{R_1 I_s}$$

Or
$$@\frac{q}{kT}\frac{R}{R_2 + R_{TC}}\,V_i = \ln\frac{V}{V_{ref}} \qquad\text{------------------(18)}$$

Changing the natural log i.e., ln to $\log_{10}$ using eqn(6) we get

$$@0.4343^{d}\frac{q}{kT}\,j\,\frac{R}{R_2 + R_{TC}}\,V_i = 0.4343\,B\,\ln\frac{V}{V_{ref}}$$

Or $@K.V_i = \log_{10} j\ \dfrac{\overline{K''}}{V_{ref}} k$

Or $\dfrac{\overline{K''}}{V_{ref}} = 10^{@k.V_i}$

Or $V_o = V_{ref}[10^{@k.V_i}]$

Where $K' = 0.4343 \dfrac{d}{kT}\ \overline{\dfrac{e''}{j}}\ \overline{\dfrac{R}{R_2 + R_{TC}}} k$

Hence an increase of input by one volt causes the output to decrease by a decade.

Comparator

To obtain for better performance, we shall also look at integrated designed specifically as comparators and converters. A comparator as its name implies, compares a signal voltage on one input of an op-amp with a known voltage called a reference voltage on the other input. Comparators are used in circuits such as,

Digital Interfacing

Schmitt Trigger

Discriminator

Voltage level detector and oscillators

1. Non-inverting Comparator:
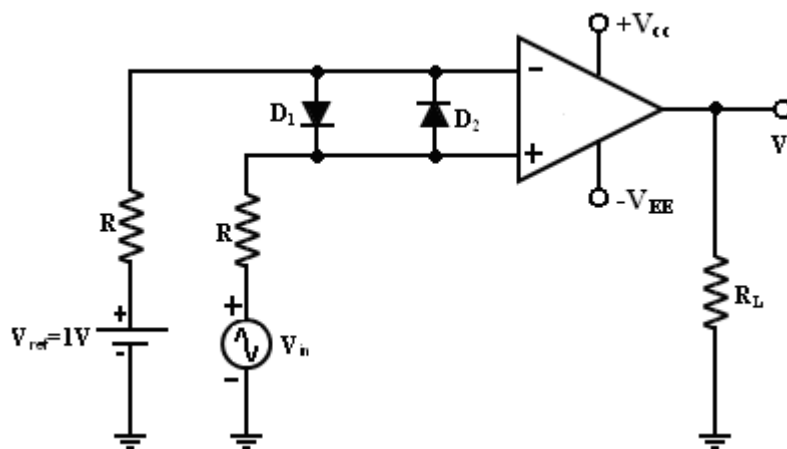
A fixed reference voltage Vref of 1 V is applied to the negative terminal and time varying signal voltage Vin is applied tot the positive terminal.When Vin is less than Vref the

output becomes V_0 at $-Vsat$ [Vin < Vref $=> V_0$ (-Vsat)]. When Vin is greater than Vref, the (+) input becomes positive, the V_0 goes to $+Vsat$. [Vin > Vref $=> V_0$ (+Vsat)]. Thus the V_0 changes from one saturation level to another. The diodes D_1 and D_2 protects the op-amp from damage due to the excessive input voltage Vin. Because of these diodes, the difference input voltage Vid of the op-amp diodes are called clamp diodes. The resistance R in series with Vin is used to limit the current through D_1 and D_2. To reduce offset problems, a resistance Rcomp = R is connected between the (-ve) input and Vref.

Input and Output Waveforms:

If Vref = −Ve

Vin > Vref

Vin < Vref
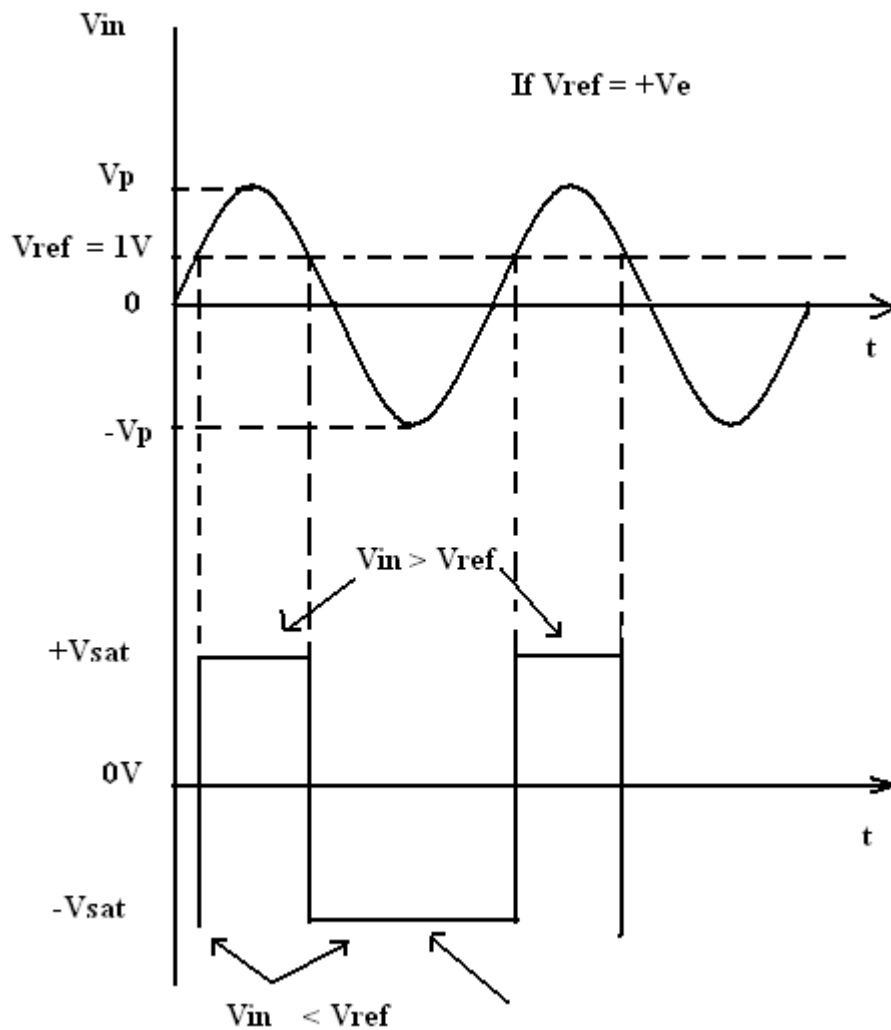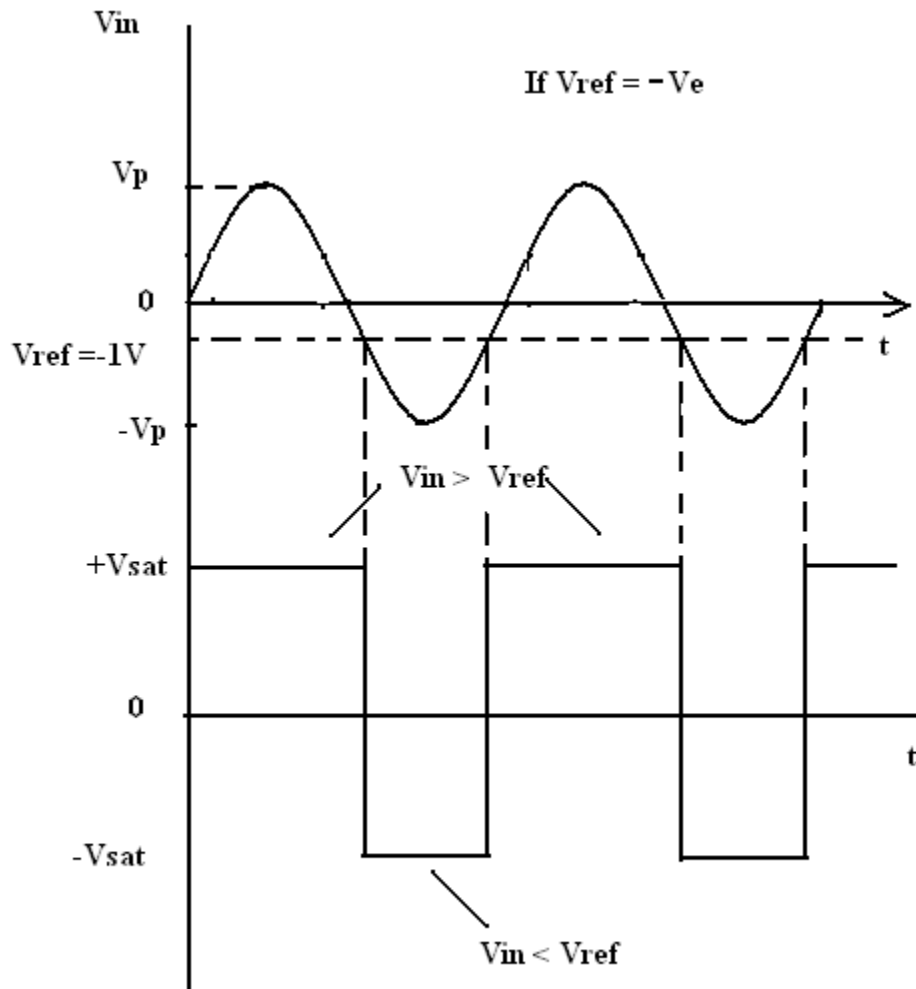
2. Inverting Comparator:
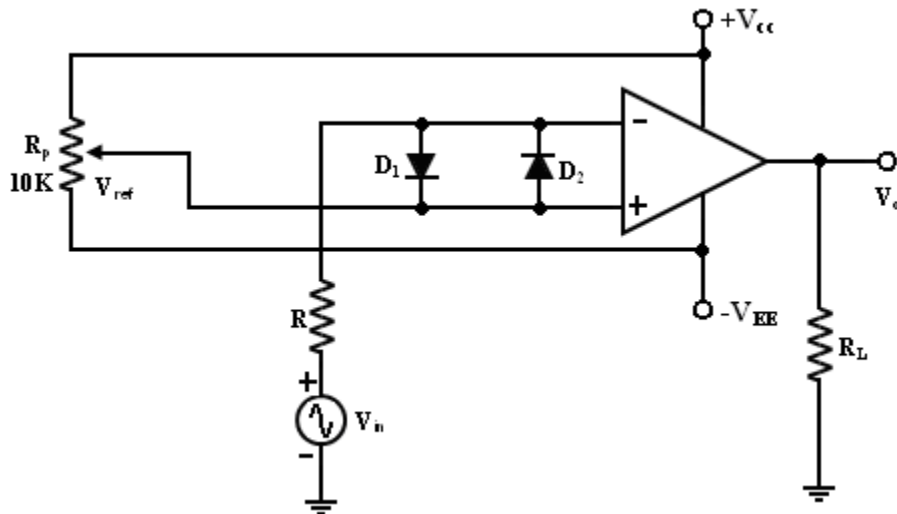
This fig shows an inverting comparator in which the reference voltage Vref is applied to the (+) input terminal and Vin is applied to the (-) input terminal. In this circuit Vref is obtained by using a

10K potentiometer that forms a voltage divider with dc supply volt +Vcc and -1 and the wiper connected to the input. As the wiper is moved towards +Vcc, Vref becomes more positive. Thus a Vref of a desired amplitude and polarity can be obtained by simply adjusting the 10k potentiometer.
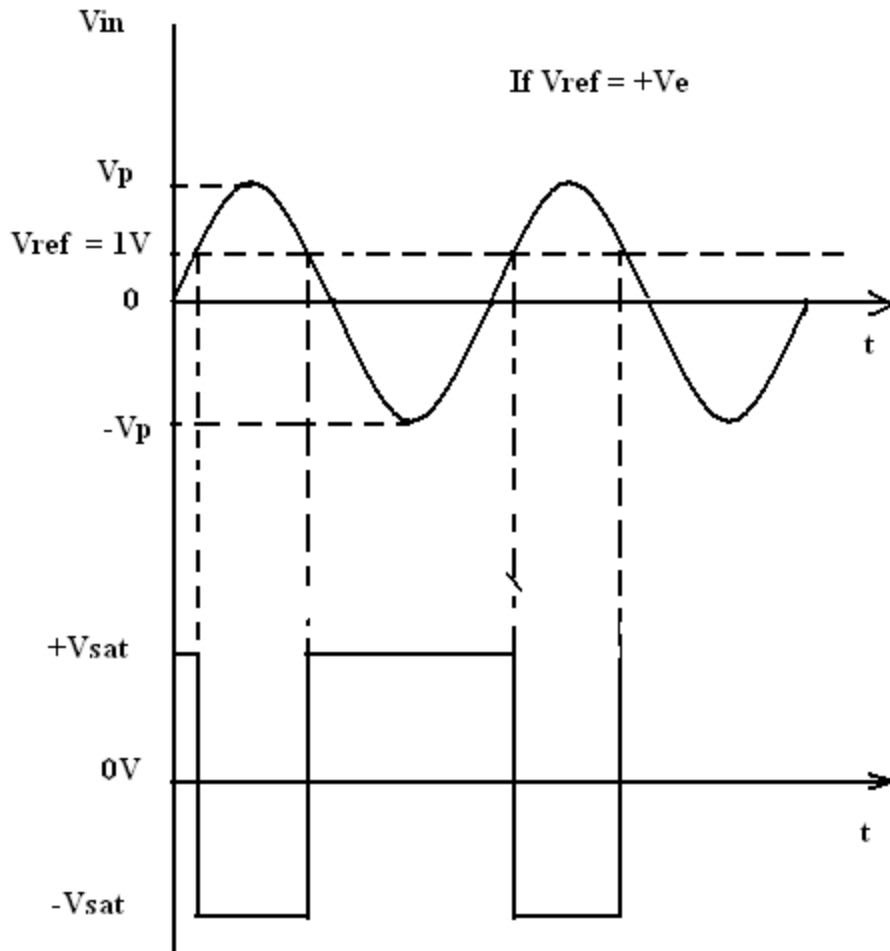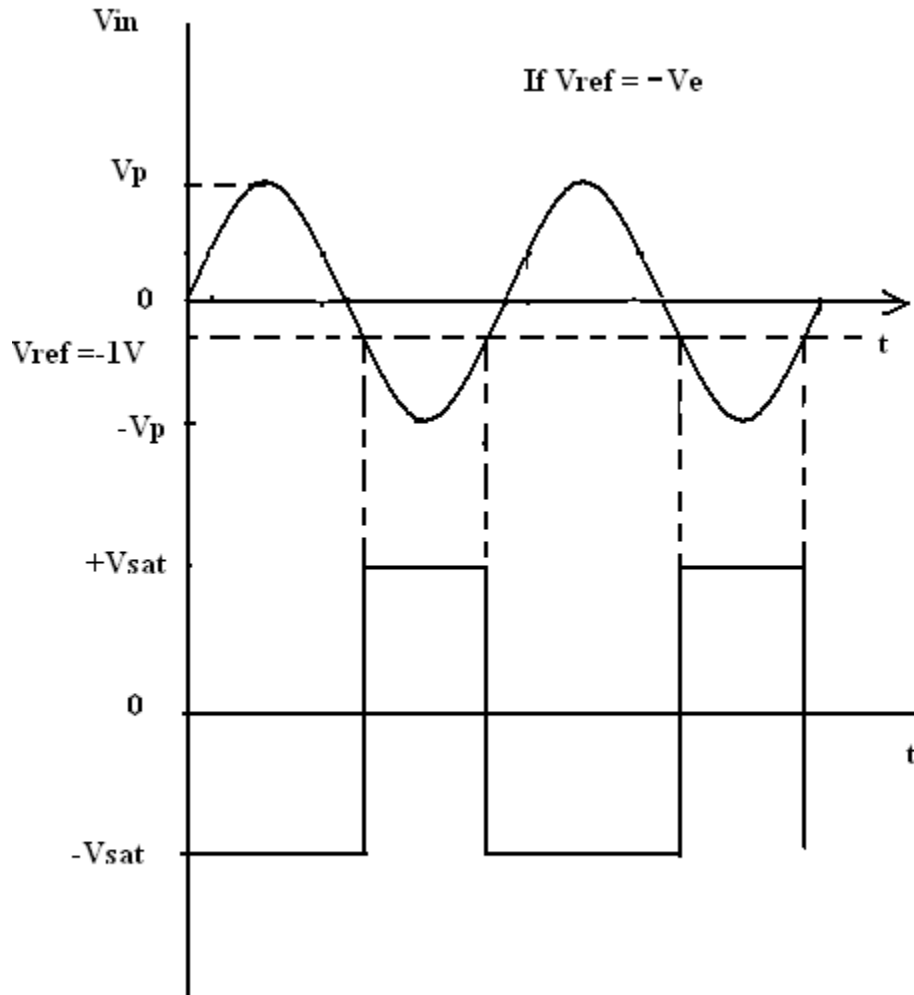
3. Zero Crossing Detector: [Sine wave to Square wave converter]
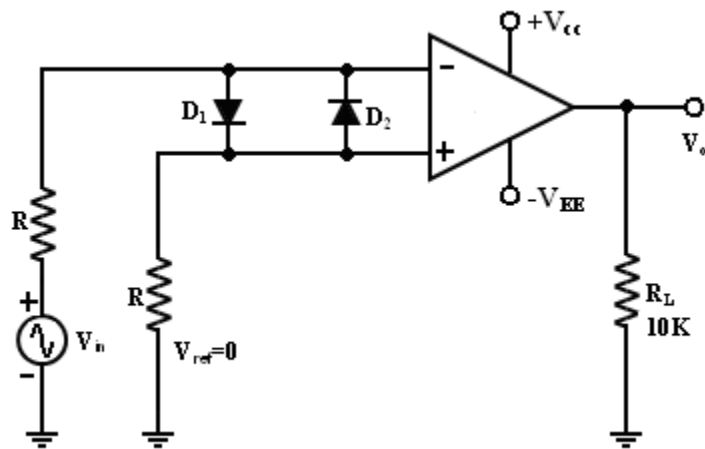
One of the application of comparator is the zero crossing detector or "sine wave to Square wave Converter". The basic comparator can be used as a zero crossing detector by setting Vref is set to Zero. (Vref =0V).

This Fig shows when in what direction an input signal Vin crosses zero volts. (i.e) the o/p V_0 is driven into negative saturation when the input the signal Vin passes through zero in positive direction. Similarly, when Vin passes through Zero in negative direction the output V_0 switches and saturates positively.
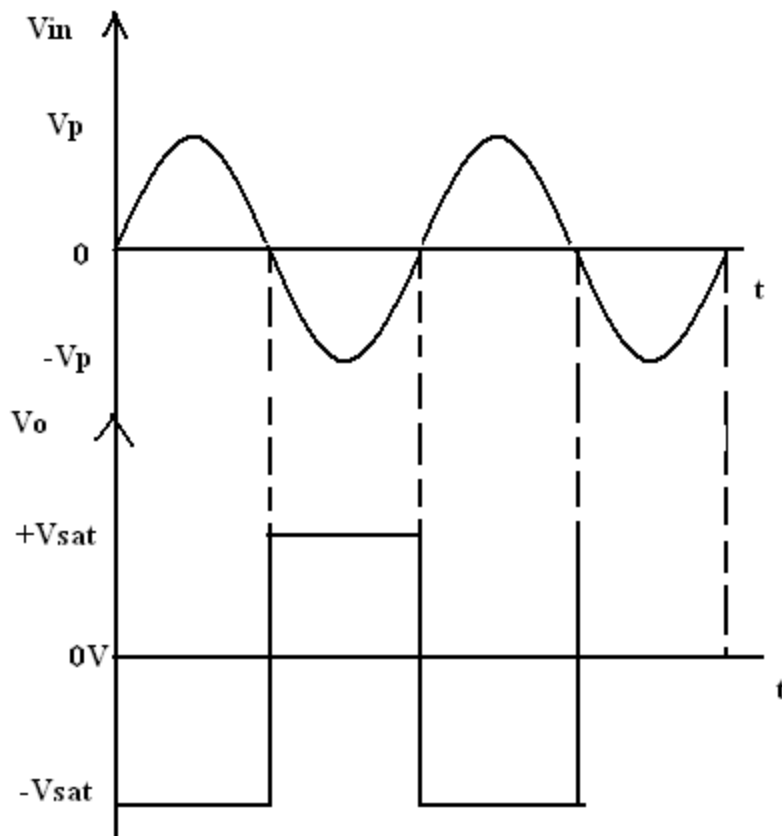
Drawbacks of Zero- crossing detector:

In some applications, the input Vin may be a slowly changing waveform, (i.e) a low frequency signal. It will take Vin more time to cross 0V, therefore V_0 may not switch quickly from one saturation voltage to the other. Because of the noise at the op-amp's input terminals the output V_0 may fluctuate between 2 saturations voltages +Vsat and −Vsat. Both of these problems can be cured with the use of regenerative or positive feedback that cause the output V_0 to change faster and eliminate any false output transitions due to noise signals at the input. Inverting comparator with positive feedback . This is known as "Schmitt Trigger".

Schmitt Trigger: [Square Circuit]
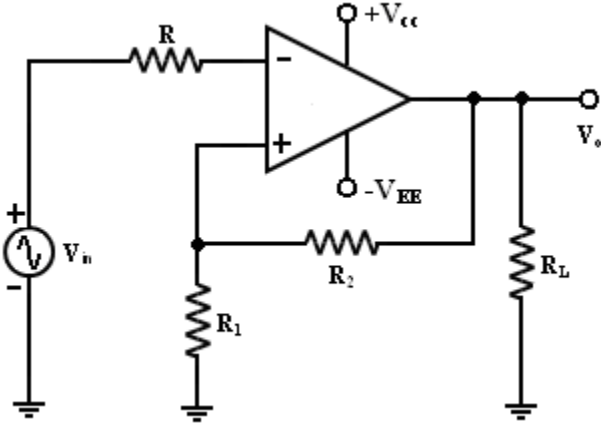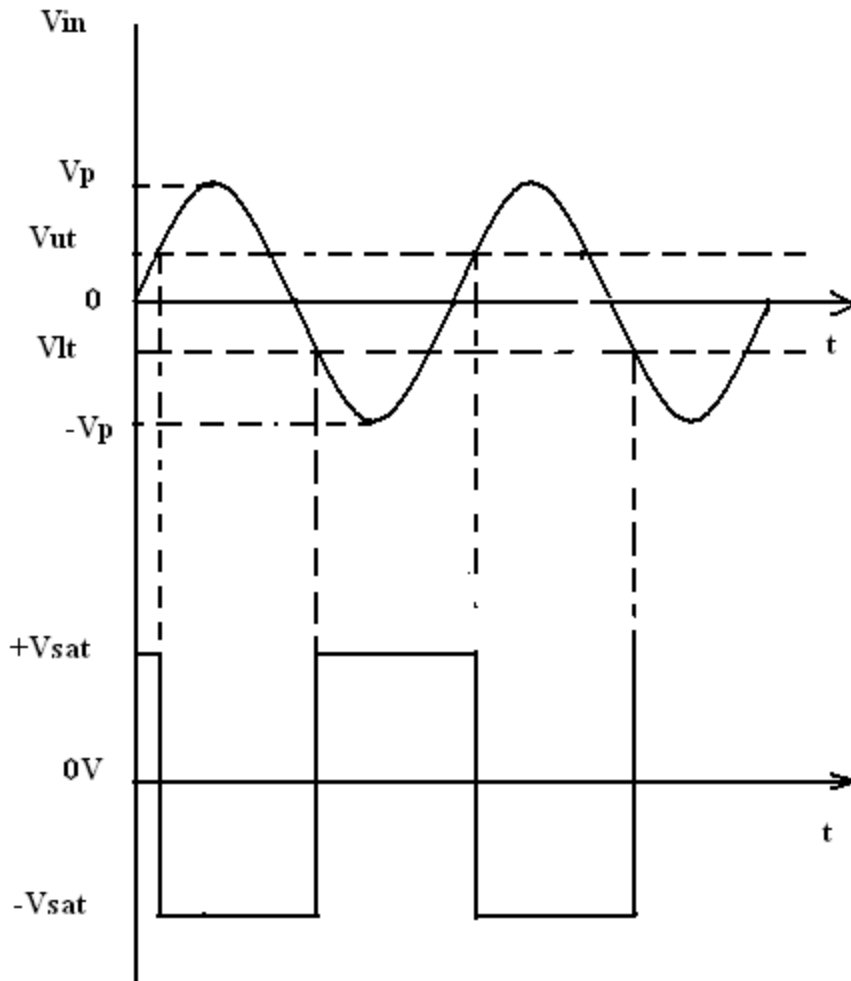
This circuit converts an irregular shaped waveform to a square wave or pulse. The circuit is known as Schmitt Trigger or squaring circuit. The input voltage Vin triggers (changes the state of) the o/p V_0 every time it exceeds certain voltage levels called the upper threshold Vut and lower threshold voltage. These threshold voltages are obtained by using theh voltage divider $R_1 - R_2$, where the voltage across R_1 is feedback to the (+) input. The voltage across R_1 is variable reference threshold voltage that depends on the value of the output voltage. When $V_0 = +$Vsat, the voltage across R_1 is called "upper threshold" voltage Vut. The input voltage Vin must be more positive than Vut in order to cause the output V_0 to switch from +Vsat to −Vsat. As long as Vin <

Vut , V_0 is at +Vsat, using voltage divider rule, $V_{ut} = \dfrac{R}{R_1 + R_2} + V_{sat}$

Similarly, when $V_0 = -Vsat$, the voltage across R_1 is called lower threshold voltage V_{lt}. the vin must be more negative than V_{lt} in order to cause V_0 to switch from $-Vsat$ to $+Vsat$. In other words, for

Vin > V_{lt}, V_0 is at $-Vsat$. V_{lt} is given by the following eqn. $V_{lt} = \dfrac{R_?^O}{R_1 + R_2} @V_{sat}^C /$

Thus, if the threshold voltages Vut and Vlt are made larger than the input noise voltages, the positive feedback will eliminate the false o/p transitions. Also the positive feedback, because of its regenerative action, will make V_0 switch faster between $+Vsat$ and $-Vsat$. Resistance Rcomp ^{L} $R_1 \parallel R_2$ is used to minimize the offset problems. The comparator with positive feedback is said to exhibit hysteresis, a dead band condition. (i.e) when the input of the comparator exceeds Vut its output switches from $+Vsat$ to $-Vsat$ and reverts to its original state, $+Vsat$ when the input goes below Vlt. The hysteresis voltage is equal to the difference between Vut and Vlt. Therefore

Vref = Vut – Vlt

Vref = R_1


   $R_1 + R_2$ [+Vsat -(-Vsat)]

Precision Rectifier:

The signal processing applications with very low voltage, current and power levels require rectifier circuits. The ordinary diodes cannot rectify voltages below the cut-in-voltage of the diode. A circuit which can act as an ideal diode or precision signal – processing rectifier circuit for rectifying voltages which are below the level of cut-in voltage of the diode can be designed by placing the diode in the feedback loop of an op-amp.

Precision diodes:

Figure shows the arrangement of a precision diode. It is a single diode arrangement and functions as a non-inverting precision half – wave rectifier circuit. If V_1 in the circuit of figure is positive, the op-amp output V_{OA} also becomes positive. Then the closed loop condition is achieved for the op-amp and the output voltage $V_0 = V_i$. when $V_i < 0$, the voltage V_{0A} becomes negative and the diode is reverse biased. The loop is then broken and the output $V_0 = 0$.
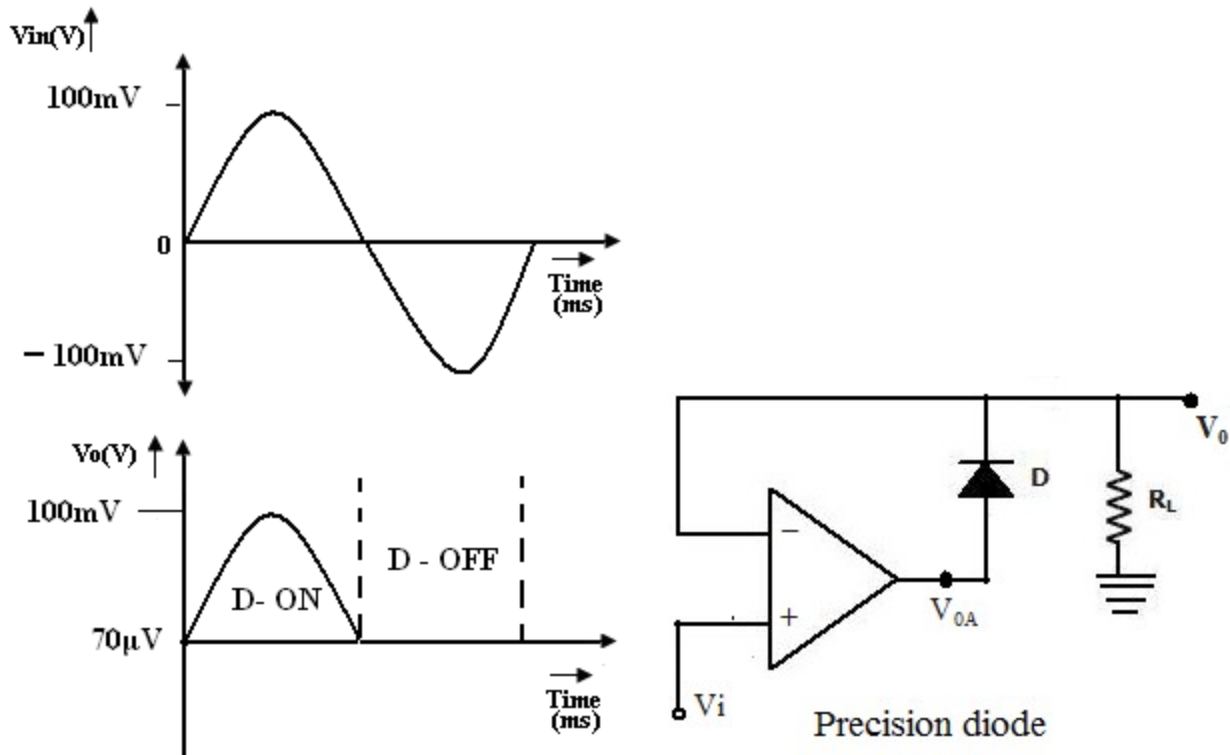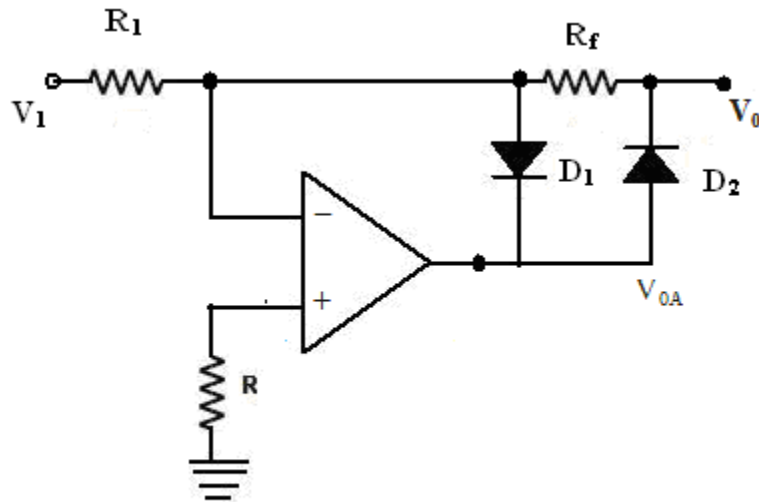
Input and Output Waveform

Consider the open loop gain A_{OL} of the op-amp is approximately 10^4 and the cut-in voltage V_γ for silicon diode is $\approx 0.7V$. When the input voltage $V_i > V_\gamma / A_{OL}$, the output of the op-amp V_{OA} exceeds V_γ and the diode D conducts. Then the circuit acts like a voltage follower for input voltage level $V_i > V_\gamma / A_{OL}$,(i.e. when $V_i > 0.7/10^4 = 70\mu V$), and the output voltage V_0 follows the input voltage during the positive half cycle for input voltages higher than $70\mu V$ as shown in figure. When V_i is negative or less than V_γ / A_{OL} , the output of op-amp V_{OA} becomes negative, and the diode becomes reverse biased. The loop is then broken, and the op-amp swings down to negative saturation. However, the output terminal is now isolated from both the input signal and the output of the op-amp terminal thus $V_0 = 0$. No current is then delivered to the load R_L except for the small bias current of the op-amp and the reverse saturation current of the diode.

This circuit is an example of a non-linear circuit, in which linear operation is achieved over the remaining region ($V_i < 0$). Since the output swings to negative saturation level when $V_i < 0$, the circuit is basically of saturating form. Thus the frequency response is also limited. The precision diodes are used in half wave rectifier, Full-wave rectifier, peak value detector, clipper and clamper circuits.

It can be observed that the precision diode as shown in figure operated in the first quadrant with V_i > 0 and V_0 > 0. The operation in third quadrant can be achieved by connecting the diode in reverse direction.

Half – wave Rectifier:

A non-saturating half wave precision rectifier circuit is shown in figure. When V_i > 0V , the voltage at the inverting input becomes positive, forcing the output V_{OA} to go negative. This results in forward biasing the diode D_1 and the op-amp output drops only by $\approx$ 0.7V below the inverting input voltage. Diode D_2 becomes reverse biased. The output voltage V_0 is zero when the input is positive. When V_i > 0, the op-amp output V_{OA} becomes positive, forward biasing the diode D_2 and reverse biasing the diode D_1 . The circuit then acts like an inverting amplifier circuit with a non-linear diode in the forward path. The gain of the circuit is unity when $R_f = R_i$.

Non - Saturating half - wave precision rectifier circuit
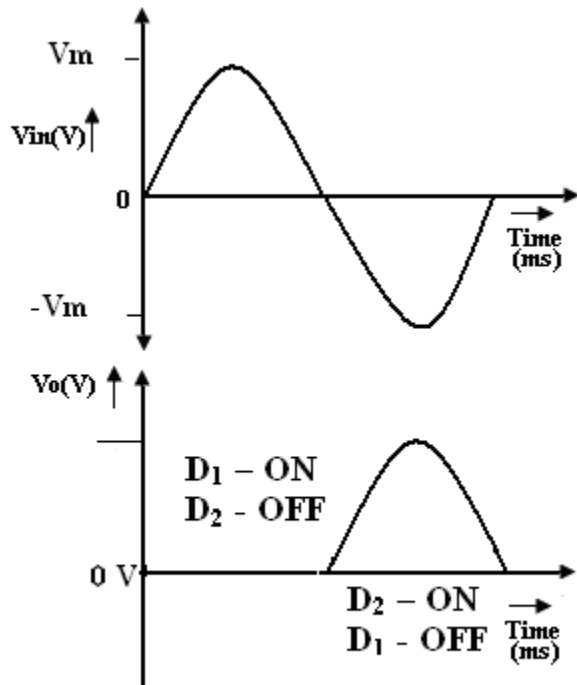
Input and Output Waveforms

The circuit operation can mathematically be expressed as

$$V_0 = 0 \ when \ V_i > 0$$

and

$$V_0 = \frac{R_f}{R_i} V_i \ for \ V_i < 0$$

The voltage V_{OA} at the op @amp output is

$$V_{OA} = 0.7 \ for \ V_i > 0V$$

and

$$V_{OA} = \frac{R_f}{R_i} V_i + 0.7V \ for \ V_i < 0V \ A$$

The input and output waveforms are shown in figure. The op-amp shown in the circuit must be a high speed op-amp. This accommodates the abrupt changes in the value of V_{OA} when V_i changes sign and improves the frequency response characteristics of the circuit.

The advantages of half wave rectifier are it is a precision half wave rectifier and it is a non saturating one.

The inverting characteristics of the output V_0 can be circumvented by the use of an additional inversion for achieving a positive output.

Full wave Rectifier:

The Full wave Rectifier circuit commonly used an absolute value circuit is shown in figure. The first part of the total circuit is a half wave rectifier circuit considered earlier in figure. The second part of the circuit is an inverting.

Active Non - saturating Full - wave Rectifier circuit
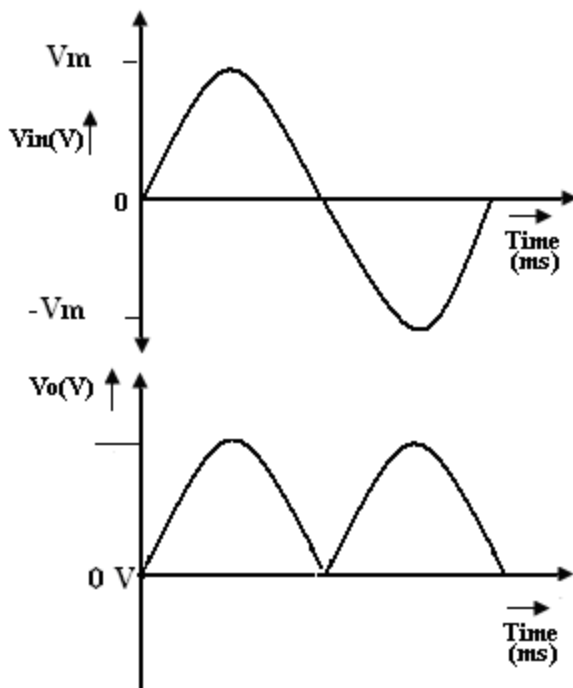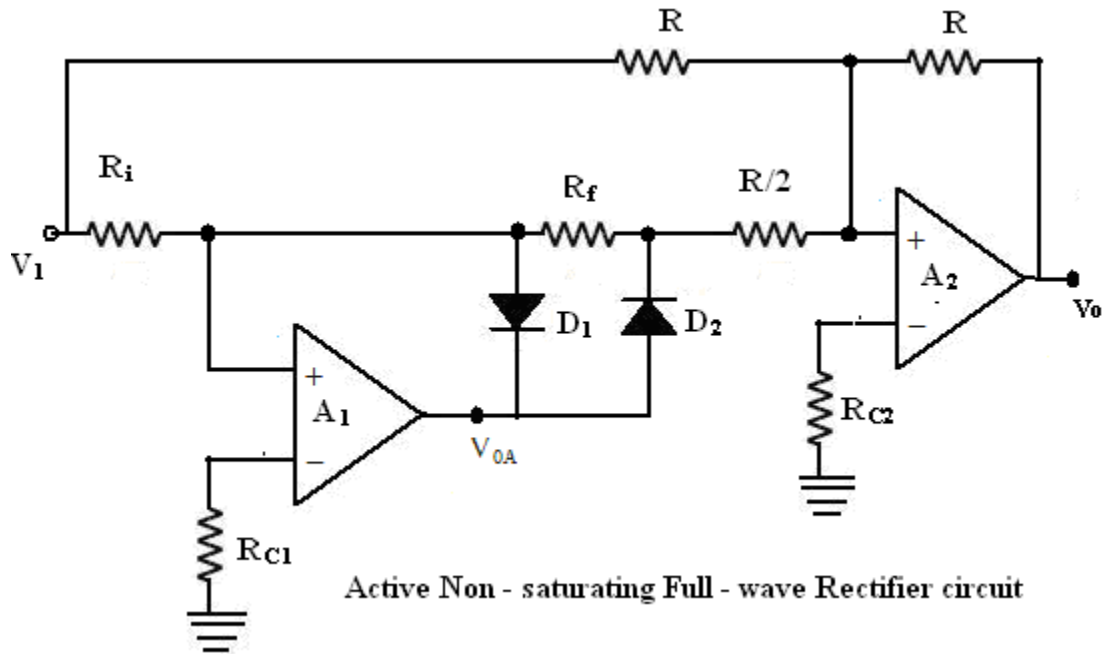
Input and Output Waveforms

For positive input voltage $V_i > 0V$ and assuming that $R_F = R_i = R$, the output voltage $V_{OA} = V_i$. The voltage V_0 appears as (-) input to the summing op-amp circuit formed by A_2, The gain for the input V'_0 is $R/(R/2)$, as shown in figure. The input V_i also appears as an input to the summing amplifier. Then, the net output is $V_0 = -V_i - 2V'_0$

$$= -V_i - 2(-V_i) = V_i$$

Since $V_i > 0V$, V'_0 will be positive, with its input output characteristics in first quadrant. For negative input $V_i < 0V$, the output V'_0 of the first part of rectifier circuit is zero. Thus, one input of the summing circuit has a value of zero. However, V_i is also applied as an input to the summer circuit formed by the op-amp A_2. The gain for this input id $(-R/R) = -1$, and hence the output is $V_0 = -V_i$. Since V_i is negative, v_0 will be inverted and will thus be positive. This corresponds to the second quadrant of the circuit.

To summarize the operation of the circuit,

$V_0 = V_i$ when $V_i < 0V$ and $V_0 = V_i$ for $V_i > 0V$, and hence $V_0 = |V_i|$

It can be observed that this circuit is of non-saturating form. The input and output waveforms are shown in the figure.

Peak detector:

Square, Triangular, Sawtooth and pulse waves are typical examples of non-sinusoidal waveforms. A conventional ac voltmeter cannot be used to measure these sinusoidal waveforms because it is designed to measure the rms value of the pure sine wave. One possible solution to this problem is to measure the peak values of the non-sinusoidal waveforms. Peak detector measures the +ve peak value of the square wave input.
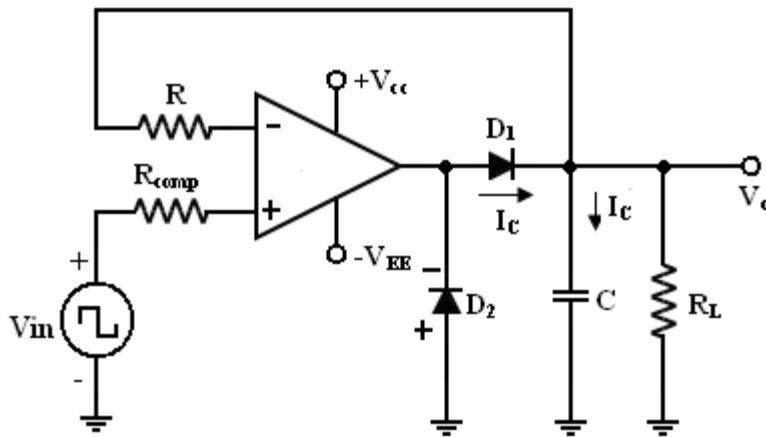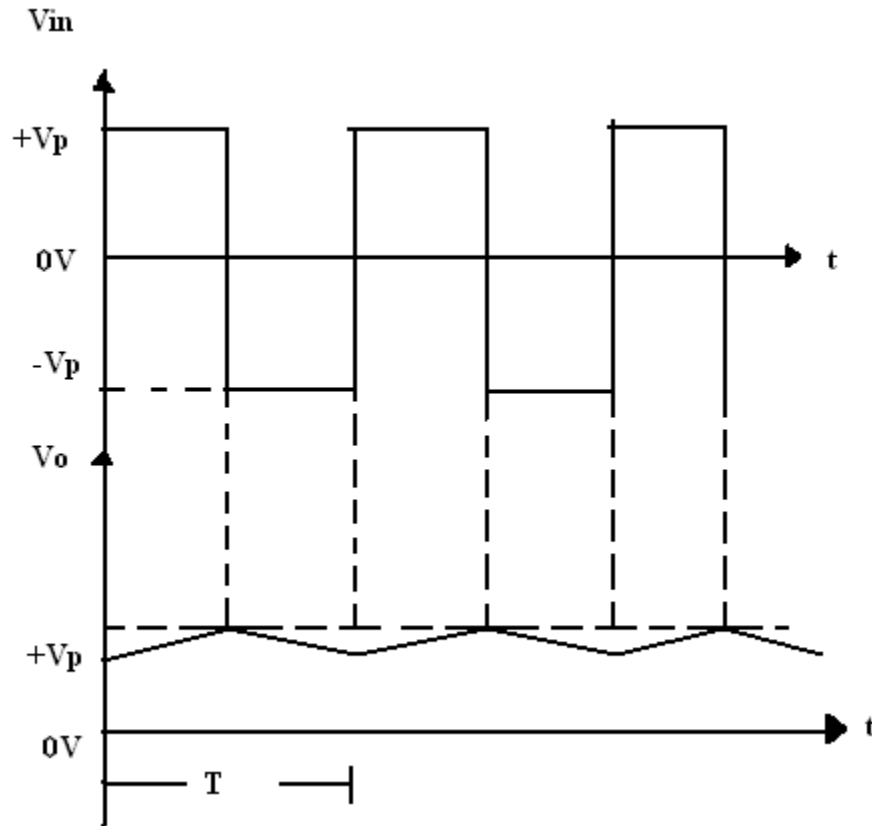
i) During the positive half cycle of Vin:

       the o/p of the op-amp drives D_1 on. (Forward biased)

       Charging capacitor C to the positive peak value V_p of the input volt Vin.

ii) During the negative half cycle of Vin:

       D_1 is reverse biased and voltage across C is retained. The only discharge path for C is through R_L since the input bias I_B is negligible.

For proper operation of the circuit, the charging time constant (CR_d) and discharging time constant (CR_L) must satisfy the following condition.

$CR_d <= T/10$ -----(1)

Where R_d = Resistance of the forward-biased diode.

    T = time period of the input waveform.

$CR_L >= 10T$ -----(2)

Where R_L = load resistor. If R_L is very small so that eqn (2) cannot be satisfied. Use a (buffer) voltage follower circuit between capacitor C and R_L load resistor.

R = is used to protect the op-amp against the excessive discharge currents.

Rcomp = minimizes the offset problems caused by input current

D_2 = conducts during the –ve half cycle of Vin and prevents the op-amp from going into negative saturation.

Note: -ve peak of the input signal can be detected simply by reversing diode D_1 and D_2.

Clippers and Clampers:

Waveshaping circuits are commonly used in digital computers and communication such as TV and FM receiver. Waveshaping technique include clipping and clamping. In op-amp clipper circuits a rectifier diode may be used to clip off a certain portion of the input signal to obtain a desired o/p waveform. The diode works as an ideal diode (switch) because when on -> the voltage drop across the diode is divided by the open loop gain of the op-amp. When off(reverse biased) -> the diode is an open circuit.

In an op-amp clamper circuits, however a predetermined dc level is deliberately inserted in the o/p volt. For this reason, the clamper is sometimes called a dc inverter.

**Positive and Negative Clipper:**

Positive Clipper:

A Circuit that removes positive parts of the input signal can be formed by using an op-amp with a rectifier diode. The clipping level is determined by the reference voltage Vref, which should less than the i/p range of the op-amp (Vref < Vin). The Output voltage has the portions of the positive half cycles above Vref clipped off.

The circuit works as follows:

During the positive half cycle of the input, the diode D_1 conducts only until Vin = Vref. This happens because when Vin <Vref, the output volts V_0' of the op-amp becomes negative to device D_1 into conduction when D_1 coonducts it closes feedback loop and op-amp operates as a voltage follower. (i.e) Output V_0 follows input until Vin = Vref.

When Vin > Vref => the V'_0 becomes +ve to derive D_1 into off. It open the feedback loop and op-amp operates open loop. When Vin drops below Vref (Vin<Vref) the o/p of the op-amp V'_0 again becomes –ve to device D_1 into conduction. It closed the f/b. (o/p follows the i/p). Thus diode D_1 is

on for vin<Vref (o/p follows the i/p) and D_1 is off for Vin>Vref. The op-amp alternates between open loop (off) and closed loop operation as the D_1 is turned off and on respectively. For this reason the op-amp used must be high speed and preferably compensated for unity gain.
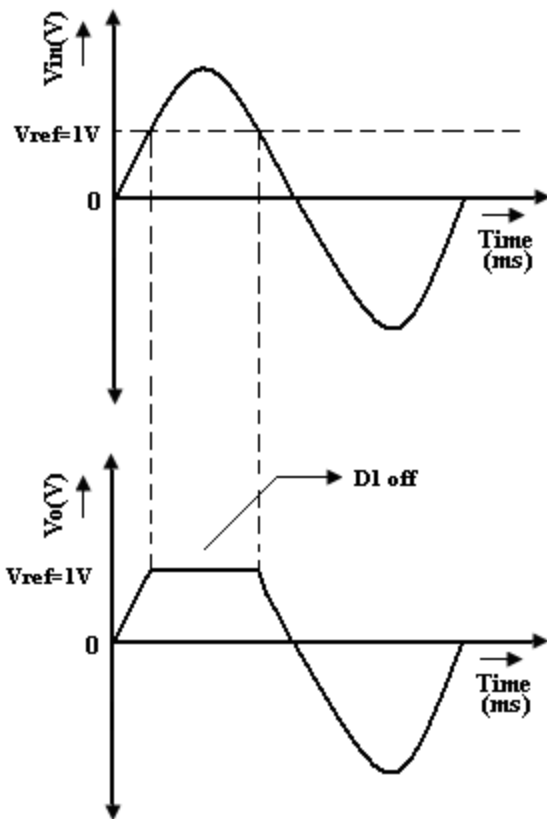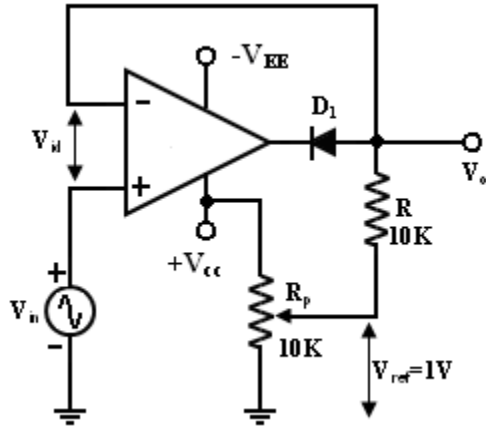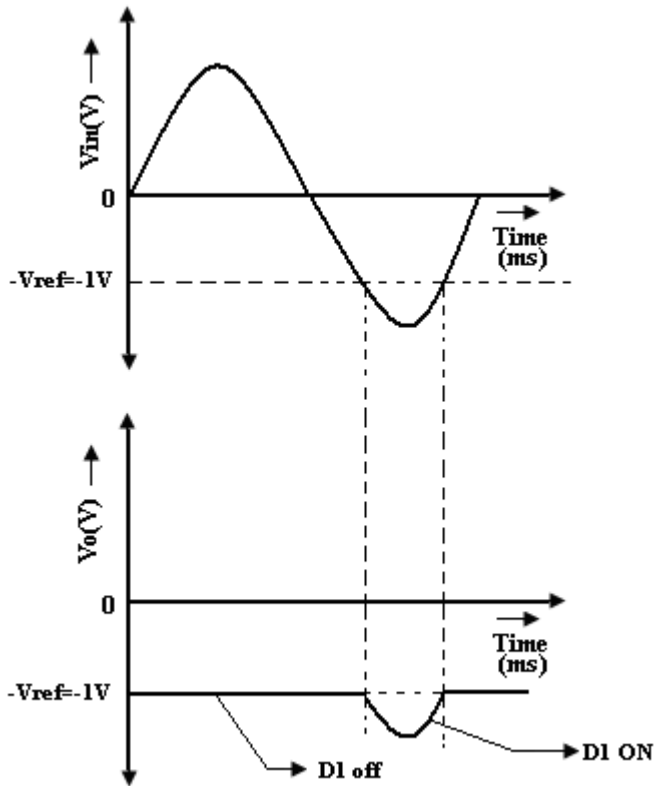
Ex: for high speed op-amp HA 2500, LM310, μA 318. In addition the difference input voltage (Vid=high) is high during the time when the feedback loop is open (D_1 is off) hence an op-amp with a high difference input voltage is necessary to prevent input breakdown. If R_p (pot) is connected to $-V_{EE}$ instead of +Vcc, the ref voltage Vref will be negative (Vref = -ve). This will cause the entire o/p waveform above –Vref to be clipped off.

Negative Clipper:
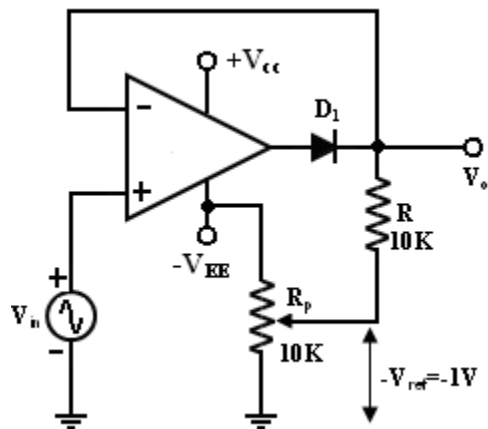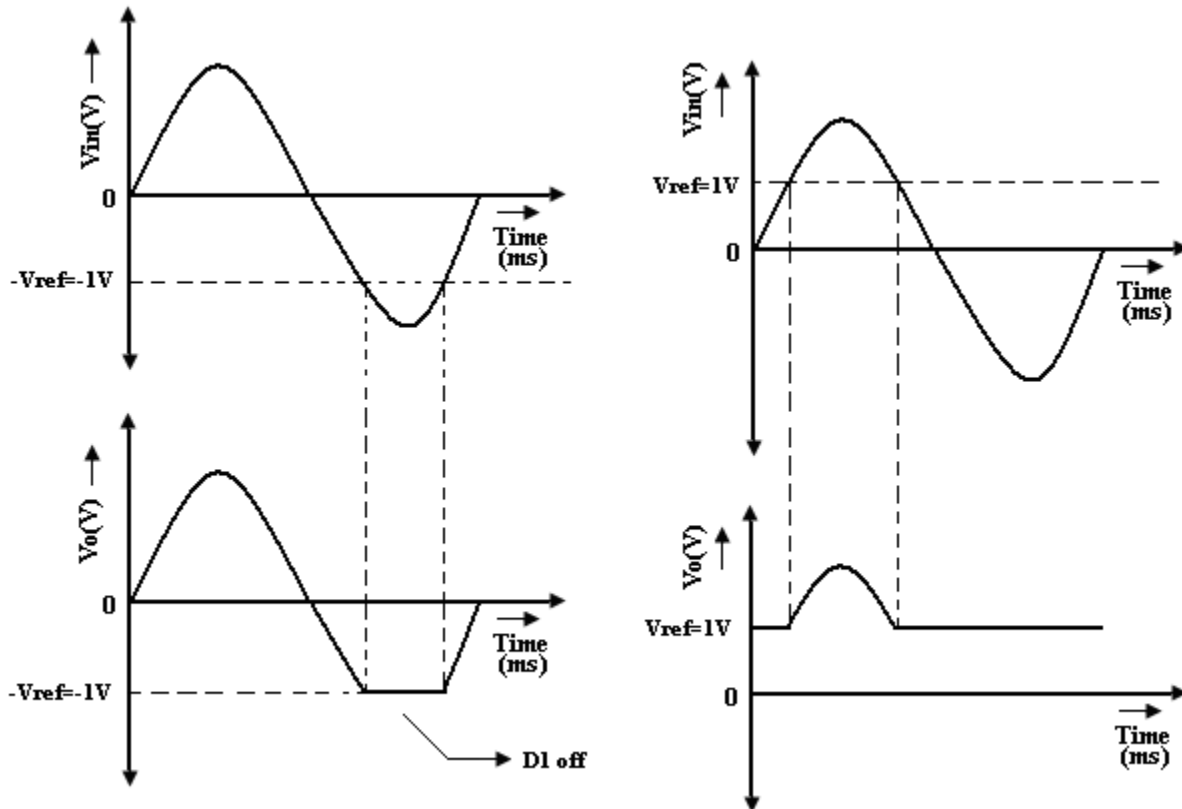
The positive clipper is converted into a −ve clipper by simply reversing diode D_1 and changing the polarity of Vref voltage. The negative clipper -> clips off the −ve parts of the input signal below the reference voltage. Diode D_1 conducts -> when Vin > -Vref and therefore during this period o/p volt V_0 follows the i/p volt Vin. The −Ve portion of the output volt below −Vref is clipped off because (D_1 is off) Vin<-Vref. If −Vref is changed to −Vref by connecting the potentiometer R_p to the +Vcc, the V_0 below +Vref will be clipped off. The diode D_1 must be on for Vin > Vref and off for Vin.

Positive and Negative Clampers:

In clamper circuits a predetermined dc level is added to the output voltage. (or) The output is clamped to a desired dc level.

1. If the clamped dc level is +ve, the clamper is positive clamper
2. If the clamped dc level is −ve, the clamper is negative clamper.

Other equivalent terms used for clamper are dc inserter or restorer. Inverting and Non-Inverting that use this technique.
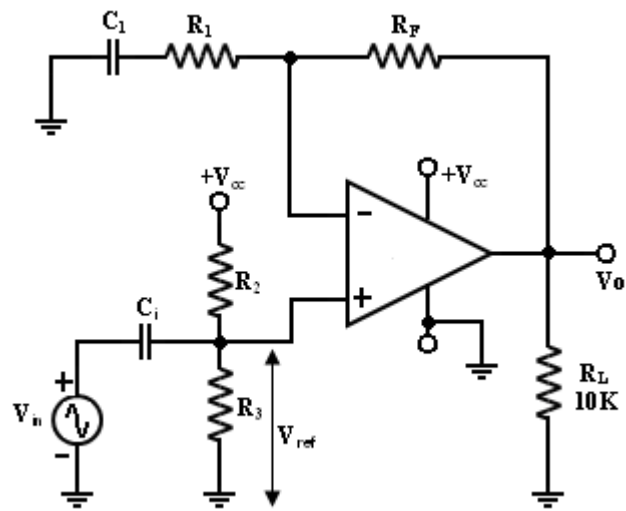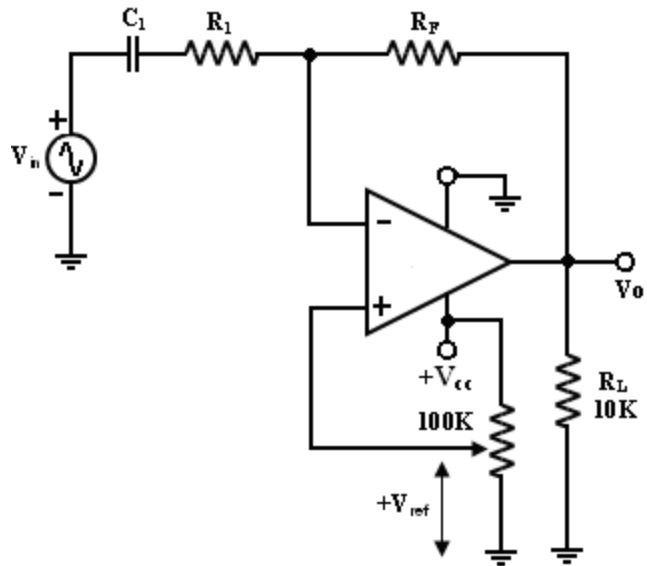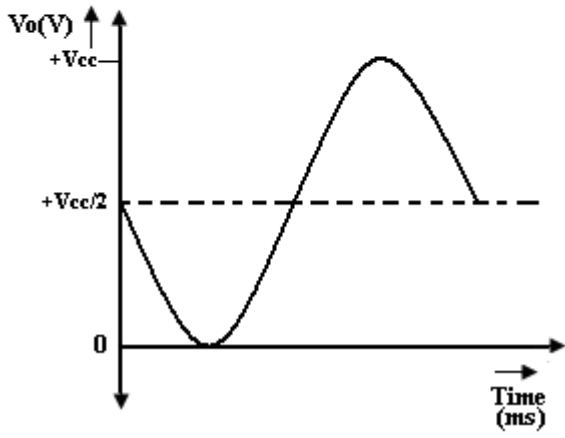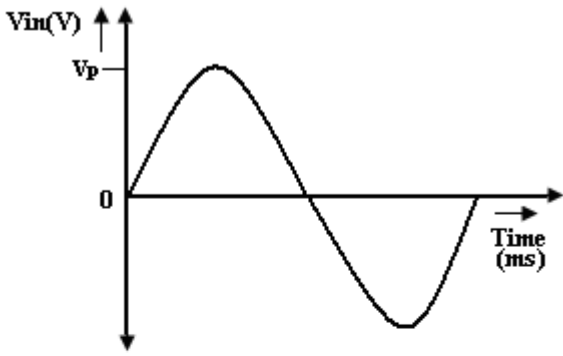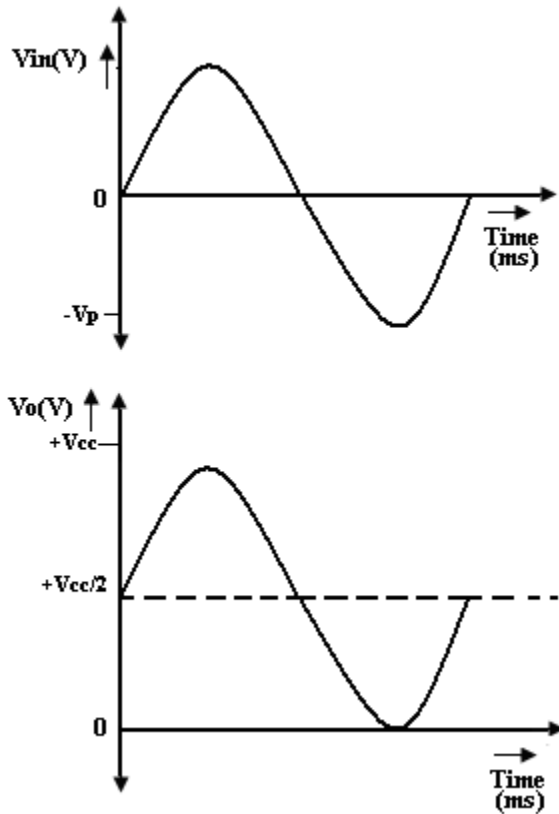
Capacitor:

The Value of the capacitors in these circuits depends on different input rates and pulse widths.

1. In both circuits the dc level added to the o/p voltage is approximately equal to Vcc/2.
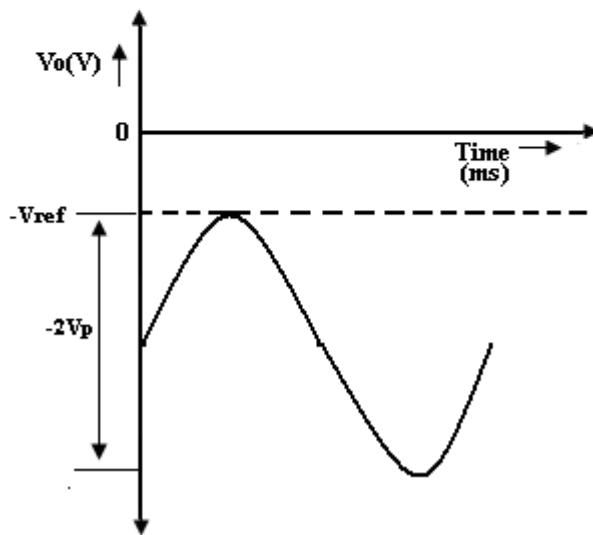2. This +ve fixed dc level is needed to obtain a maximum undistored symmetrical sine wave.

Peak clamper circuit: **Input and output waveform with +Vref:**

Input and Output Waveform with –Vref:

Vin(V)

Vp —

0

Time
(ms)

-Vp —

Vo(V)

0

Time
(ms)

-Vref

-2Vp
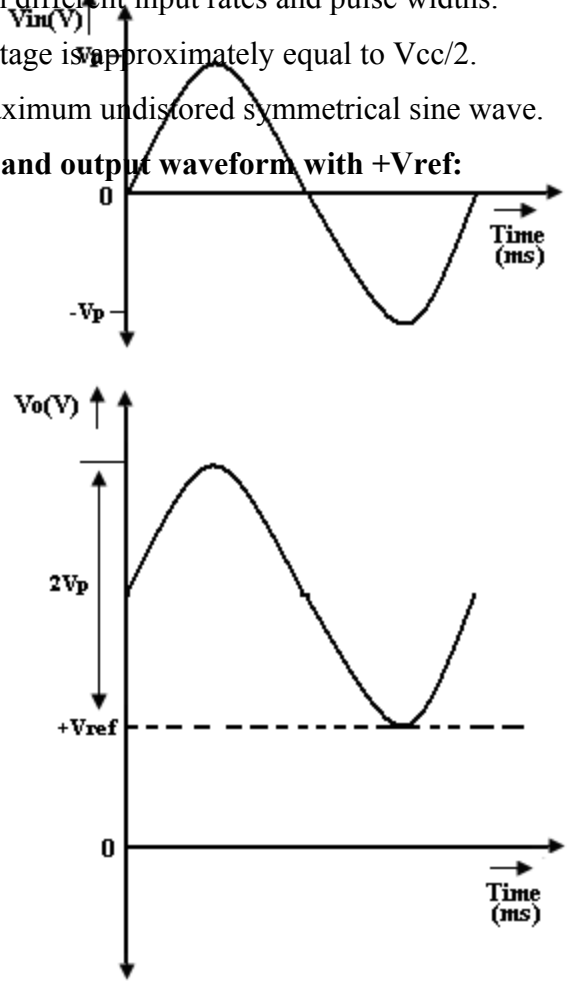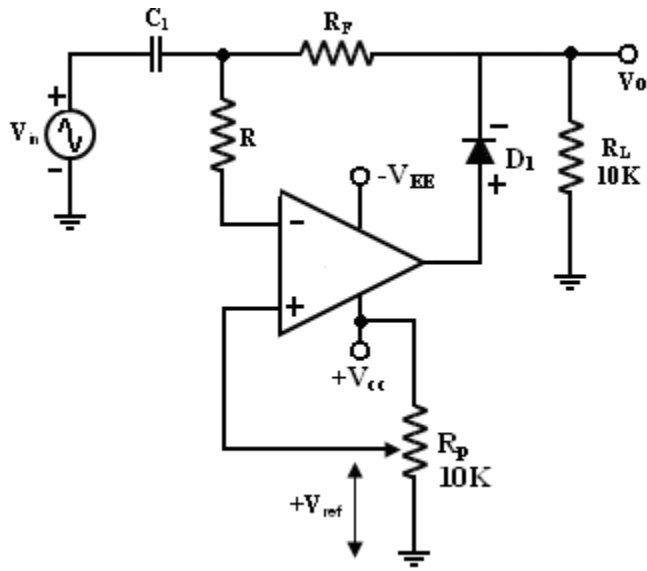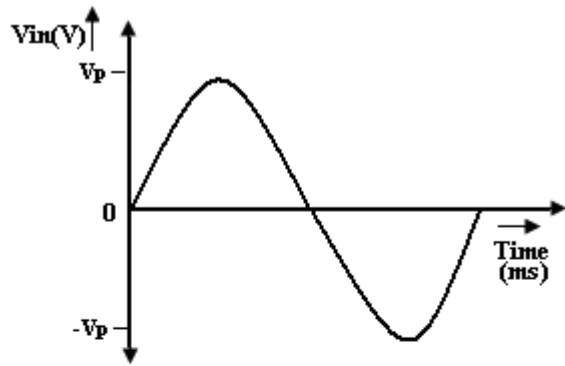
In this circuit, the input waveform peak is clamped at Vref. For this reason, the circuit is called the peak clamper.

First consider the input voltage Vref at the (+) input: since this volt is +ve, V'_0 is also +ve which forward biases D_1. This closed the feedback loop.

Voltage Vin at the (-) input: During its −ve half cycle, diode D_1 conducts, charging c; to the −ve peak value of V_p. During the +ve half cycle, diode D_1 in reverse biased. Since this voltage V_p is in series with the +ve peak volt V_p the o/p volt $V_0 = 2 V_p$. Thus the nett o/p is Vref plus 2 V_p. so the −ve peak of 2 V_p is at Vref. For precision clamping, $C_i R_d \ll T/2$

Where R_d = resistance of diode D_1 when it is forward biased.

T = time period of the input waveform.

Resistor r => is used to protect the op-amp against excessive discharge currents from capacitor C_i especially when the dc supply voltages are switched off. A +ve peak clamping is accomplished by reversing D_1 and using –ve reference voltage (-Vref).

Note:

Inv and Non-Inv clamper – Fixed dc level

Peak clamper – Variable dc level

Active filters:

Another important field of application using op-amp.

Filters and Oscillators:

An electric filter is often a frequency selective circuit that passes a specified band of frequencies and blocks or alternates signal and frequencies outside this band.

Filters may be classified as

1. Analog or digital.
2. Active or passive
3. Audio (AF) or Radio Frequency (RF)

1. Analog or digital filters:

Analog filters are designed to process analog signals, while digital filters process analog signals using digital technique.

2. Active or Passive:

Depending on the type of elements used in their construction, filter may be classified as passive or Active elements used in passive filters are Resistors, capacitors, inductors. Elements used in active filters are transistor, or op-amp.

Active filters offers the following advantages over a passive filters:

1. Gain and Frequency adjustment flexibility:

Since the op-amp is capable of providing a gain, the i/p signal is not attenuated as it is in a passive filter. [Active filter is easier to tune or adjust].

2. No loading problem:

Because of the high input resistance and low o/p resistance of the op-amp, the active filter does not cause loading of the source or load.

3. Cost:

Active filters are more economical than passive filter. This is because of the variety of cheaper op-amps and the absence of inductors.

The most commonly used filters are these:
1. Low pass Filters
2. High pass Filters
3. Band pass filters
4. Band –reject filters
5. All pass filters.

Frequency response of the active filters:
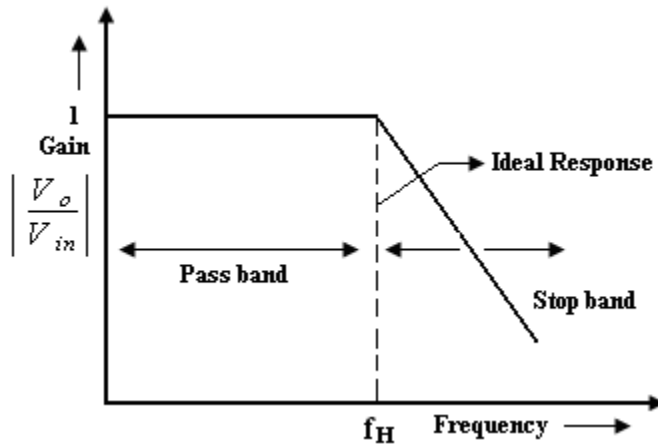
Low pass Filter
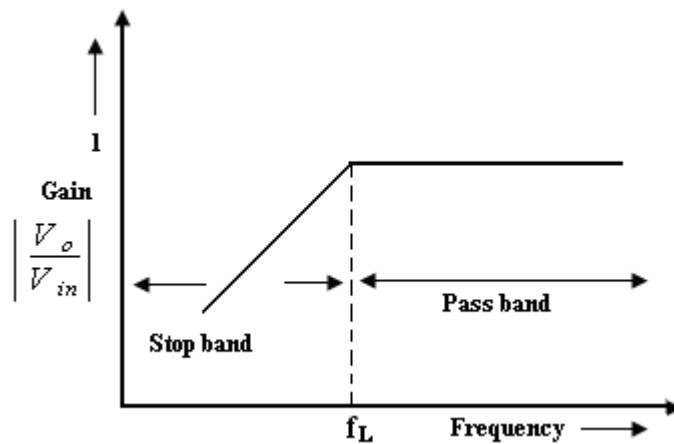
High pass Filter
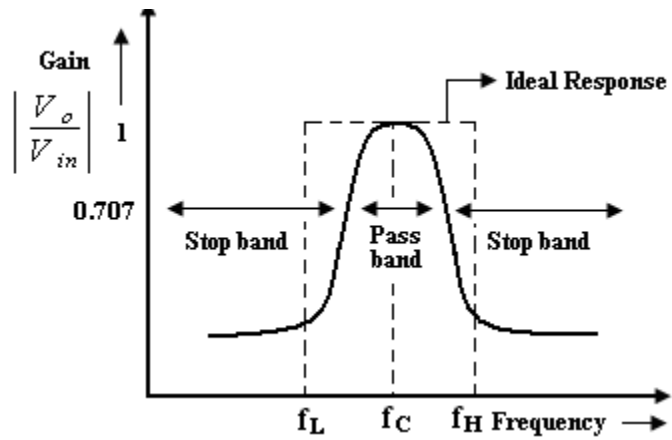
Band Pass Filters
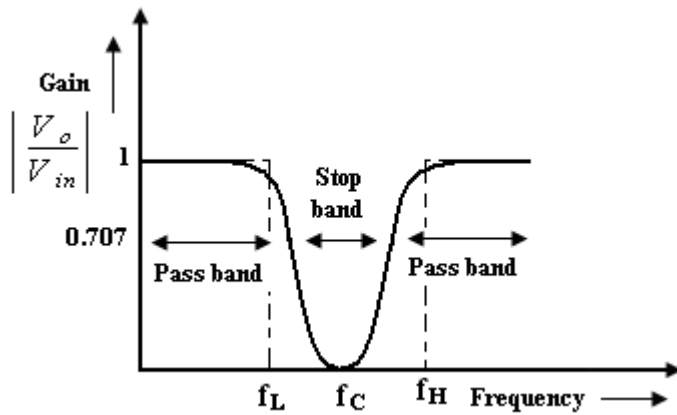
Band Reject

Low pass filters:

1. It has a constant gain from 0 Hz to a high cutoff frequency f_1.
2. At f_H the gain in down by 3db.

3. The frequency between 0hz and f_H are known as the passband frequencies. Where as the range of frequencies those beyond f_H, that are attenuated includes the stopband frequencies.

4. Butterworth, clebyshev and cauer filter are some of the most commonly used practical filters.

5. The key characteristics of the butter worth filter is that it has a flat pass band as well as stop band. For this reason, it is sometimes called a flat-flat filters.

6. Chebyshev filter -> has a ripple pass band & flat stop band.

7. Causer Filter -> has a ripple pass band & ripple stopband. It gives best stopband response among the three.

High pass filter:

High pass filter with a stop band $0 < f < f_L$ and a pass band $f > f_L$

f_L -> low cut off frequency

f -> operating frequency.

Band pass filter:

It has a pass band between 2 cut off frequencies f_H and f_L where $f_H > f_L$ and two, stop bands : $0 < f < f_L$ and $f > f_H$ between the band pass filter (equal to $f_H - f_L$.

Band –reject filter: (Band stop or Band elimination)

It performs exactly opposite to the band pass. It has a band stop between 2 cut-off frequency f_L and f_H and 2 passbands: $0 < f < f_L$ and $f > f_H$

f_C -> center frequency.

Note:

The actual response curves of the filters in the stopband either R or S or both with R in frequencies.

The rate at which the gain of the filter changes in the stopband is determined by the order of the filter.

Ex: 1st order low pass filter the gain rolls off at the rate of 20dB/decade in the stopband. (i.e) for $f > f_H$.

2nd order LPF -> the gain roll off rate is 40dB/decade.

1st order HPF -> the gain Rs at the rate of 20dB (i.e) until $f:f_L$

2nd order HPF -> the gain R_S at the rate of 40dB/decade

First order LPF Butterworth filter:

First order LPF that uses an RC for filtering op-amp is used in the non inverting configuration. Resistor R1 & R_f determine the gain of the filter. According to the voltage –divider rule, the voltage at the non-inverting terminal (across capacitor) C is,

2[nd] order HPF -> the gain R_S at the rate of 40dB/decade

First order LPF Butterworth filter:

First order LPF that uses an RC for filtering op-amp is used in the non inverting configuration. Resistor R1 & R_f determine the gain of the filter. According to the voltage –divider rule, the voltage at the non-inverting terminal (across capacitor) C is,

$$V_1 = \frac{-jX_C}{R - jX_C} Vin \quad @@@@@ \; 1^a a$$
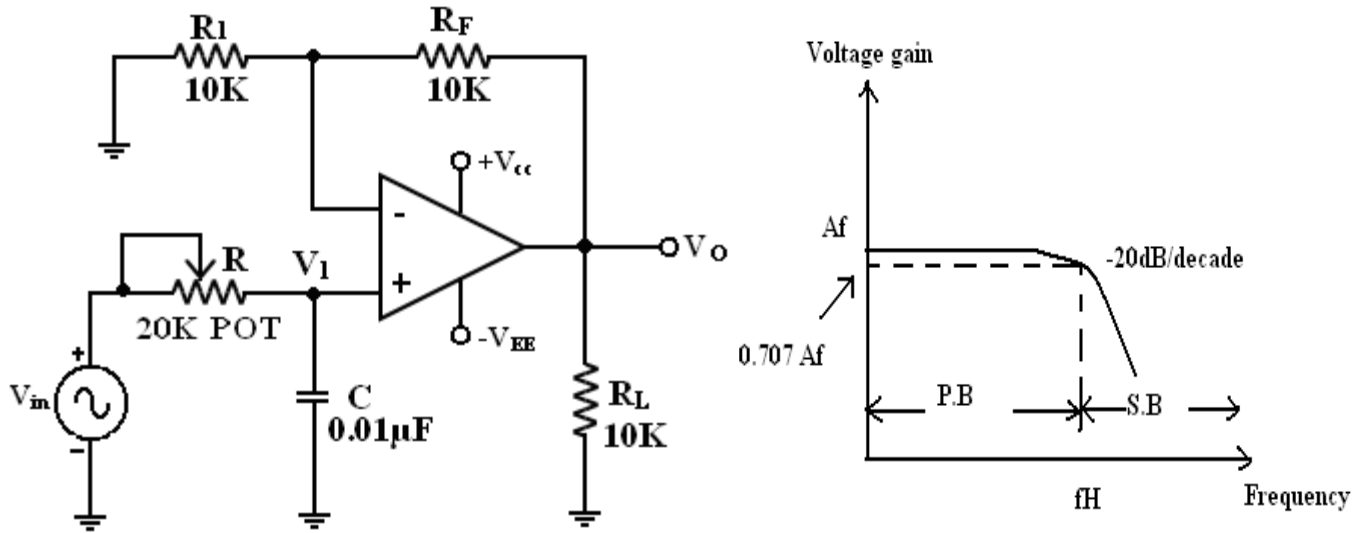
where

$$j = \sqrt{-1} \quad \varepsilon_1 \quad -jX_C = \frac{1}{j2\pi f_C}$$

simplifying eqn $1^a a$ *we get*

$$= \frac{Vin \frac{1}{2\pi f_C}}{R + \frac{1}{2\pi f_c}}$$

$$= \frac{Vin}{1 + j2\pi f RC}$$

Ouptut Voltage, $i.e \; V_0 = A_f \cdot V_1$

$$V_0 = \left[1 + \frac{R_f}{R_1} \right] V_1$$

$$V_0 = \left[1 + \frac{R_f}{R_1} \right] \frac{Vin}{1 + 2\pi f RC}$$

$$\frac{V_0}{V_{in}} = \frac{A_f}{1 + j \frac{f}{f_H}} \quad @@@ \; 1^a b \qquad f_H = \frac{1}{2\pi RC}$$

where $\dfrac{V_0}{V_{in}}$ =gain of the filter as a function of frequency

$$a_F = 1 + \frac{R_f}{R_!} = \text{passband gain of the filter}$$

F =frequency of the input signal Λ

$$f_H = \frac{1}{2\pi RC} = \text{high cut off frequency of the filter} \; \Lambda$$

        The gain magnitude and phase angle of the equation of the LPF can be obtained by converting eqn (1) b into its equivalent polar form as follows.

$$\left|\frac{V_0}{V_{in}}\right| = \frac{A_F}{\sqrt{1 + \left(\dfrac{f}{f_H}\right)^2}} \qquad \cdots (2)a$$

$$\phi = -\tan^{-1}\left(\frac{f}{f_H}\right) \qquad \cdots\cdots (2)b$$

Where Φ is the phase angle in degrees. The operation of the LPF can be verified from the magnitude eqn (2)a

1. At very low frequency, f<f$_H$ $\qquad \left|\dfrac{V_0}{V_{in}}\right| = A_F$

2. At f =f$_H$ $\qquad \left|\dfrac{V_0}{V_{in}}\right| = \dfrac{A_F}{\sqrt 2} = 0.707\, A_F$

3. At f> f$_H$ $\qquad \left|\dfrac{V_0}{V_{in}}\right| < A_F$

When the frequency R tenfold (one decade), the volt gain is divided by 10. (or) The gain S 20 dB(=20log10) each time the frequency is R by 10.

Hence the rate at which the gain rolls off f$_H$ = 20 dB or 6dB/octatve (twofold R in frequency). The frequency f = f$_H$ is called the cut off frequency because the gain of the filter at this frequency is down by 3 dB(=20 log 0.70)

Filter Origin:

A LPF can be designed by implementing the following steps.

1. Choose a value of high cut off frequency f$_H$.

2. Select a value of C less than or equal to 1μf.

3. Choose the value of R suing, $R = \dfrac{1}{2\pi f_H C}$

4. Finally select values of R1 and R$_F$ dependent on the desired passband gain A$_F$ using,

$$A_F = 1 + \frac{R_F}{R_1}$$

Frequency Scaling:

Once a filter is designed, these may sometimes be a need to change its cutoff frequency.

Convertion of original cutoff frequency f_H to a new cut off frequency f_H ' is called frequency scaling.

To change a high cutoff frequency multiply R or C, but not both by the ratio of

Original cutoff frequency

New cut off frequency

And f'_H R or f'_H C and then calculate f_H.

Second order LP Butterworth filter:

A second order LPF having a gain 40dB/decade in stop band. A First order LPF can be converted into a II order type simply by using an additional RC network.

The gain of the II order filter is set by R1 and R_F, while the high cut off frequency f_H is determined by R2,C2,R3 and C3.

$$f_H = \frac{1}{2\pi \sqrt{R_2 R_3 C_2 C_3}} @@@ 1^a$$

Voltage gain
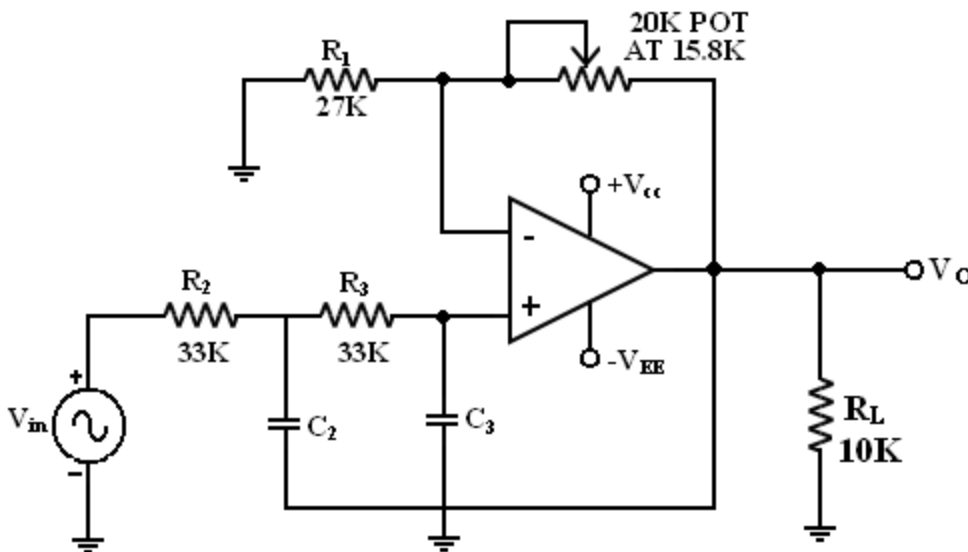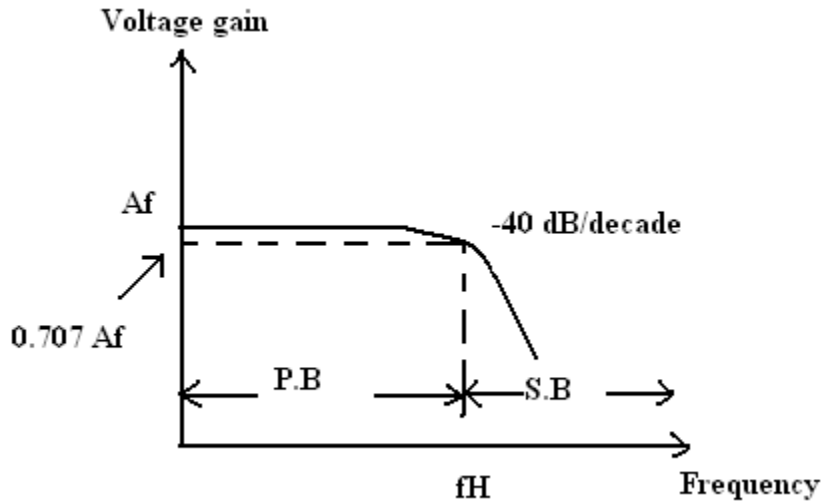
This above fig transferred into S domain.
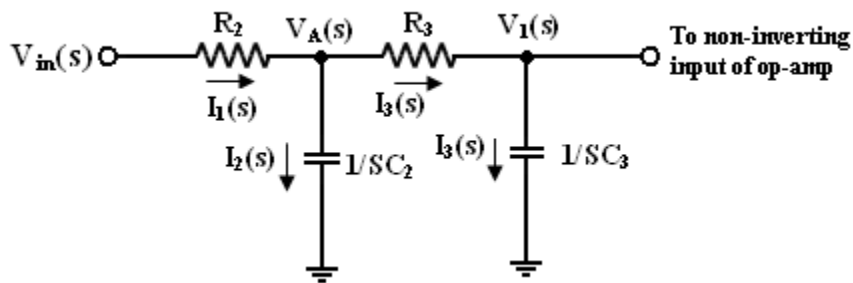
In this circuit all the components and the circuit parameters are expressed in the S-domain where S $= j$.

Writing Kirchoff's current law at node $V_A(S)$.

$$I_1 = I_2 + I_3$$

$$\frac{V_?-V_?}{R_2} = \frac{V_?-V_?}{\frac{1}{SC_2}} + \frac{V_?-V_?}{R_3} @@@@ \grave{}2^a$$

using voltage divider rule,

$$V_1 = \frac{\frac{1}{SC_2}}{R_3 + \frac{1}{SC_2}} V_A$$

$$V_1 = V_1 = \frac{V_?}{R_3 C_3 s + 1}$$

$$V_A = R_3 C_3 S + 1 \; V_1 @@@@@ \grave{}3^a$$

Substituting thhe value of V_A *in eqn* $\grave{}2^a$ *and solving for* V_1, *we get,*

From Eqn 2^a

$$\frac{V_{in}@V_A}{R_2} = SC_2 {}^{b}V_A @V_0 {}^{c} + \frac{V_{in}@V_A}{R_3}$$

$$V_{in}@V_A = R_2 C_2 SV_A @R_2 C_2 SV_0 + {}^{b}V_A @V_1 {}^{c}\frac{R_2}{R_3}$$

$$V_{in}@V_A = R_2 C_2 SV_A @R_2 C_2 SV_0 + V_A \frac{R_2}{R_3}@V_1 \frac{R_2}{R_3}$$

$$@R_2 C_2 SV_A @\frac{R_2}{R_3}V_A @V_A = @V_{in}@R_2 C_2 SV_0 @V_1 \frac{R_2}{R_3}$$

$$V_A {}^{F}\left[R_2 C_2 S + \frac{R_2}{R_3} + 1\right]^{G} = V_{in} + R_2 C_2 SV_0 + V_1 \frac{R_2}{R_3}$$

$$V_A {}^{B}\left[R_3 R_2 C_2 S + R_2 + R_3\right]^{C} = V_{in} R_3 + R_2 R_3 C_2 SV_0 + V_1 R_2$$

substituting V_A

$${}^{b}\left[R_3 C_3 S + 1\right]^{c} V_1 {}^{B}\left[R_2 R_3 C_2 s + R_2 + R_3\right]^{C} = V_{in} R_3 + R_2 R_3 C_2 SV_0 R_2 V_1$$

$${}^{b}\left[R_3 C_3 S + 1\right]^{c} v_1 {}^{B}\left[R_2 R_3 C_2 S + R_2 + R_3\right]^{C} @R_2 V_1 = V_{in} R_3 + R_{r_3} C_2 SV_1$$

$$V_1 = {}^{b}\frac{R_3 V_{in} + R_2 R_3 C_2 SV_0}{\left[R_3 C_3 S + 1\right]_{cb}\left[R_2 R_3 C_2 S + R_2 + R_3\right]^{c} @R_2} @@@@ \;\grave{}\;4^{a}$$

$$V_0 = A_F {}^{b}V_1 {}^{c} \qquad A_F = 1 + \frac{R_2}{R_1}$$

$$V_0 = {}^{b}\frac{{}^{B}A_F V_{in} R_3 + R_2 R_3 C_2 sV_0{}^{C}}{\left[R_3 C_3 S + 1\right]_{cb}\left[R_2 C_2 R_3 S + R_2 + R_3\right]^{c} @R_2} \qquad \frac{V_0}{V_{in}} = A_F$$

$$= \frac{A_F V_{in} {}^{J}\left[R_3 + r_2 R_3 C_2 S\right] \frac{V_0}{V_{in}}^{K}}{R_2 + R_3 R_3 R_2 C_2 S + R_3^2 R_2 C_3 C_2 S^2 + R_3 R_2 C_3 S + R_3^2 C_3 S @R_2}$$

$$= \frac{{}^{B}A_F V_{in} \left[1 + R_3 C_2 S\right]^{C}A_F}{S^2 R_3^2 R_2 C_2 C_3 + R_3^2 C_3 S + R_2 R_3 C_3 S + R_3 R_2 C_2 S + R_3}$$

$$= \frac{{}^{B}A_F V_{in} \left[1 + R_3 C_2 S\right]^{C}A_F}{S^2 R_3 R_2 C_3 C_2 + R_3 C_3 S + R_2 C_3 S + R_2 C_2 S + 1}$$

$$= \frac{{}^{B}A_F \left[1 + R_3 C_2 S\right]^{C}A_F}{{}^{b}S^2 {}^{c} + \frac{R_3 C_3 + R_2 C_3 + R_2 C_2 S}{R_3 R_2 C_2 C_3} + \frac{1}{R_3 R_2 C_2 C_3}} @@@@@@ \;\grave{}\;5^{a}$$

The denominator quadratic in the gain (V_0/V_{in}) eqn must have two real and equal roots. This means that

$$\omega^2 H = \frac{1}{R_2 R_3 C_2 C_3} \qquad @@@@@@ 6^a$$

$$or\, \omega H = \frac{1}{\sqrt{R_2 R_3 C_2 C_3}} \qquad @@@@@@ 7^a$$

$$f_H = \frac{1}{2\pi \sqrt{R_2 R_3 C_2 C_3}} \qquad @@@@ 8^a$$

For a second-order LP Butterworth response, the volt gain magnitude eqn is,

$$\left|\frac{V_0}{V_{in}}\right| = \frac{A_F}{\sqrt{1 + \left(\frac{f}{f_H}\right)^4}}$$

$$A_F = 1 + \frac{R_F}{R_1} = passband\ gain\ of\ the\ filter\ A$$

$$f = frequency\ of\ the\ input\ signal\ \grave{}Hz^a$$

$$f_H = \frac{1}{2\pi \sqrt{R_2 R_3 C_2 C_3}} = high\ cut\ off\ frequency\ \grave{}Hz^a$$

Filter Design:

1. Choose a value for a high cut off freq (f_H).
2. To simplify the design calculations, set $R_2 = R_3 = R$ and $C_2 = C_3 = C$ then choose a value of c<=1µf.
3. Calculate the value of R using eqn.(8) $R = \dfrac{1}{2\pi f_H C}$
4. Finally, because of the equal resistor ($R_2 = R_3$) and capacitor ($C_2 = C_3$) values, the pass band volt gain $A_F = 1 + R_F / R_1$ of the second order had to be = to 1.586. $R_F = 0.586\ R_1$. Hence choose a value of R_1<=100kΩ and
5. Calculate the value of R_F.

First order HP Butterworth filter:

High pass filters are often formed simply by interchanging frequency-determining resistors and capacitors in low-pass filters.

(i.e) I order HPF is formed from a I order LPF by interchanging components R & C.

Similarly II order HPF is formed from a II order LPF by interchanging R & C.
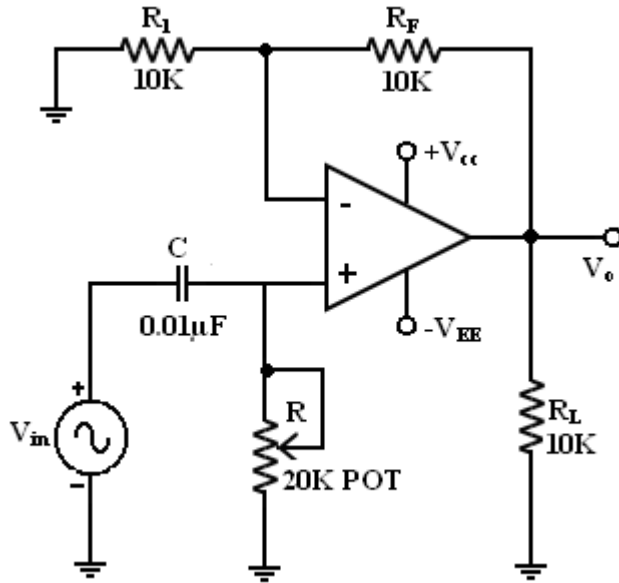
I order HPF
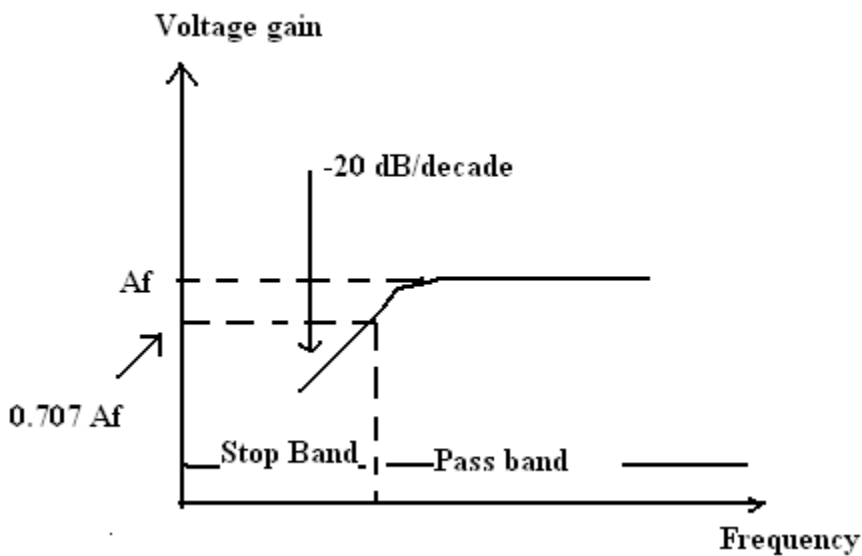
Here I order HPF with a low cut off frequency of f_L. This is the frequency at which the magnitude of the gain is 0.707 times its passband value.

Here all the frequencies higher than f_L are passband frequencies.

For the first order high pass filter, the output voltage is,

$$V_0 = \left[1 + \frac{R_F}{R_1}\right]\frac{j2\pi fRC}{1 + j2\pi fRC}\,Vin$$

$$\frac{V_0}{Vin} = A_F\left[\frac{j\dfrac{f}{f_L}}{1 + j\dfrac{f}{f_L}}\right] \qquad @@@@@\; 1$$

$$V_1 = \frac{R}{R @ jX_C}\,Vin$$

$$= \frac{R}{R + \dfrac{1}{j}2\pi f_C}\,Vin$$

$$V_1 = \frac{j2\pi fRC}{j2\pi fRC + 1}$$

$$V_0 = A_F\,V_1$$

$$A_F = 1 + \frac{R_F}{R_1} \quad where \; A_F = 1 + \frac{R_F}{R_{1\,}} = passband\ gain\ of\ the\ filter$$

$$f = frequencyy\ of\ the\ input\ signal\ \ Hz$$

$$f_L = \frac{1}{2\pi RC} = low\ cut\ off\ Frequency\ \ Hz$$

Hence the magnitude of the voltage gaiin is,

$$\left|\frac{V_0}{Vin}\right| = \frac{A_F\dfrac{f}{f_L}}{\sqrt{1 + \dfrac{f}{f_L^2}}} \qquad @@@@@@\; 2$$

Note: Design and Frequency scaling procedure of the LPF are also applicable to the HPF.

Second – order High Pass Butterworth Filter:

I order Filter, II order HPF can be formed from a II order LPF by interchanging the frequency – determine resistors and capacitors.
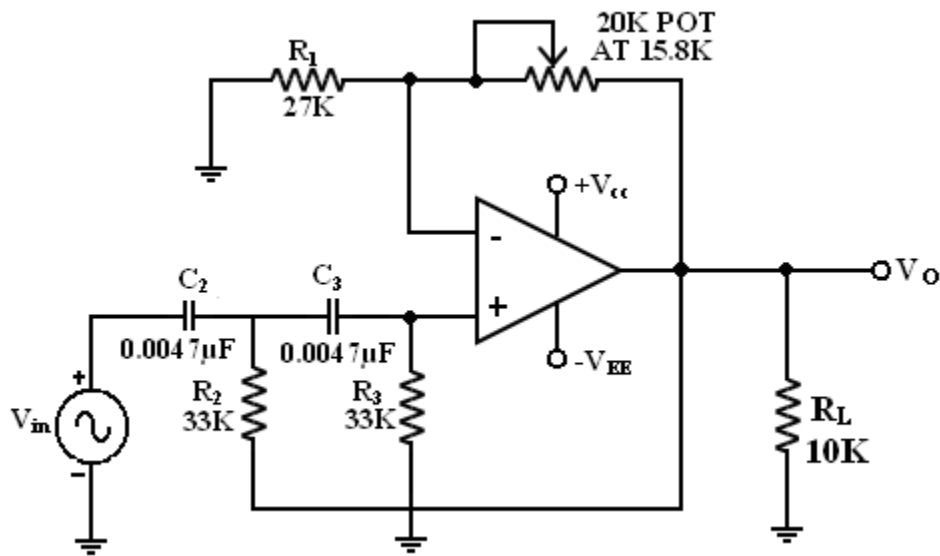
II order HPF
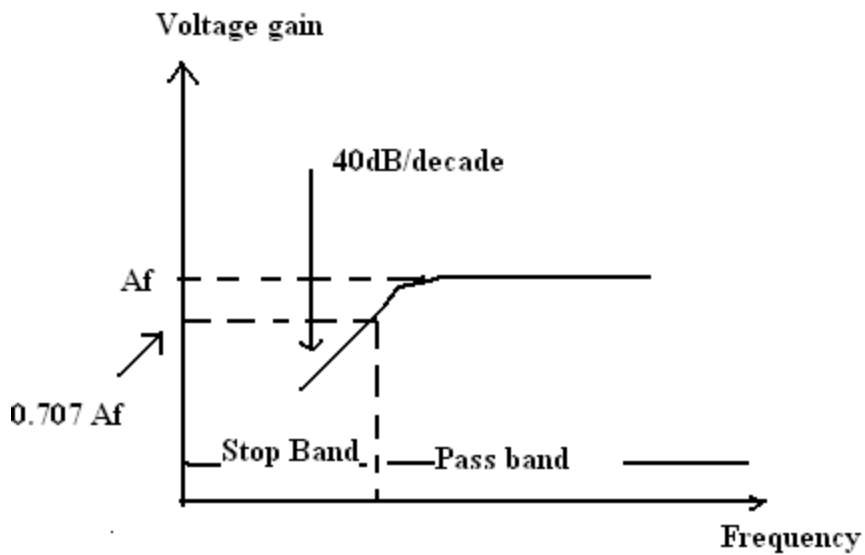
The Volt gain magnitude eqn of the II order HPF is as follows,

$$\left|\frac{V_0}{V_{in}}\right| = \frac{A_F}{\sqrt{1 + \left(\dfrac{f_L}{f}\right)^4}} \qquad @@@@@ \ 1$$

$A_F = 1.586 \ passband \ gain \ for \ the \ II \ order \ HPF$

$f = frequency \ of \ the \ input \ signal \ \ Hz$

$f_L = low \ cut \ off \ frequency \ \ Hz$

Analog Multipliers:

A multiple produces an output V_0 , which is proportional to the product of two inputs V_x and V_y.

That is, $V_0 = KV_xV_y$ where K is the scaling factor that is usually maintained as $(1/10)$ V^{-1} . There are various methods available for performing analog multiplication. Four of such techniques, namely,

1. Logarithmic summing technique
2. Pulse height/width modulation Technique
3. Variable trans conductance Technique
4. Multiplication using Gilbert cell and
5. Multiplication using variable trans conductance technique.

An actual multiplier has its output voltage V_0 defined by

$$V_0 = \frac{V_x + \phi_x \quad V_y + \phi_y}{10 \quad 1 + \varepsilon} + \phi_0$$

where ϕ_x and ϕ_y are the offsets associated with signals V_x and V_y, ε is the error signal associated with K and ϕ_0 is the offset voltage of the multiplier output.

The commonly used terminologies associated voltage of the multiplier characteristics:

Accuracy:

This specifies the derivation of the actual output from the ideal output, for any combination of X and Y inputs falling within the permissible operating range of the multiplier.

Linearity:

This defines the accuracy of the multiplier. The figure shows the response of the output as a function of one input voltage V_x when the other V_y is assumed constant. It represents the maximum percentage derivation from the ideal straight line output. An error surface is formed by plotting the output for different combinations of X and Y inputs. The Linearity Error can be defined as the maximum absolute derivation of the error surface. This linearity error imposes a lower limit on the multiplier accuracy.

$$y = \left(\frac{\Delta V_z(max)}{V_z(fullscale)}\right) X100\%$$
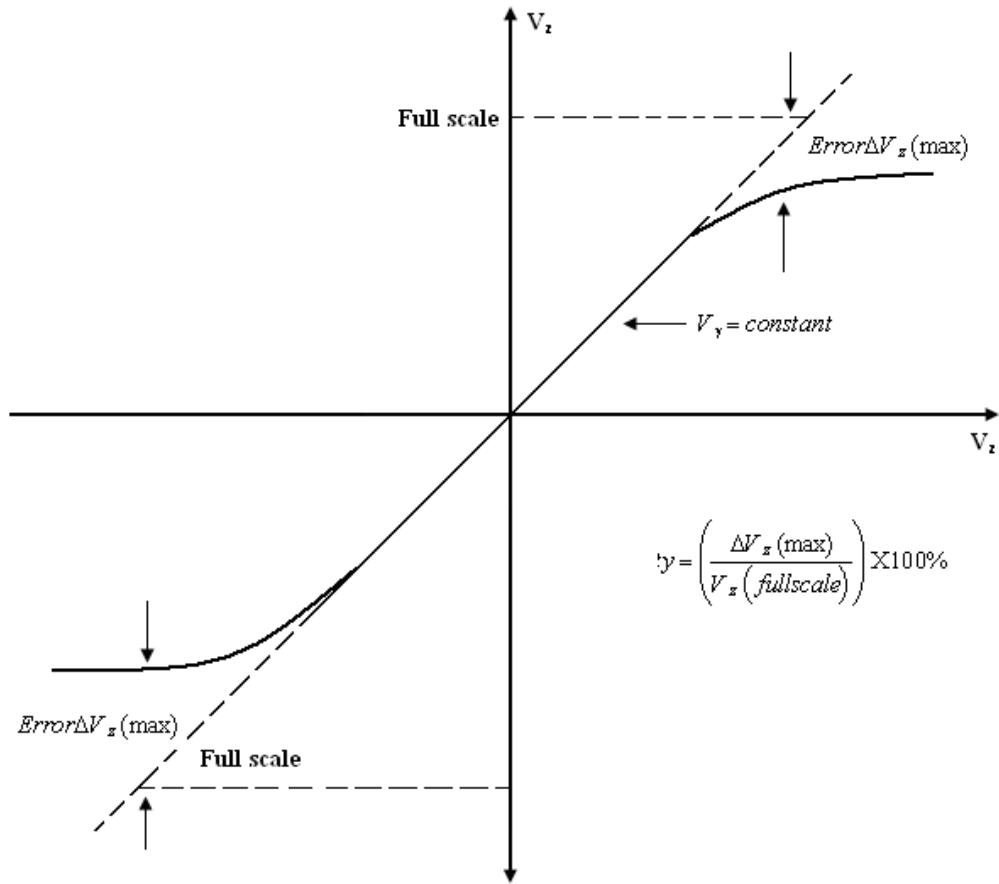
Squaring Mode Accuracy:

The Square – law curve is obtained with both the X and Y inputs connected together and applied with the same input signal. The maximum derivation of the output voltage from an ideal square – law curve expresses the squaring mode accuracy.
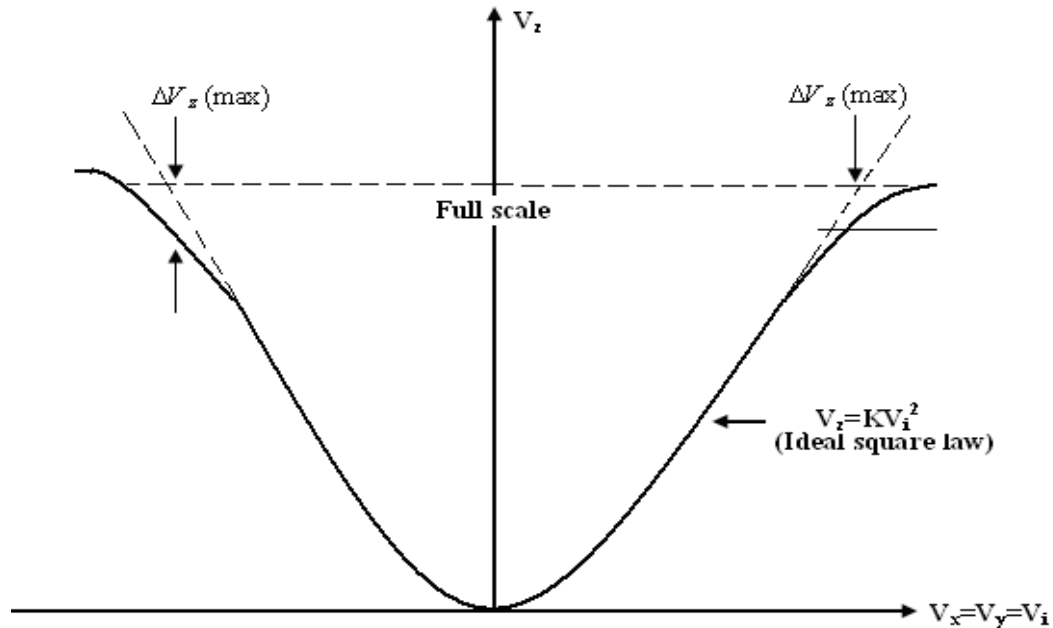
Bandwidth:

The Bandwidth indicates the operating capability of an analog multiplier at higher frequency values. Small signal 3 dB bandwidth defines the frequency f_0 at which the output reduces by 3dB from its low frequency value for a constant input voltage. This is identified individually for the X and Y input channels normally.

The transconductance bandwidth represents the frequency at which the transconductance of the multiplier drops by 3dB of its low frequency value. This characteristics defines the application frequency ranges when used for phase detection or AM detection.

Quadrant:

The quadrant defines the applicability of the circuit for bipolar signals at its inputs. First – quadrant device accepts only positive input signals, the two quadrant device accepts one bipolar signal and one unipolar signal and the four quadrant device accepts two bipolar signals.

Logarithmic summing Technique:

This technique uses the relationship

$\ln V_x + \ln V_y = \ln(V_x V_y)$
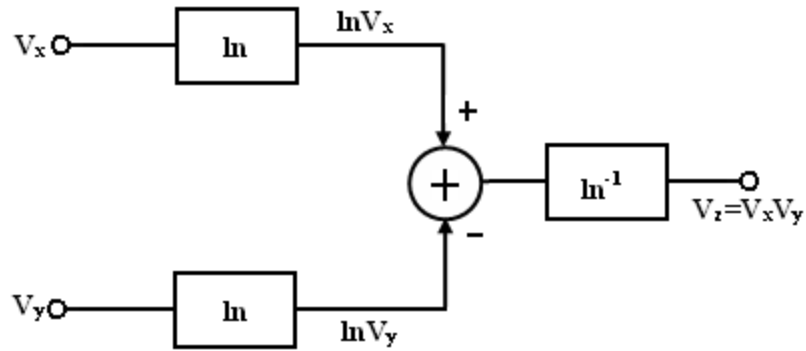
As shown in figure the input voltages V_x and V_y are converted to their logarithmic equivalent, which are then added together by a summer. An antilogarithmic converter produces the output voltage of the summer. The output is given by,

$V_z = \ln^{-1}(\ln(V_x V_y)) = V_x V_y$ The exponential relationship between the collector current and base to emitter voltage of bipolar transistor during its active mode of operation could be explained for the logarithmic and anti-logarithmic conversions. The relationship between I_0 and V_{BE} of the transistor is given by

$I_C = I_0 e^{(V_{BE}/V_T)}$ It is found that the transistor follows the relationship very accurately in the range of 10nA to 100mA. Logarithmic multiplier has low accuracy and high temperature instability. This method is applicable only to positive values of V_x and V_y. Therefore, this type of multiplier is restricted to one quadrant operation only.

Pulse Height/ Width Modulation Technique:
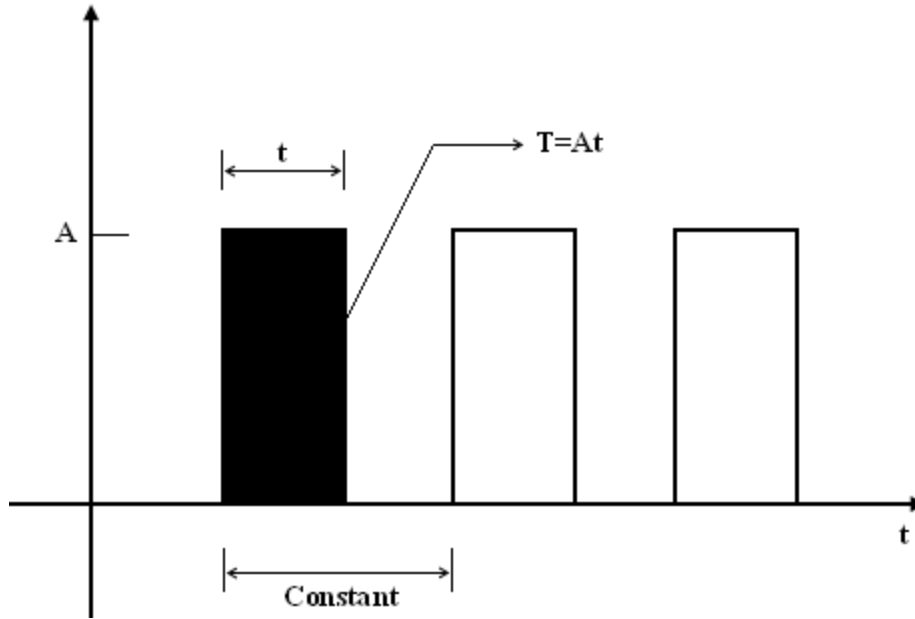
In this method, the pulse width of a pulse train is made proportional to one input voltage and the pulse amplitude is made proportional to the second input voltage. Therefore, $V_x = K_x A$, $V_y = K_y t$, and $V_z = K_z T$ where K_x, K_y, K_z are scaling factors. In figure A is the amplitude of the pulse, t is the pulse width and T is the area of the pulse. Therefore,

$$V_z = K_z T = K_z At = \frac{V_x V_y}{K_x K_y}$$

The modulated pulse train is passed through an integrated circuit. Therefore, the input of the integrator is proportional to the area of pulse, which in turn is proportional to the product of two input voltages.

A simple multiplier using an Emitter coupled Transistor pair:
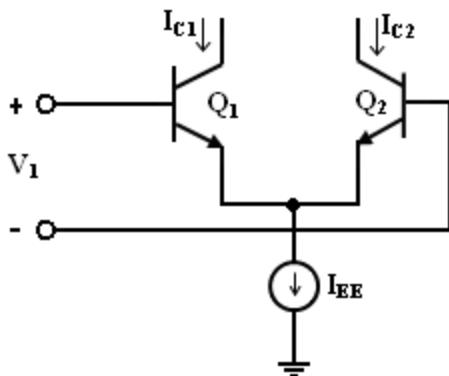
A circuit using an emitter coupled pair is shown in figure. The output currents I_{C1} and I_{C2} are related to the differential input voltage V_1 by $I_{C1} = \dfrac{I_{EE}}{1+e^{-V_1/V_T}}$ and $I_{C2} = \dfrac{I_{EE}}{1+e^{V_1/V_T}}$ where V_T is the thermal voltage and the base currents have been neglected. Combining above eqn, we have the difference between the two output currents as

$$\Delta I_C = I_{C1} - I_{C2}$$

$$= I_{EE}\left[\frac{1}{1+e^{-V_1/V_T}} - \frac{1}{1+e^{V_1/V_T}}\right]$$

$$= I_{EE}\tanh\frac{V_1}{2V_T}$$

The dc transfer characteristics of the emitter – coupled pair is shown in figure. It shows that the emitter coupled pair can be used as a simple multiplier using this configuration. When the differential input voltage $V_1 \ll V_T$, we can appropriate as given by

$$I_{EE}\tanh\frac{V_1}{2V_T} = I_{EE}\frac{V_1}{2V_T}$$
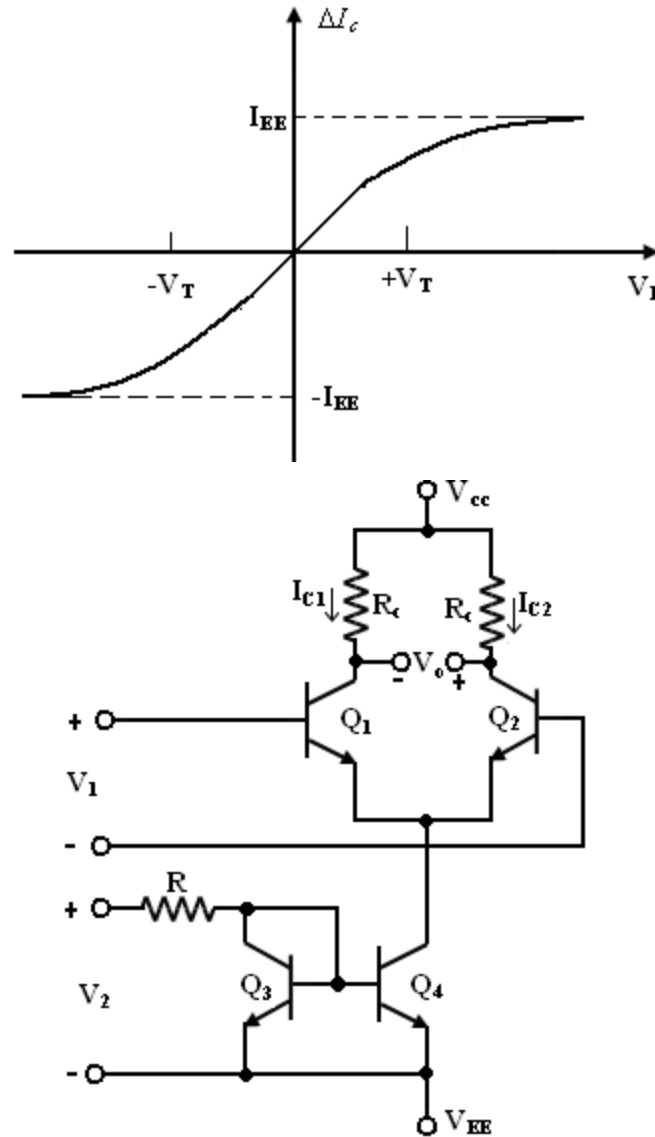
Then it becomes,   ---- (*)

$$\Delta I_C = I_{EE}\frac{V_1}{2V_T}$$

The current I_{EE} is the bias current for the emitter – coupled pair. If the current I_{EE} is made proportional to a second input signal V_2, then

$$I_{EE} = K_0\left(V_2 - V_{BE\,on}\right)$$

Substituting above eqn in (*), we get $\Delta I_C = \dfrac{K_0 V_1\left(V_2 - V_{BE\,on}\right)}{2V_T}$

This arrangement is shown in figure. It is a simple modulator circuit constructed using a differential amplifier. It can be used as a multiplier, provided V_1 is small and much less than 50mV, and V_2 is greater than $V_{BE(on)}$. But, the multiplier circuit shown in figure has several limitations. The first limitation is that V_2 is offset by $V_{BE(on)}$. The second is that V_2 must always be positive which results in only a two-quadrant multiplier operation. The third limitation is that, the tanh (X) is approximately as X, where $X = V_1 / 2V_T$. The first two limitations are overcome in the Gilbert cell.

Gilbert Multiplier cell:

The Gilbert multiplier cell is a modification of the emitter coupled cell and this allows four – quadrant multiplication. Therefore, it forms the basis of most of the integrated circuit balanced

multipliers. Two cross- coupled emitter- coupled pairs in series connection with an emitter coupled pair form the structure of the Gilbert multiplier cell. The operation of the Gilbert cell is shown in figure.

The collector current of Q_3 and Q_4 are given by

$$I_{C3} = \frac{I_{C1}}{1 + e^{@V_T}}$$

and $I_{C4} = \dfrac{I_{C1}}{1 + e^{V_T}}$

Similarly, The collector current of Q_5 and Q_6 are given by

$$I_{C5} = \frac{I_{C2}}{1 + e^{V_T}}$$

and $I_{C6} = \dfrac{I_{C2}}{1 + e^{@V_T}}$

The collector current I_{C1} and I_{C2} of transistors Q_1 and Q_2 can be expressed as

$$I_{C1} = \frac{I_{EE}}{1 + e^{@V_T}}$$

and $I_{C2} = \dfrac{I_{EE}}{1 + e^{V_T}}$

Substituting the above equation in I_{C3} and I_{C4}, we get

$$I_{C3} = \frac{I_{EE}}{\left(1 + e^{@V_T}\right)\left(1 + e^{@V_T}\right)}$$

and $I_{C4} = \dfrac{I_{EE}}{\left(1 + e^{V_T}\right)\left(1 + e^{@V_T}\right)}$

Similarly substituting I_{c2} in I_{c5} and I_{C6}, we get,

$$I_{C5} = \frac{I_{EE}}{\left(1 + e^{V_T}\right)\left(1 + e^{@V_T}\right)}$$

and

$$I_{C6} = \frac{I_{EE}}{\left(1 + e^{@V_T}\right)\left(1 + e^{V_T}\right)}$$

The differential output current ΔI is given by

$\Delta I = I_{L1} @ I_{L2}$

That is,
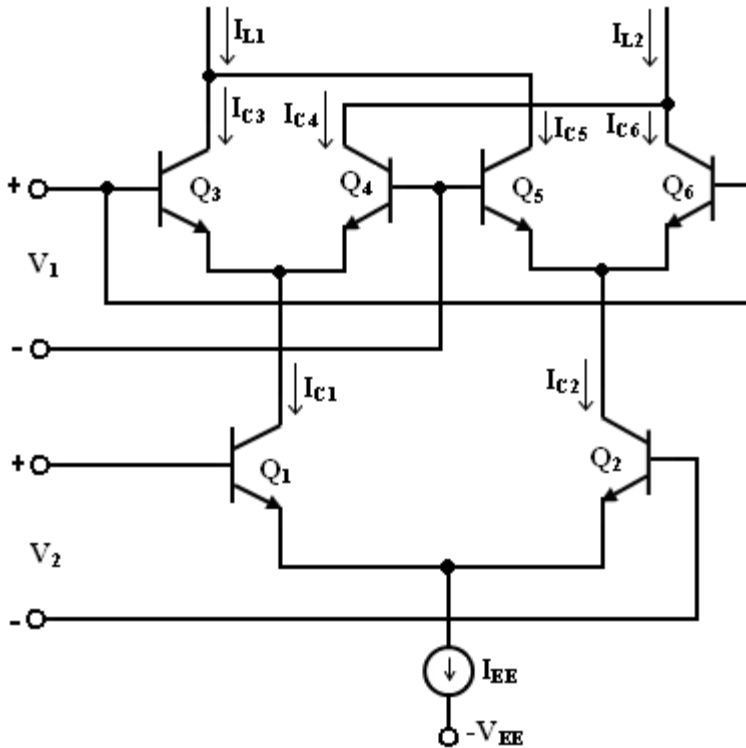
The above equation shows that when V_1 and V_2 are small, the Gilbert Cell shown in figure can be used as a four quadrant analog multiplier with the use of current to voltage converters. The dc transfer characteristic of such a multiplier circuit is the product of the hyperbolic tangent of the two input voltages. The output voltage V_0 can be generated from ΔI, by using two equal valued resistors connected to Vcc and by sending I_{L1} ($=I_{C3} +I_{C5}$) through one resistor and I_{L2} ($=I_{C4} +I_{C6}$) through the second resistor.

A modulator or a mixer is a circuit with two inputs, namely, carrier input and modulating input and one modulated output. A linear response is required only for the modulating input, since the carrier is usually an ac signal with constant amplitude.

The multiplier shown in figure can also used as a modulator, if one of the inputs is very large and the second input is very small ($\tanh(X) = X$). Then, the transistors operated by the large-signal input act as switches. This effectively multiplies the small input signal by a square wave. Hence, this mode of operation acts as a modulator. These are called synchronous modulators and they find applications in signal processing, demodulation and phase detection.

Gilbert multiplier with pre distortion circuits:

When the magnitudes of V_1 and V_2 are very small when compared with V_T, the hyperbolic tan function is approximated as linear, and the circuit can be used as a multiplier, for finding the

product of V_1 and V_2. But, when larger V_1 and V_2 are to be multiplied, a nonlinearity function can be used to pre distort the input signals. This compensates for the hyperbolic tangent transfer characteristic of the basic cell. The required nonlinearity function is an inverse hyperbolic tangent characteristic whose arrangement is shown in figure.

$$\Delta I_o = I_{c3-5} - I_{C4-6}$$
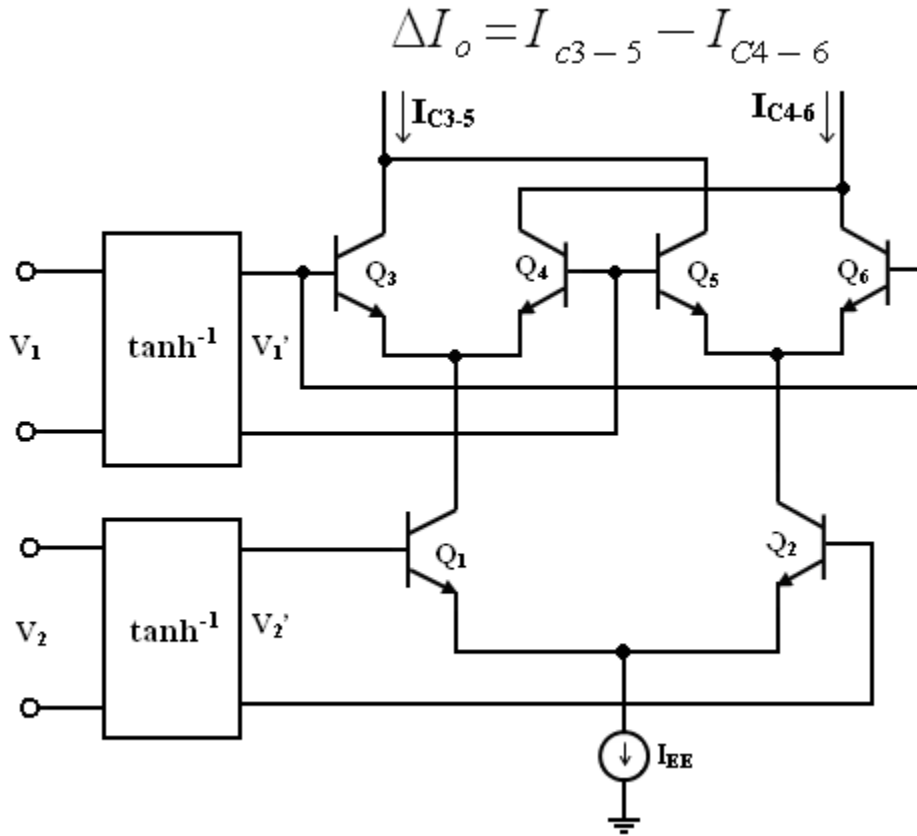
The generation of the inverse hyperbolic tangent function is shown in figure. Assume that the circuit within the box generates a differential output current, and it linearly depends on the input voltage V_1.

Then, $I_{E1} = I_{o1} + K_1 V_1$ and $I_{E2} = I_{o1} + K_1 V_1$

Vcc

Q₇   Q₈

+
ΔV
–

↓ I_{E1}   I_{E2} ↓

V₁

Voltage-to-Current Converter
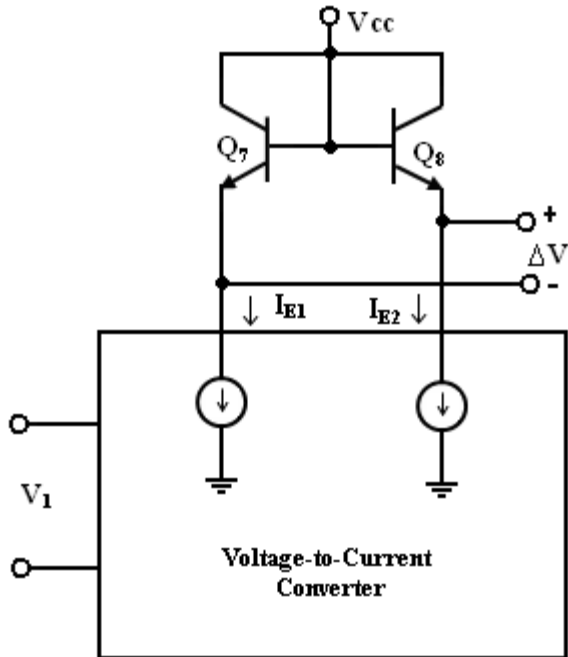
Where I_{01} is the dc current flowing in each output, K_1 is the transconductance of the voltage – to current converter, and it is assumed that $V_1 = 0$. The differential voltage ΔV across the diode – connected transistors Q_7 and Q_8 is given by

$$\Delta V = V_T \ln\left[\frac{I_{01} + K_1 V_1}{I_0}\right] @ V_T \ln\left[\frac{I_{01} @ K_1 V_1}{I_0}\right]$$

$$= V_T \ln\left\{\frac{I_{01} + K_1 V_1}{I_{01} @ K_1 V_1}\right\}$$

This can be transformed into $\Delta V = 2 V_T \tanh^{@1}\left[\frac{K_1 V_1}{I_{01}}\right]$ Using the identity

$$\tanh^{@1} X^a = \frac{1}{2} \ln\left[\frac{1 + X}{1 @ X}\right]$$

When this functional block is used, it compensates for the nonlinearity of the inputs. Then ,

$$\Delta I = I_{EE}\left[\frac{K_1 V_1}{I_{01}}\right]^T \left[\frac{K_1 V_1}{I_{02}}\right]$$

where $I_{01,}$ K_1 and I_{02} , K_2 are the parameters of the functional blocks following inputs V_1 and V_2 respectively. The above equation shows that the differential output current is proportional to the product $V_1 V_2$.

Complete four – Quadrant analog multiplier:

The above figure illustrates the circuit diagram of the complete four – quadrant analog multiplier using Gilbert Cell. The three boxes are voltage to current converters or current to voltages converters in effect. The pre- distortion for the input signal is achieved by transistors Q_7 and Q_8 . The currents I_9 and I_{10} passing through the emitters of Q_7 and Q_8 generate a voltage between the two emitter terminals, that is proportional to the inverse hyperbolic tangent of V_1 .

Analysis of the circuit:
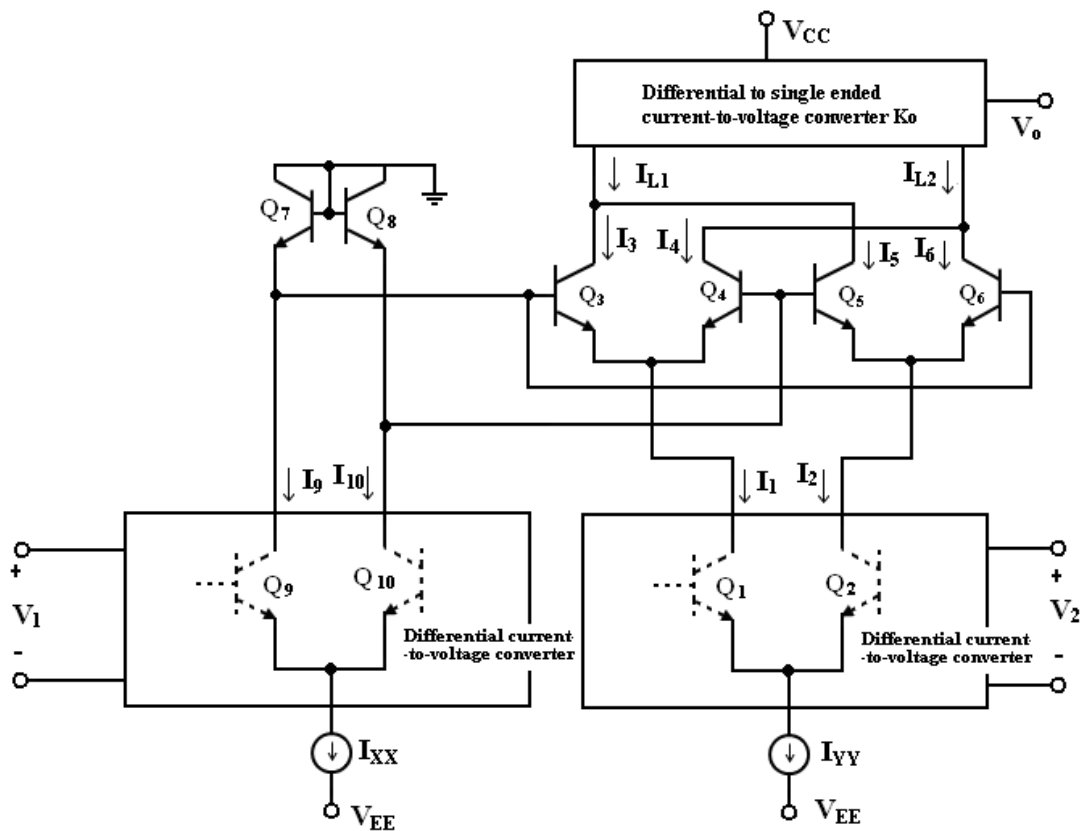
A complete four quadrant analog multiplier using Gilbert cell is shown in figure. The current through base – emitter junctions of transistors Q_7 , Q_3 , Q_4 , Q_8 connected in series can be expressed by

$I_9 I_3 = I_4 I_{10}$ ---(1)

Similarly, from the series connections of the transistors Q_7 , Q_6 , Q_5 and Q_8 we get $I_9 I_6 = I_5 I_{10}$ ---(2)

From figure, we see that,

$I_1 = I_3 + I_4$ --(3)

$I_2 = I_5 + I_6$ --(4)

$I_{L1} = I_3 + I_5$ --(5)

$I_{L2} = I_4 + I_6$ ---(6)

$I_{XX} = I_9 + I_{10}$ ---(7)

The transfer characteristics of the differential voltage to current converter is given by

$I_9 - I_{10} = V_1/K_1$ ---(8)

$I_1 - I_2 = V_2/K_2$ ---(9)

and the transfer characteristics of the differential to single ended current is given by

$V_0 = K_0(I_{L2} - I_{L1})$ ---(10)

Where K_0, K_1, and K_2 are constants.

Substituting for I_{L1} and I_{L2} from (5) and (6) in (10) , we get

$V_0 = K_0 [(I_4 + I_6) - (I_3 + I_5)]$

Using (1) and (2) ,

$$V_0 = K_0 \left[I_4 + I_5 \frac{I_{\ldots}}{I_9} @ I_4 \frac{I_{\ldots}}{I_9} + I_5 \right] K \qquad @@@ \ 11$$

Simplifying the above eqn, we get

$$V_0 = K_0 \left[\frac{I_{\ldots}}{I_9} I_4 @ I_5 \right] \qquad @@@ \ 12$$

From figure, we see that

$$I_1 @ I_2 = I_3 + I_4 \ @ \ I_5 + I_6$$

$$= I_4 \frac{I_{\ldots}}{I_9} + I_4 \ @ \ I_5 + I_5 \frac{I_{\ldots}}{I_9} \qquad @@@ \ 13$$

Solving for $(I_4 - I_5)$ gives

$$I_4 @ I_5 = \frac{I_{\ldots}}{I_9 + I_{10}} I_1 @ I_2 \qquad @@@ \ 14$$

Substituting (14) in (12) using (8) and (9) , we get

$$V_0 = K_0 \frac{I_1 @ I_2 \, \text{gb}}{I_9 + I_{10}} \, {}^c I_1 @ I_2$$

$$= \frac{K_m V_1 V_2}{I_{XX} K_1 K_2} = K_m V_1 V_2 \quad @@@ \ 15^a$$

Where

$$K_m = \frac{K}{I_{XX} K_1 K_2}$$

Eqn (15) employs no approximations. Hence the input signal amplitudes have no constraints.

Practical implementation of the four – quadrant analog multiplier:
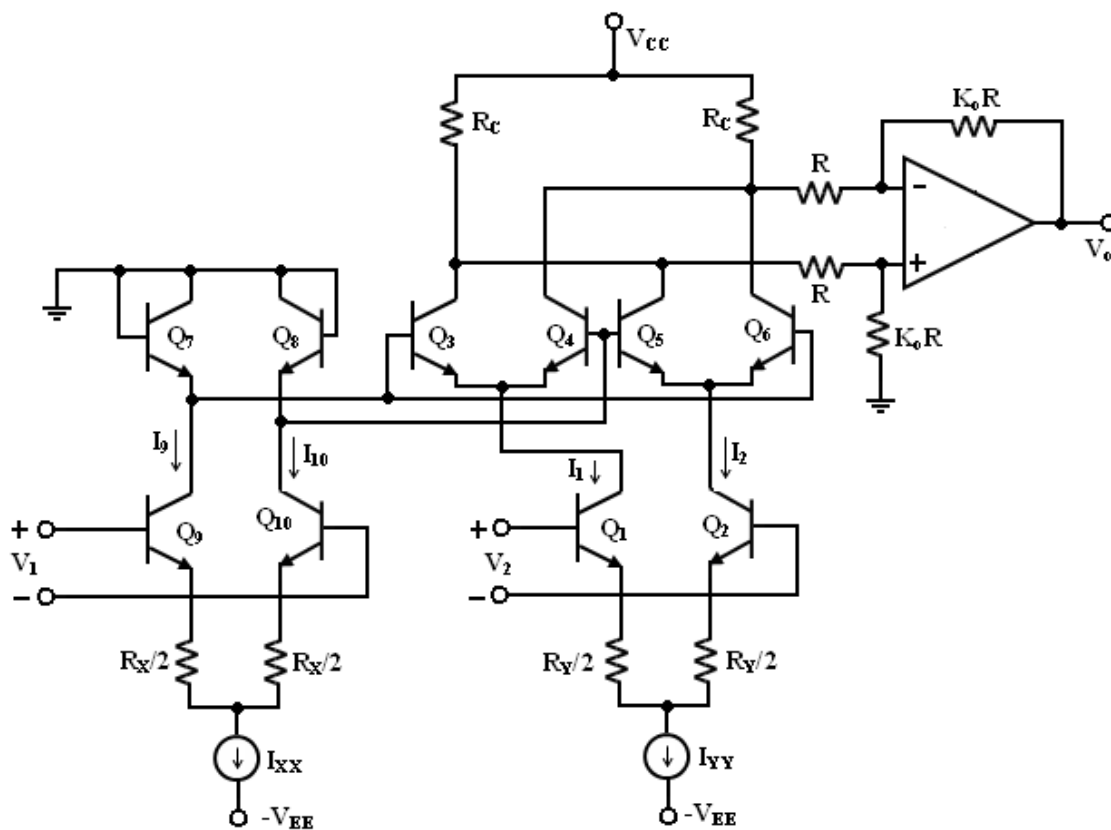
A practical four –quadrant analog multiplier circuit is shown in figure. It can be observed that,

$$I_1 @ I_2 = \frac{2V}{R_Y} \quad @@@@ \ 16^a$$

$$I_9 @ I_{10} = \frac{2V}{R_X} \quad @@@@@ \ 17^a$$

further it is assumed that the drop across base-emitter of $Q_9 - Q_{10}$ and $Q_1 - Q_2$ are small in comparison with the drop across R_X and R_Y.

Substituting Eqn 16 and 17 in eqn 15 we get,

$$V_0 = \frac{4 K_m R_m V_m V_m}{I_{XX} R_X R_Y}$$

$$= K_m V_1 V_2 \ where \ R >> R_C$$

The circuit is capable of performing precise multiplication of a continuously varying analog signal by another signal. One of the problems though, is need to be able to trim the errors due to offsets and mismatches in the integrated circuit implementation.

Variable Transconductance Technique:

The variable transconductance technique makes use of the dependence characteristic of the transistor transconductance parameter on the emitter current bias applied. A simple differential circuit arrangement depicting the principle is shown in figure. The relationship between V_0 and V_x is given by

$$V_0 = g_m R_L V_X$$
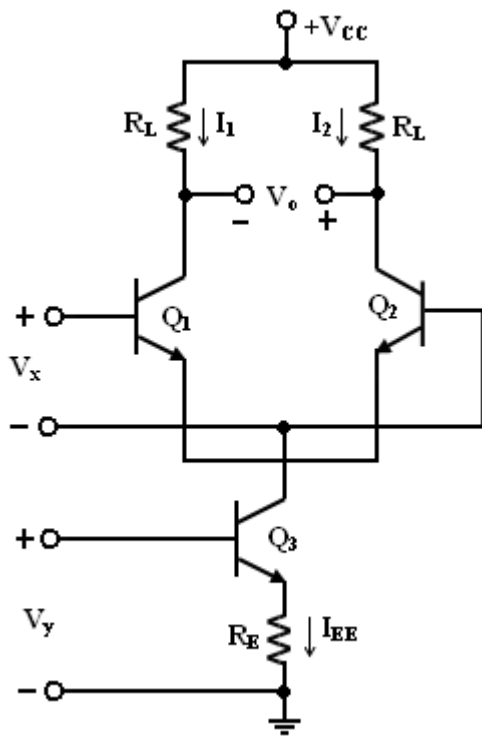
Where $g_m = I_{EE}/V_T$ is the transconductance of the stage. Application of a second input V_y to the reference current source of the differential amplifier can vary g_m.

Thus, if $R_E I_{EE} \gg V_{BE}$, the bias voltage V_y is related to I_{EE} by the relation $V_y = I_{EE} R_E$. Then, the overall voltage transfer expression is given by

$$V_0 = g_m R_L V_x = (V_y/V_T R_E)V_x R_L$$
$$= V_x V_y \ \frac{R_L}{V_T R_E}$$

Generation of logarithmic bias input for differential stage:
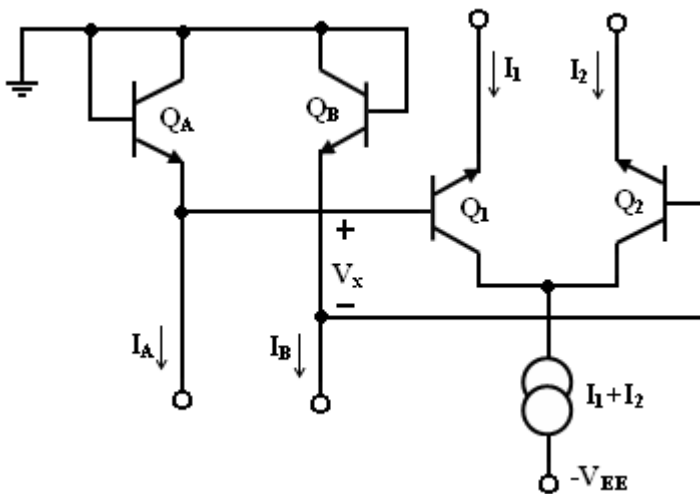
It is assumed that $|V_x| \ll V_T$ and there is no emitter degeneration. Referring to below figure, the collector currents I_1 and I_2 are related to the applied voltage V_x by the relation

$$\frac{I_1}{I_2} = e^{\frac{V_x}{V_y}} \quad \text{---(1)}$$

Therefore, linearity can be achieved by reducing the exponential current – voltage characteristic to a linear one as shown in figure. The transistor Q_1 and Q_2 are biased through the diode connected Q_A and Q_B, which are driven by controlled current sources I_A and I_B respectively. Then the net bias voltage V_x is represented by

$$V_x = V_T \ln \left[\frac{I_g}{I_A} \right] \qquad @@@\ 2^a$$

Substituting eqn 2^a in 1^a we get

$$\frac{I}{I_2} = \frac{I}{I_A}$$

Similarly,

$$\frac{I_N}{I_A + A_B} = \frac{I_g}{I_1 + I_2} = \frac{I_1}{1 + e^{\frac{1}{V_T}}} @@@\ 3^a$$

and

$$\frac{I_g}{I_A + I_B} = \frac{I}{I_1 + I_2} = \frac{I}{1 + e^{\frac{1}{V_T}}} @@@@\ 4^a$$

The above equations are valid over a wider range, if the device characteristics are well matched and V_{BE} obeys the basic diode equation.

Four Quadrant Variable transconductance multiplier:

A typical four quadrant multiplier circuit is shown below. The four quadrant operation indicates that the output voltage is directly proportional to the product of the two input voltages regardless of the polarity of the inputs and such multipliers can be operated in all the four quadrants of operation.
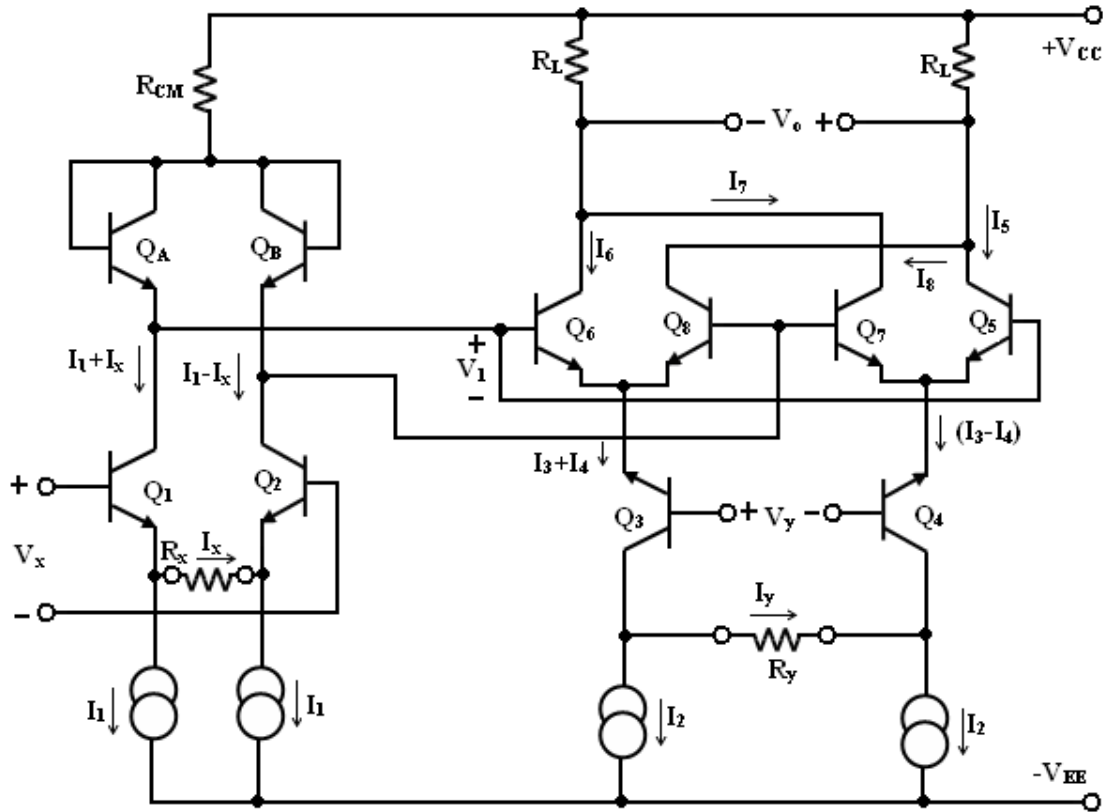
The first part of the circuit generates an intermediate voltage V_1 across the transistors Q_A and Q_B in response to the input signal V_x . The nonlinear response to the input V_x in generating V_1 is compensated by the inverse nonlinearity associated with the base – emitter junctions of the quad-transistors $Q_5 - Q_6$ and $Q_7 - Q_8$. Thus the output voltage V_z is maintained proportional to the linear product of the two voltages. The emitter degeneration resistors R_x and R_y provide linear conversion of the input voltages to differential currents I_x and I_y. Thus $I_X = V_x / R_x$ and $I_y = V_y / R_y$. The value of R_x and R_y are chosen such that $R_x >> V_T / I_1$ and $R_y >> V_T / I_2$ respectively.

The output voltage V_0 can be written as

$$V_0 = R_L ((I_6 + I_7) - (I_5 + I_8)) \qquad ---(5)$$

Applying eqn 3 and 4 to the circuit, we obtain

$$\frac{\text{...}}{I_3 + I_y} = \frac{\text{...}}{I_3 @ I_y} = \frac{\text{...}}{2I_1}$$

and

$$\frac{\text{...}}{I_3 + I_y} = \frac{\text{...}}{I_3 @ I_y} = \frac{\text{...}}{2I_1}$$

Sub eqn 6 and 7 into 5 we get,

$$V_0 = \frac{2R \quad^b}{I_1}\,^c I_x I_y$$

Since I_x and I_y are linearly related to V_x and V_y respectively we have

$$V_0 = K V_x V_y$$

where the scaling factor $K = \dfrac{2R}{I R_x R_y}$, which is normally chosen as 0.1

Analog Multiplier ICs

Analog multiplier is a circuit whose output voltage at any instant is proportional to the product of instantaneous value of two individual input voltages. The important applications of these multipliers are multiplication, division, squaring and square – rooting of signals, modulation and demodulation. These analog multipliers are available as integrated circuits consisting of op-amps and other circuit elements. The Schematic of a typical analog multiplier, namely, AD633 is shown in figure.
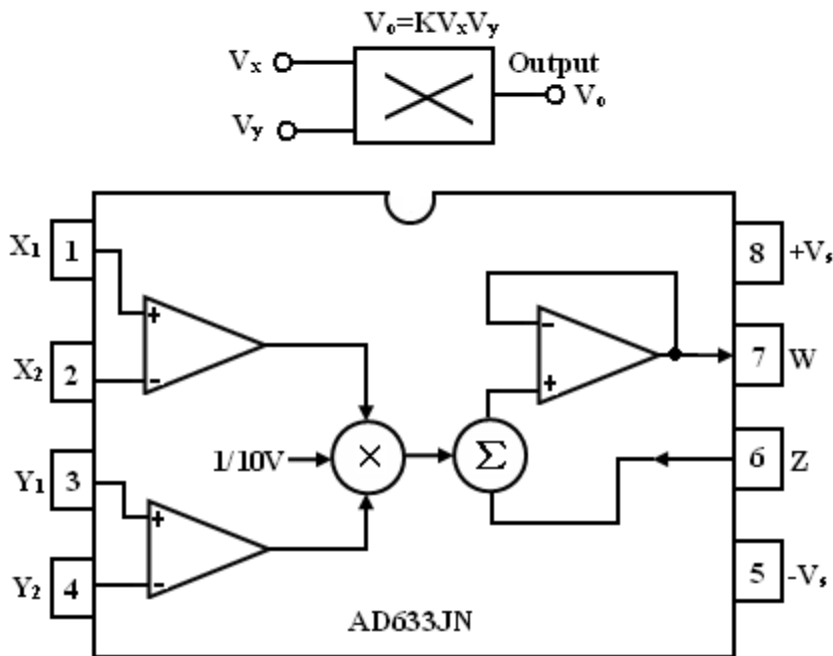
The AD633 multiplier is a four – quadrant analog multiplier. It possesses high input impedance, and this characteristic makes the loading effect on the signal source negligible. It can operate with supply voltages ranging from ±18V. The IC does not require external components. The calibration by user is not necessary. The typical range of the two input signals is ±10V.

Schematic representation of a multiplier:

The schematic representation of an analog multiplier is shown in figure. The output V_0 is the product of the two inputs V_x and V_y is divided by a reference voltage Vref. Normally, the reference voltage Vref is internally set to 10V. Therefore, $V_0 = VxVy/10$. In other words, the basic input – output relationship can be defined by $KV_x V_y$ when $K = 1/10$, a constant. Thus for peak input voltages of 10V, the peak magnitude of output voltage is $1/10 *10 *10 = 10V$. Thus, it can be noted that, as long as $V_x < 10V$ and $V_y < 10V$, the multiplier output will not saturate.

Multiplier quadrants:

The transfer characteristics of a typical four-quadrant multiplier is shown in figure. Both the inputs can be positive or negative to obtain the corresponding output as shown in the transfer characteristics.
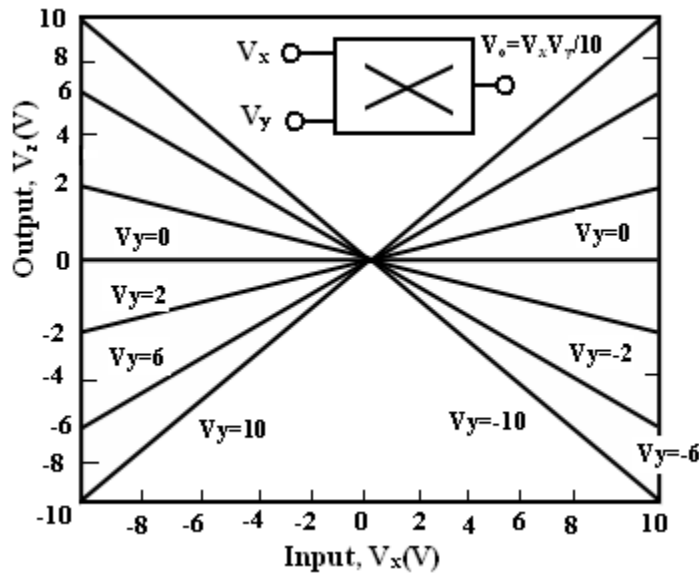
Applications of Multiplier ICs:

The multiplier ICs are used for the following purposes:

1. Voltage Squarer
2. Frequency doubler

3. Voltage divider
4. Square rooter
5. Phase angle detector
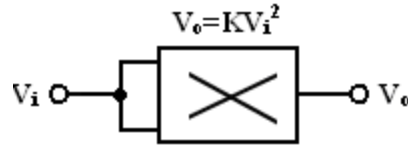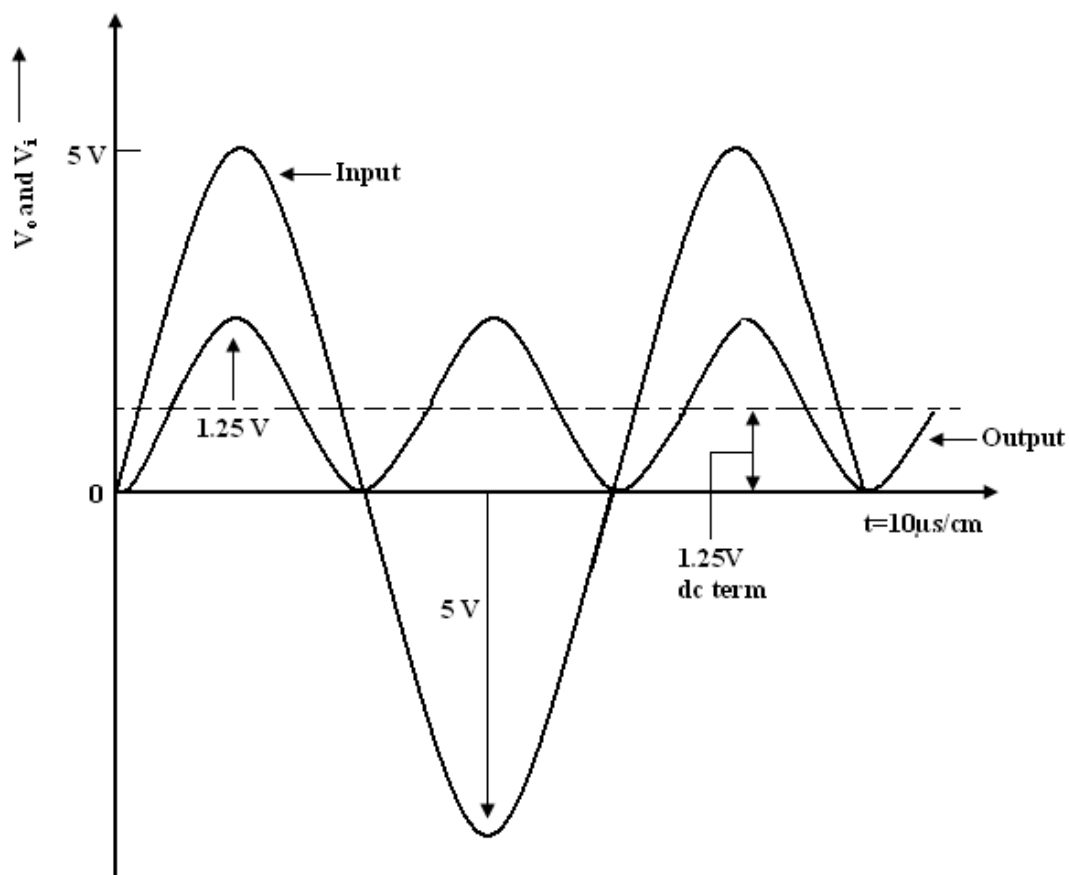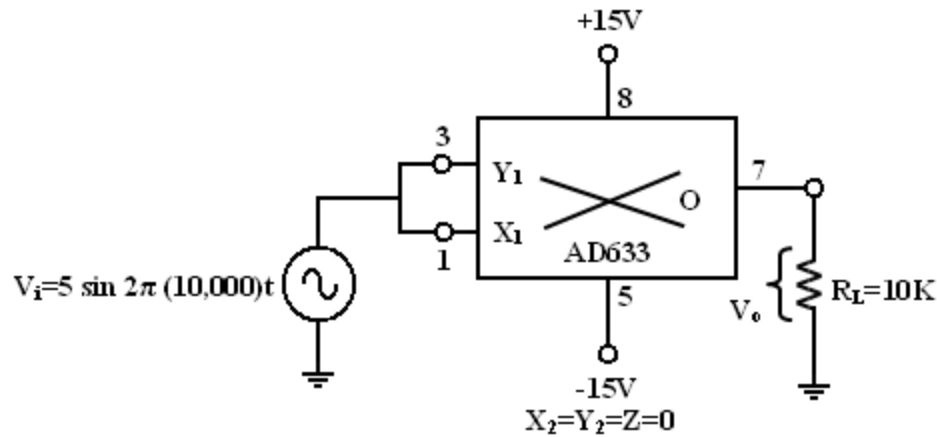6. Rectifier

Voltage Squarer:

Figure shows the multiplier IC connected as a squaring circuit. The inputs can be positive or negative, represented by any corresponding voltage level between 0 and 10V. The input voltage V_i to be squared is simply connected to both the input terminals, and hence we have, $V_x = V_y = V_i$ and the output is $V_0 = Kv^2{}_i$. The circuit thus performs the squaring operation. This application can be extended for frequency doubling applications.

Frequency doubler:

Figure shows the squaring circuit connected for frequency doubling operation. A sine-wave signal V_i has a peak amplitude of A_v and frequency of fHz. Then, the output voltage of the doubler circuit is given by

$$V_0 = \frac{A_v\sin 2\pi ft \cdot A_v \sin 2\pi ft}{10} = \frac{A_v^2}{10}\sin^2 2\pi ft$$

$$= \frac{A_v^2}{20}\left[1 - \cos 4\pi ft \right]$$

Assuming a peak amplitude A_v of 5V and frequency f of 10KHz, $V_0 = 1.25 - 1.25 \cos 2\Pi(20000)t$. The first term represents the dc term of 1.25V peak amplitude. The input and output waveforms are shown in figure. The output waveforms ripples with twice the input frequency in the rectified output of the input signal. This forms the principle of application of analog multiplier as rectifier of ac signals. The dc component of output V_0 can be removed by connecting a 1μF coupling capacitor between the output terminal and a load resistor, across which the output can be observed.

$V_i = 5 \sin 2\pi (10{,}000)t$

+15V

8

3

Y_1

X_1

AD633

7

O

5

$R_L = 10K$

V_o

-15V

$X_2 = Y_2 = Z = 0$

5 V — Input

1.25 V

0

5 V

1.25V dc term

t=10µs/cm

Output

Voltage Divider:

The voltage divider circuit can be constructed using a multiplier and an op-amp as shown in figure. This circuit produces the ratio of two input signals. The division is achieved by connecting the multiplier in the feedback loop of an op-amp. The voltages V_{den} and V_{num} represent the two input voltages, V_{dm} forms one input of the multiplier, and output of op-amp V_{oA} forms the second input.

The output V_{OA} forms the second input. The output V_{OM} of the multiplier is connected back of op-amp in the feedback loop. Then the characteristic operation of the multiplier gives

$V_{om} = K V_{OA} V_{dm}$ ---(1)
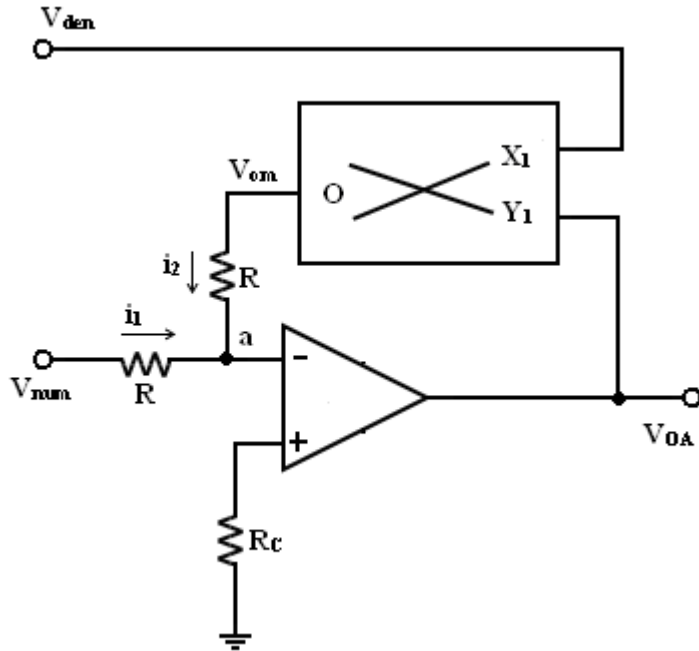
As shown in figure, no input signal current can flow into the inverting input terminal of op-amp, which is at virtual ground. Therefore, at the junction a, $i_1 + i_2 = 0$, The current $i_1 = V_{num} / R$, where R is the input resistance and the current $i_2 = V_{om} / R$. With virtual ground existing at a,

$$i_1 + i_2 = \frac{V_{num}}{R} + \frac{V_{om}}{R} = 0,$$

$$V_{om} = @V_{num}$$

Sub 1 in above eqn

$$KV_{OA} V_{den} = @V_{num}$$

or

$$V_{OA} = @\frac{V_{num}}{KV_{den}}$$

Where V_{num} and V_{den} are the numerator and denominator voltages respectively. Therefore, the voltage division operation is achieved. V_{num} can be a positive or negative voltage and V_{dm} can have only positive values to ensure negative feedback. When V_{dm} is changed, the gain $10/V_{dm}$ changes, and this feature is used in automatic gain control (AGC) circuits.

Square Rooter:

The divider voltage an V_{dm} can be used to find the square root of a signal by connecting both inputs of the multiplier to the output of the op-amp. Then, the output voltage of the multiplier V_{OM} is

equal in magnitude but opposite in polarity (with respect to ground) to Vi. But we know that V_{om} is one- term (Scale factor) of $V_0 * V_0$ or

$-V_i = V_{om} = V^2_0$

Solving for V_0 and eliminating $\sqrt{-1}$ yields.

$V_0 = \sqrt{10}|V_i|$

Eqn states that V_0 equals the square root of 10 times the absolute magnitude of V_i . The input voltage V_i must be negative, or else, the op-amp saturates. The range of V_i is between -1 and -10V. Voltages less than -1V will cause inaccuracies in the result. The diode prevents negative saturation for positive polarity V_i signals. For positive values of V_i the diode connections are reversed.

Phase Angle detector:

The multiplier configured for phase angle detection measurement is shown in figure. When two sine-waves of the same frequency are applied to the inputs of the multiplier, the output V_0 has a dc component and an ac component.

The trigonometric identity shows that

Sin A sin B =1/2 (cos(A-B) – cos(A+B)).

When the two frequencies are equal, but with different phase angles, e.g. A=$2\pi ft$ +θ for signal V_x amd B= $2\pi ft$ for signal $V_{y,}$ then using the identity
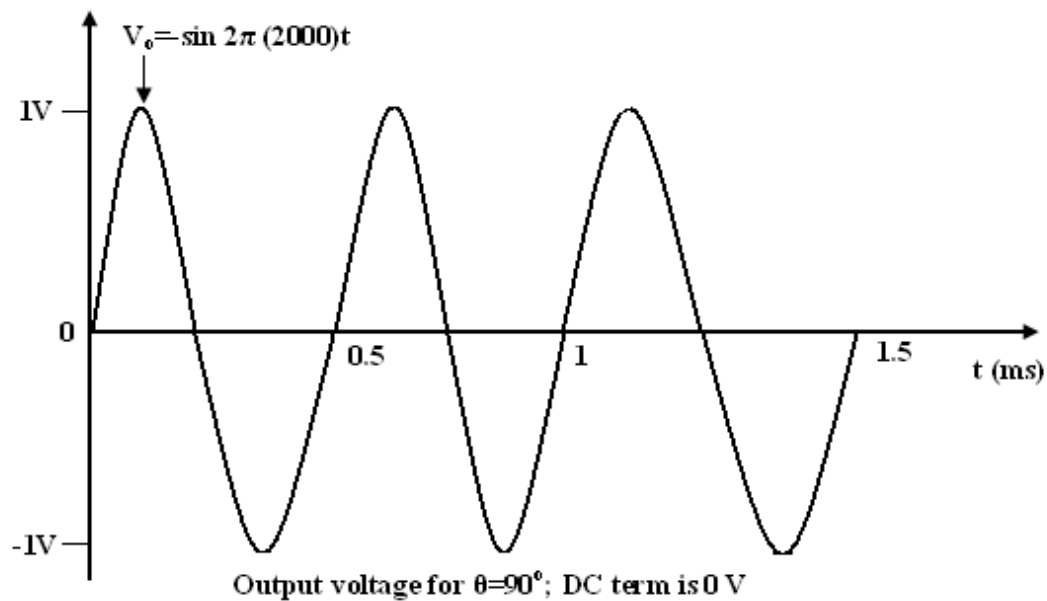
$$\sin\left(2\pi ft + \theta\right)\sin 2\pi ft = \frac{1}{2}\left[\cos\theta - \cos\left(4\pi ft + \theta\right)\right]$$

$$= \frac{1}{2} \, dc \; the \; double \; frequency \; term$$

Therefore, when the two input signals V_x and V_y are applied to the multiplier, $V_{0(dc)}$ is given by

$$V_{0\,dc} = \frac{V_{xp} V_{yp}}{20}\cos\theta$$

where V_{xp} and V_{yp} are the peak voltage amplitudes of the signals V_x and V_y. Thus, the output $V_{0(dc)}$ depends on the factor cos θ. A dc voltmeter can be calibrated as a phase angle meter when the product of V_{xp} and V_{yp} is made equal to 20. Then, a (0-1) V range dc voltmeter can directly read cos θ, with the meter calibrated directly in degrees from a cosine table. The input and output waveforms are shown in figure.

Then the above eqn becomes $V_{0(dc)}$ = cos θ, if we make the product $V_{xp} V_{yp}$ = 20 or in other words, $V_{xp} - V_{yp} = 4.47V$

+15V

8

$V_Y = V_{YP} \sin (2\pi ft)$

3

Y_1

X_1

1

O

7

AD633

5

−15V

$X_2 = Y_2 = Z = 0$

$V_X = V_{XP} \sin (2\pi ft + \theta)$

V_m

DC Voltmeter
to measure θ
0 V to 1 V scale

$V_y = 4.47 \sin 2\pi (1000)t$

$V_x = 4.47 \sin (2\pi(1000)t + \theta)$

V_x and V_y

0

θ=90°

1

1.5

t (ms)

Input voltage for θ=90°

$V_o = \sin 2\pi (2000)t$

1V

0

0.5

1

1.5

t (ms)

−1V

Output voltage for θ=90°; DC term is 0 V
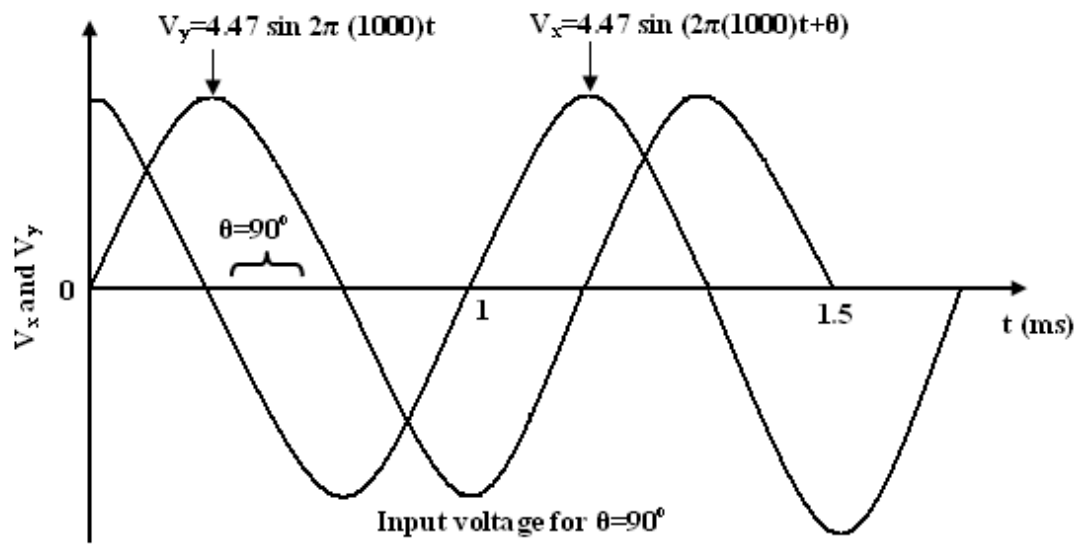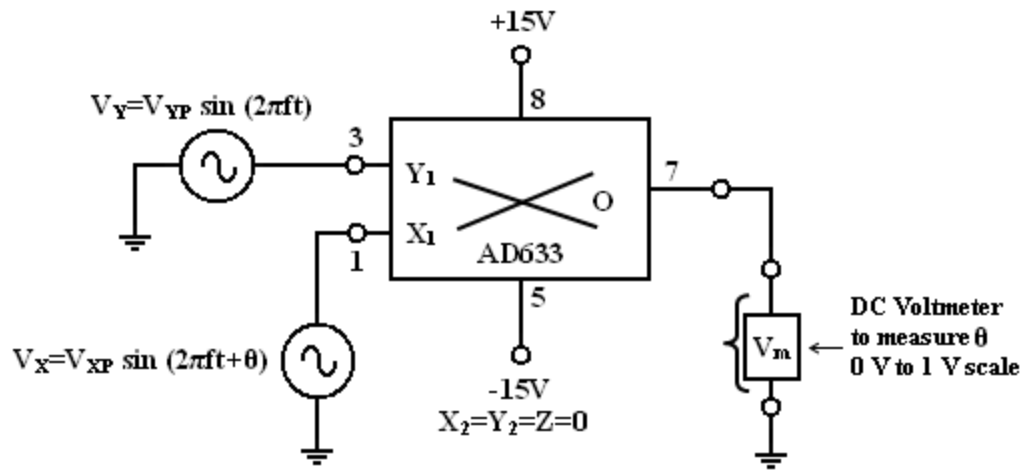
PHASE LOCKED LOOP:

Basic Block Diagram of a PLL

Forward path

f_{IN}
Input frequency → **Phase Detector** → **Low Pass Filter** → **Voltage Controlled Oscillator** →

Feedback path
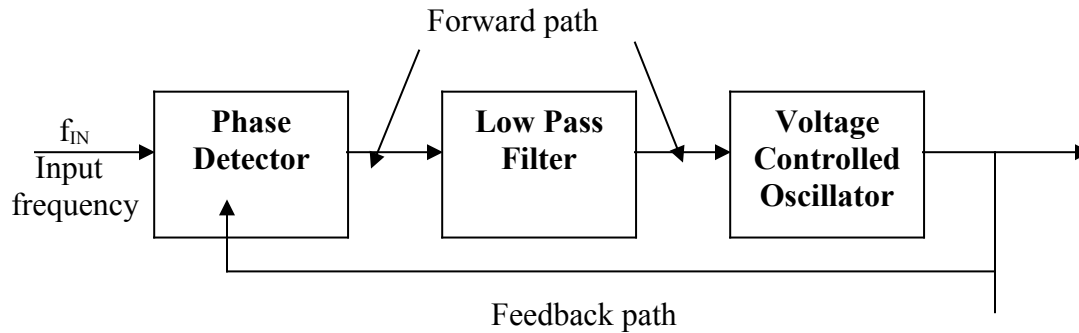
phase locked loop construction and operation:

- The PLL consists of i) Phase detector ii) LPF iii) VCO. The phase detector or comparator compares the input frequency f_{IN} with feedback frequency f_{OUT}.
- The output of the phase detector is proportional to the phase difference between f_{IN} & f_{OUT}. The output of the phase detector is a dc voltage & therefore is often referred to as the error voltage.
- The output of the phase detector is then applied to the LPF, which removes the high frequency noise and produces a dc level. This dc level in turn, is input to the VCO.
- The output frequency of VCO is directly proportional to the dc level. The VCO frequency is compared with input frequency and adjusted until it is equal to the input frequencies.
- PLL goes through 3 states, i) free running ii) Capture iii) Phase lock.

Before the input is applied, the PLL is in free running state. Once the input frequency is applied the VCO frequency starts to change and PLL is said to be in the capture mode. The VCO frequency continuous to change until it equals the input frequency and the PLL is in phase lock mode. When Phase locked, the loop tracks any change in the input frequency through its repetitive action. If an input signal v_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output v_o of the VCO. If the two signals differ in frequency of the incoming signal to that of the output v_o of the VCO. If the two signals differ in frequency and/or phase, an error voltage v_e is generated.

The phase detector is basically a multiplier and produces the sum ($f_s + f_o$) and difference ($f_s - f_o$) components at its output. The high frequency component ($f_s + f_o$) is removed by the low pass filter and the difference frequency component is amplified then applied as control voltage v_c to VCO. The signal v_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s and f_o. Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked. Once locked, the output frequency f_o of VCO is identical to f_s except for a finite phase difference φ. This phase difference φ generates a corrective control voltage v_c to shift the VCO frequency from f_0 to f_s and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages (i) free running, (ii) capture and (iii) locked or tracking.

Capture range: the range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of f_o.

Pull-in time: the total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

(a) Phase Detector:

    Phase detector compares the input frequency and VCO frequency and generates DC voltage i.e., proportional to the phase difference between the two frequencies. Depending on whether the analog/digital phase detector is used, the PLL is called either an analog/digital type respectively. Even though most monolithic PLL integrated circuits use analog phase detectors.

Ex for Analog: Double-balanced mixer
Ex for Digital: Ex-OR, Edge trigger, monolithic Phase detector.

Ex-OR Phase Detector:
This uses an exclusive OR gate. The output of the Ex-OR gate is high only when f_{IN} or f_{OUT} is high.

The DC output voltage of the Ex-OR phase detector is a function of the phase difference between its two outputs. The maximum dc output voltage occurs when the phase difference is Π radians or

180 degrees. The slope of the curve between 0 or Π radians is the conversion gain k_p of the phase detector for eg; if the Ex-OR gate uses a supply voltage $Vcc = 5V$, the conversion gain K_p is

$$K_P = \frac{5V}{\Pi} = 1.59V / RAD$$

Edge Triggered Phase Detector:

Advantages of Edge Triggered Phase Detector over Ex-OR are

i) The dc output voltage is linear over 2Π radians or 360 degrees, but in Ex-OR it is Π radians or 180 degrees.

ii) Better Capture, tracking & locking characteristics.

Edge triggered type of phase detector using RS Flip – Flop. It is formed from a pair of cross coupled NOR gates.

RS FF is triggered, i.e, the output of the detector changes its logic state on the positive edge of the inputs f_{IN} & f_{OUT}

Monolithic Phase detector:

- It consists of 2 digital phase detector, a charge pump and an amplifier.
- Phase detector 1 is used in applications that require zero frequency and phase difference at lock.
- Phase detector 2, if quadrature lock is desired, when detector 1 is used in the main loop, detector can also be used to indicate whether the main loop is in lock or out of lock.

    R→ Reference

    V→ Variable or 0feedback input

    PU → Pump Up signal

    PD→Pump Down signal

    UF → Up frequency output signal

    DF → Down frequency output signal

(b) Low – Pass filter:

The function of the LPF is to remove the high frequency components in the output of the phase detector and to remove the high frequency noise. LPF controls the characteristics of the phase locked loop. i.e, capture range, lock ranges, bandwidth

- Lock range(Tracking range):

  The lock range is defined as the range of frequencies over which the PLL system follows the changes in the input frequency f_{IN}.

- Capture range:

  Capture range is the frequency range in which the PLL acquires phase lock. Capture range is always smaller than the lock range.

- Filter Bandwidth:

  Filter Bandwidth is reduced, its response time increases. However reduced Bandwidth reduces the capture range of the PLL. Reduced Bandwidth helps to keep the loop in lock through momentary losses of signal and also minimizes noise.

(c) Voltage Controlled Oscillator (VCO):

The third section of PLL is the VCO; it generates an output frequency that is directly proportional to its input voltage. The maximum output frequency of NE/SE 566 is 500 Khz.

f_{IN} → Input frequency → **Voltage Controlled Oscillator** → OUT →
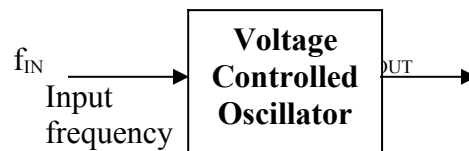
Feedback path and optional divider:

Most PLLs also include a divider between the oscillator and the feedback input to the phase detector to produce a frequency synthesizer. A programmable divider is particularly useful in radio

transmitter applications, since a large number of transmit frequencies can be produced from a single stable, accurate, but expensive, quartz crystal–controlled reference oscillator.

Some PLLs also include a divider between the reference clock and the reference input to the phase detector. If this divider divides by M, it allows the VCO to multiply the reference frequency by N / M. It might seem simpler to just feed the PLL a lower frequency, but in some cases the reference frequency may be constrained by other issues, and then the reference divider is useful. Frequency multiplication in a sense can also be attained by locking the PLL to the 'N'th harmonic of the signal.

Equations:

The equations governing a phase-locked loop with an analog multiplier as the phase detector may be derived as follows. Let the input to the phase detector be $x_c(t)$ and the output of the voltage-controlled oscillator (VCO) is $x_r(t)$ with frequency $\omega_r(t)$, then the output of the phase detector $x_m(t)$ is given by

$$x_m(t) = x_c(t) \cdot x_r(t)$$

the VCO frequency may be written as a function of the VCO input $y(t)$ as

$$\omega_r(t) = \omega_f + g_v y(t)$$

where g_v is the *sensitivity* of the VCO and is expressed in Hz / V.

Hence the VCO output takes the form

$$x_r(t) = A_r \cos\left(\int_0^t \omega_r(\tau)\, d\tau\right) = A_r \cos(\omega_f t + \varphi(t))$$

where

$$\varphi(t) = \int_0^t g_v y(\tau)\, d\tau$$

The loop filter receives this signal as input and produces an output

$$x_f(t) = F_{\text{filter}}(x_m(t))$$

where F_{Filter} is the operator representing the loop filter transformation.

When the loop is closed, the output from the loop filter becomes the input to the VCO thus

$$y(t) = x_f(t) = F_{\text{filter}}(x_m(t))$$

We can deduce how the PLL reacts to a sinusoidal input signal:

$$x_c(t) = A_c \sin(\omega_c t).$$

The output of the phase detector then is:

$$x_m(t) = A_c \sin(\omega_c t) A_r \cos(\omega_f t + \varphi(t)).$$

This can be rewritten into sum and difference components using trigonometric identities:

$$x_m(t) = \frac{A_c A_f}{2} \sin(\omega_c t - \omega_f t - \varphi(t)) + \frac{A_c A_f}{2} \sin(\omega_c t + \omega_f t + \varphi(t))$$

As an approximation to the behaviour of the loop filter we may consider only the difference frequency being passed with no phase change, which enables us to derive a small-signal model of the phase-locked loop. If we can make $\omega_f \approx \omega_c$, then the $\sin(\cdot)$ can be approximated by its argument resulting in: $y(t) = x_f(t) \simeq -A_c A_f \varphi(t)/2$. The phase-locked loop is said to be *locked* if this is the case.

<div align="center">CONTROL SYSTEM ANALYSIS/ CLOSED LOOP ANALYSIS OF PLL</div>

Phase locked loops can also be analyzed as control systems by applying the Laplace transform. The loop response can be written as:

$$\frac{\theta_o}{\theta_i} = \frac{K_p K_v F(s)}{s + K_p K_v F(s)}$$

Where

- θ_o is the output phase in radians

- θ_i is the input phase in radians

- K_p is the phase detector gain in volts per radian

- K_v is the VCO gain in radians per volt-second

- $F(s)$ is the loop filter transfer function (dimensionless)

The loop characteristics can be controlled by inserting different types of loop filters. The simplest filter is a one-pole RC circuit. The loop transfer function in this case is:

$$F(s) = \frac{1}{1 + sRC}$$

The loop response becomes:

$$\frac{\theta_o}{\theta_i} = \frac{\frac{K_p K_v}{RC}}{s^2 + \frac{s}{RC} + \frac{K_p K_v}{RC}}$$

This is the form of a classic harmonic oscillator. The denominator can be related to that of a second order system:

$$s^2 + 2s\zeta\omega_n + \omega_n^2$$

Where

- ζ is the damping factor

- ω_n is the natural frequency of the loop

For the one-pole RC filter,

$$\omega_n = \sqrt{\frac{K_p K_v}{RC}}$$

$$\zeta = \frac{1}{2\sqrt{K_p K_v RC}}$$

The loop natural frequency is a measure of the response time of the loop, and the damping factor is a measure of the overshoot and ringing. Ideally, the natural frequency should be high and the damping factor should be near 0.707 (critical damping). With a single pole filter, it is not possible to control the loop frequency and damping factor independently. For the case of critical damping,

$$RC = \frac{1}{2K_p K_v}$$

$$\omega_c = K_p K_v \sqrt{2}$$

A slightly more effective filter, the lag-lead filter includes one pole and one zero. This can be realized with two resistors and one capacitor. The transfer function for this filter is

$$F(s) = \frac{1 + sCR_2}{1 + sC(R_1 + R_2)}$$

This filter has two time constants

$$\tau_1 = C(R_1 + R_2)$$

$$\tau_2 = CR_2$$

Substituting above yields the following natural frequency and damping factor

$$\omega_n = \sqrt{\frac{K_p K_v}{\tau_1}}$$

$$\zeta = \frac{1}{2\omega_n \tau_1} + \frac{\omega_n \tau_2}{2}$$

The loop filter components can be calculated independently for a given natural frequency and damping factor

$$\tau_1 = \frac{K_p K_v}{\omega_n^2}$$

$$\tau_2 = \frac{2\zeta}{\omega_n} - \frac{1}{K_p K_v}$$

Real world loop filter design can be much more complex eg using higher order filters to reduce various types or source of phase noise.

Applications of PLL:

The PLL principle has been used in applications such as FM stereo decoders, motor speed control, tracking filters, FM modulation and demodulation, FSK modulation, Frequency multiplier, Frequency synthesis etc.,
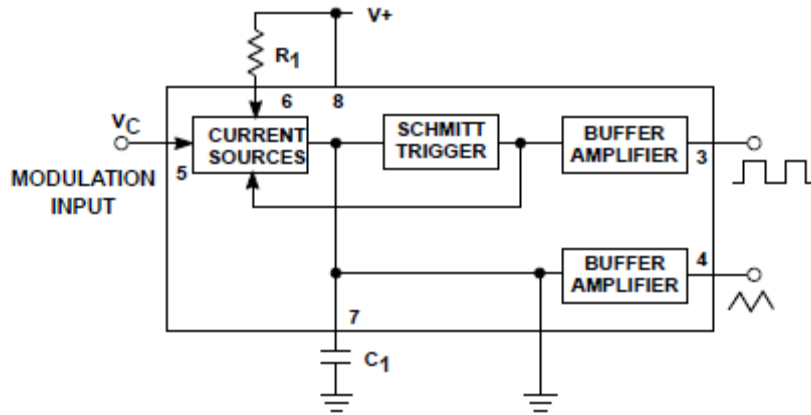
Example PLL ICs:

560 series (560, 561, 562, 564, 565 & 567)

VOLTAGE CONTROLLED OSCILLATOR:

A common type of VCO available in IC form is Signetics NE/SE566. The pin configuration and basic block diagram of 566 VCO are shown in figures below.
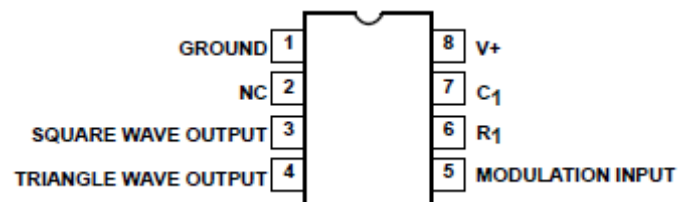
Referring to the circuit in the above figure, the capacitor c_1 is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the voltage v_c applied at the modulating input (pin 5) or by changing the timing resistor R_1 external to the IC chip. The voltage at pin 6 is held at the same voltage as pin 5. Thus, if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_1 and thereby decreasing the charging current.

The voltage across the capacitor C_1 is applied to the inverting input terminal of Schmitt trigger via buffer amplifier. The output voltage swing of the Schmitt trigger is designed to V_{cc} and 0.5 V_{cc}. If $R_a = R_b$ in the positive feedback loop, the voltage at the non-inverting input terminal of Schmitt trigger swings from 0.5 V_{cc} to 0.25 V_{cc}. When the voltage on the capacitor c_1 exceeds 0.5 V_{cc} during charging, the output of the Schmitt trigger goes LOW (0.5 V_{cc}). The capacitor now discharges and when it is at 0.25 V_{cc}, the output of Schmitt trigger goes HIGH (V_{cc}). Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time. This gives a triangular voltage waveform across c_1 which is also available at pin 4. The square wave output of the Schmitt trigger is inverted by buffer amplifier at pin 3. The output waveforms are shown near the pins 4 and 3.
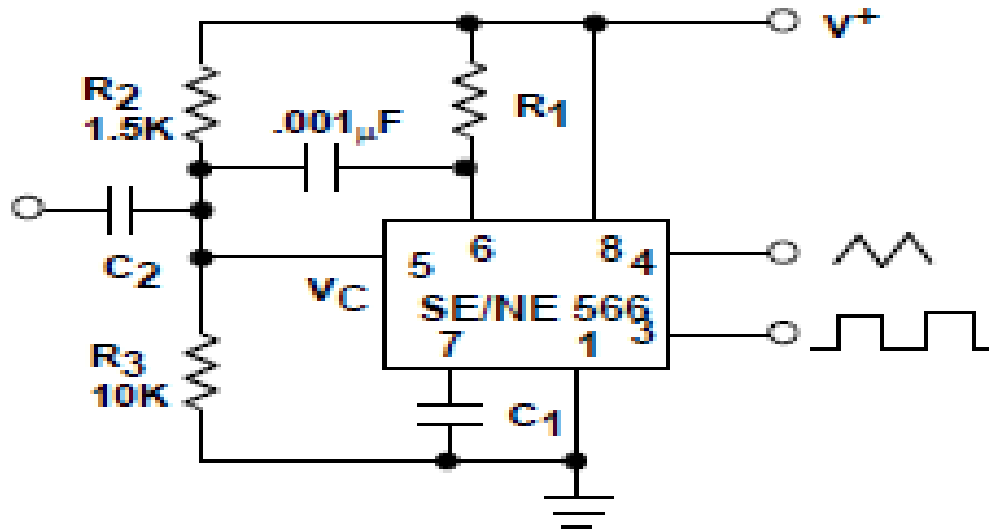
The output frequency of the VCO can be given as follows:

$$f_o = \frac{2\,[(V+) - (V_c)]}{R_1\,C_1\,V+}$$

where V+ is V_{cc}.

The output frequency of the VCO can be changed either by (i) R_1, (ii) c_1 or (iii) the voltage v_c at the modulating input terminal pin 5. The voltage v_c can be varied by connecting a R_1R_2 circuit

as shown in the figure below. The components R_1 and c_1 are first selected so that VCO output frequency lies in the centre of the operating frequency range. Now the modulating input voltage is usually varied from $0.75\ V_{cc}$ to V_{cc} which can produce a frequency variation of about 10 to 1.

MONOLITHIC PHASE LOCKED LOOPS (PLL IC 565):

Pin Configuration of PLL IC 565:

14-Pin DIP Package

Basic Block Diagram Representation of IC 565

NE/SE 565 PLL Block Diagram

The signetics NE/SE 560 series is monolithic phase locked loops. The SE/NE 560, 561, 562, 564, 565 & 567 differ mainly in operating frequency range, poser supply requirements & frequency & bandwidth adjustment ranges. The important electrical characteristics of the 565 PLL are,

- Operating frequency range: 0.001Hz to 500 Khz.
- Operating voltage range: ±6 to ±12v
- Input level required for tracking: 10mv rms min to 3 Vpp max
- Input impedance: 10 K ohms typically.
- Output sink current: 1mA
- Output source current: 10 mA
-

The center frequency of the PLL is determined by the free running frequency of the VCO, which is given by

$$f_{OUT} = \frac{1.2}{4R1C1} \text{ Hz} \text{------------(1)}$$

where R1&C1 are an external resistor & a capacitor connected to pins 8 & 9.

- The VCO free-running frequency f_{OUT} is adjusted externally with R1 & C1 to be at the center of the input frequency range.
- C1 can be any value, R1 must have a value between 2 k ohms and 20 K ohms.
- Capacitor C2 connected between 7 & +V.
- The filter capacitor C2 should be large enough to eliminate variations in the demodulated output voltage in order to stabilize the VCO frequency.
- The lock range f_L & capture range fc of PLL is given by,

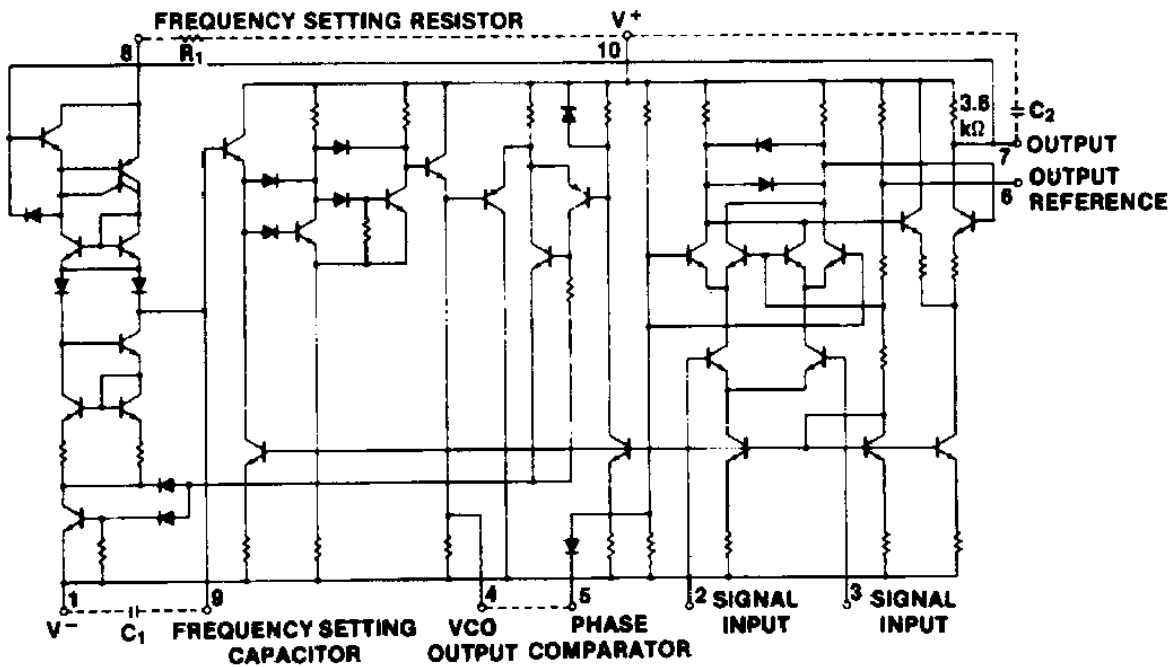$$f_L = \pm \frac{8 \text{ fout}}{V} \text{ Hz } \text{------------------(2)}$$

Where f_{OUT} = free running frequency of VCO (Hz)

  V = (+V)-(-V) volts

$$f_L$$

$$f_C = \pm \left[\; \frac{\text{--------------------}}{(2\Pi)(3.6)(10^3)C_2} \; \right]^{\frac{1}{2}} \text{--------------(3)}$$

The circuit diagram of LM565 PLL

Monolithic PLL IC 565 applications:

The output from a PLL system can be obtained either as the voltage signal $v_c(t)$ corresponding to the error voltage in the feedback loop, or as a frequency signal at VCO output terminal. The voltage output is used in frequency discriminator applications whereas the frequency output is used in signal conditioning, frequency synthesis or clock recovery applications.

Consider the case of voltage output. When PLL is locked to an input frequency, the error voltage $v_c(t)$ is proportional to (f_s-f_o). If the input frequency is varied as in the case of FM signal, v_c will also vary in order to maintain the lock. Thus the voltage output serves as a frequency discriminator which converts the input frequency changes to voltage changes.

In the case of frequency output, if the input signal is comprised of many frequency components corrupted with noise and other disturbances, the PLL can be made to lock, selectively on one particular frequency component at the input. The output of VCO would then regenerate that particular frequency (because of LPF which gives output for beat frequency) and attenuate heavily other frequencies. VCO output thus can be used for regenerating or reconditioning a desired frequency signal (which is weak and buried in noise) out of many undesirable frequency signals. Some of the typical applications of PLL are discussed below.
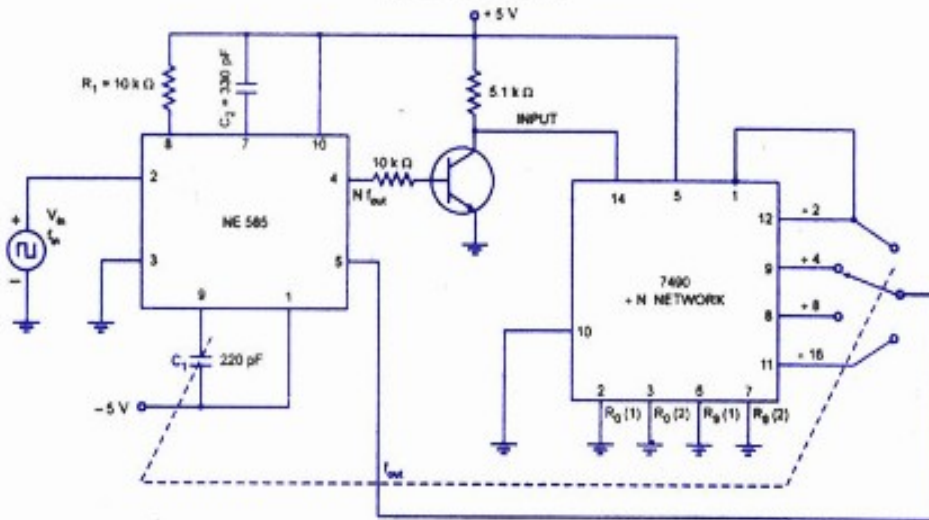
(i)Frequency Multiplier:

- Frequency divider is inserted between the VCO & phase comparator. Since the output of the divider is locked to the f_{IN}, VCO is actually running at a multiple of the input frequency.
- The desired amount of multiplication can be obtained by selecting a proper divide-by-N network, where N is an integer.
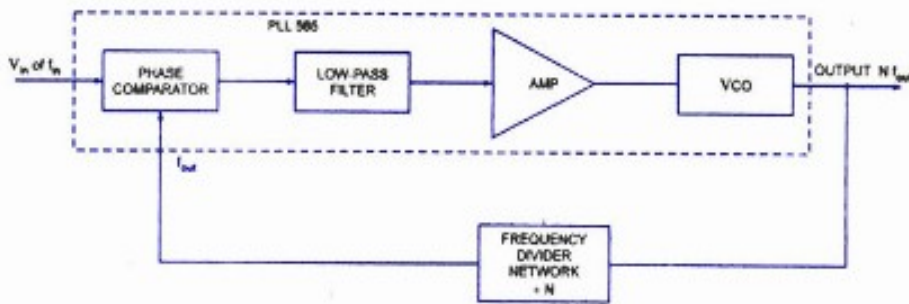
(a) Block Diagram

(b) Connection Diagram For Multiple 4 Frequency Multiplier

(ii)Frequency Shift Keying (FSK) demodulator:

In computer peripheral & radio (wireless) communication the binary data or code is transmitted by means of a carrier frequency that is shifted between two preset frequencies. Since a carrier frequency is shifted between two preset frequencies, the data transmission is said to use a FSK. The frequency corresponding to logic 1 & logic 0 states are commonly called the mark & space frequency.

For example, When transmitting teletype writer information using a modulator-demodulator (modem) a 1070-1270 (mark-space) pair represents the originate signal, while a 2025-2225 Hz (mark-space) pair represents the answer signal.

565 As An FSK Demodulator
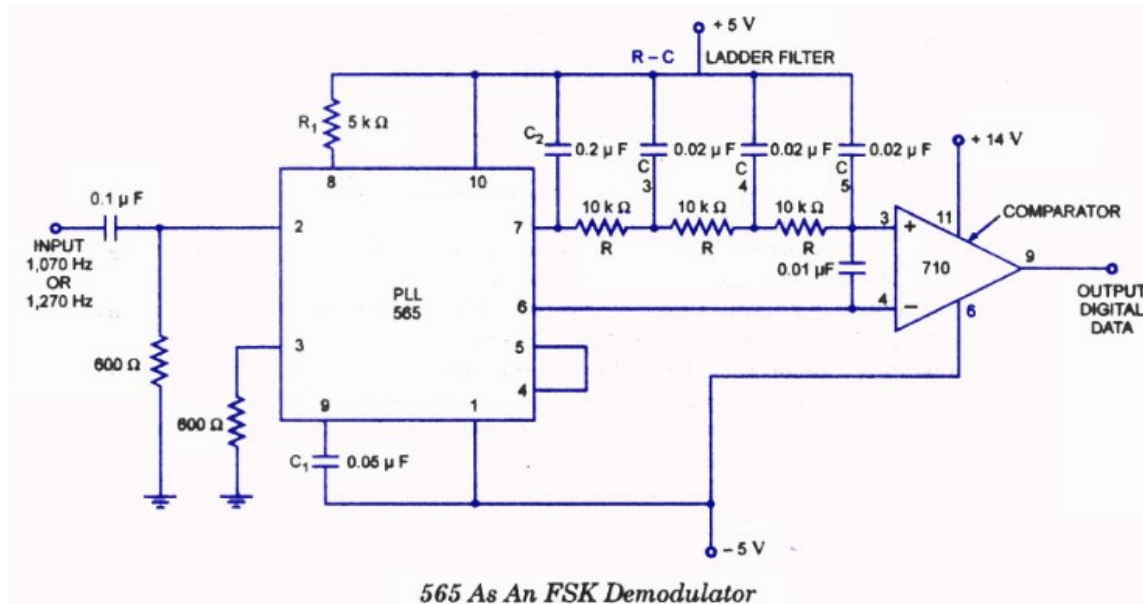
FSK Generator:

- The FSK generator is formed by using a 555 as an astable multivibrator, whose frequency is controlled by the sate of transistor Q1.
- In other words, the output frequency of the FSK generator depends on the logic state of the digital data input.
- 150 Hz is one the standards frequencies at which the data are commonly transmitted.
- When the input is logic 1, the transistor Q1 is off. Under the condition, 555 timer works in its normal mode as an astable multivibrator i.e., capacitor C charges through R_A & R_B to 2/3 Vcc & discharges through R_B to 1/3 Vcc.

  Thus capacitor C charges & discharges between 2/3 Vcc & 1/3 Vcc as long as the input is logic 1.
- The frequency of the output waveform is given by,

$$fo = \frac{1.45}{(R_A + 2R_B)C} = 1070 \text{ Hz (mark frequency)}$$

- When the input is logic 0, (Q1 is ON saturated) which inturn connects the resistance Rc across R_A. This action reduces the charging time of capacitor C1 increases the output frequency, which is given by,

$$1.45$$

$$f_o = \frac{}{(R_A \parallel R_C + 2 R_B)C} = 1270 \text{ Hz (space frequency)}$$

- By proper selection of resistance Rc, this frequency is adjusted to equal the space frequency of 1270 Hz. The difference between the FSK signals of 1070 Hz & 1270 Hz is 200 Hz, this difference is called "frequency shift".
- The output 150 Hz can be made by connecting a voltage comparator between the output of the ladder filter and pin 6 of PLL.
- The VCO frequency is adjusted with R1 so that at $f_{IN} = 1070$ Hz.

FSK Demodulator:

- The output of 555 FSK generator is applied to the 565 FSK demodulator.
- Capacitive coupling is used at the input to remove dc line.
- At the input of 565, the loop locks to the input frequency & tracks it between the 2 frequencies.
- R1 & C1 determine the free running frequency of the VCO, 3 stage RC ladder filter is used to remove the carrier component from the output.

In digital data communication and computer peripheral, binary data is transmitted by means of a carrier frequency which is shifted between two preset frequencies. This type of data transmission is called frequency shift keying (FSK) technique. The binary data can be retrieved using FSK demodulator. The figure below shows FSK demodulator using PLL for tele-typewriter signals of 1070 Hz and 1270 Hz. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output. A three stage filter removes the carrier component and the output signal is made logic compatible by a voltage comparator.
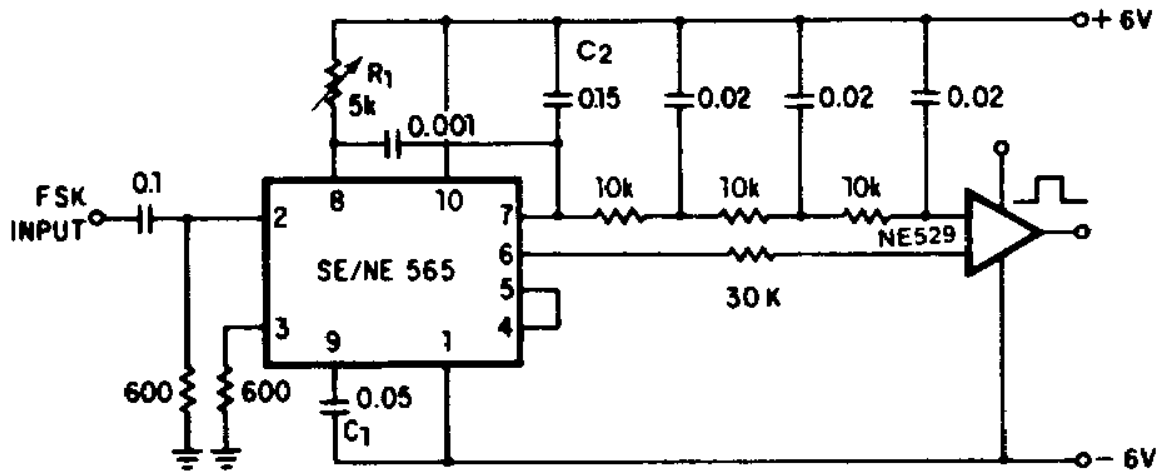
(iii)AM Demodulation:

A PLL may be used to demodulate AM signals as shown in the figure below. The PLL is locked to the carrier frequency of the incoming AM signal. The output of VCO which has the same frequency as the carrier, but unmodulated is fed to the multiplier. Since VCO output is always 90^0 before being fed to the multiplier. This makes both the signals applied to the multiplier and the difference signals, the demodulated output is obtained after filtering high frequency components by the LPF. Since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL AM detector exhibits high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

AM input
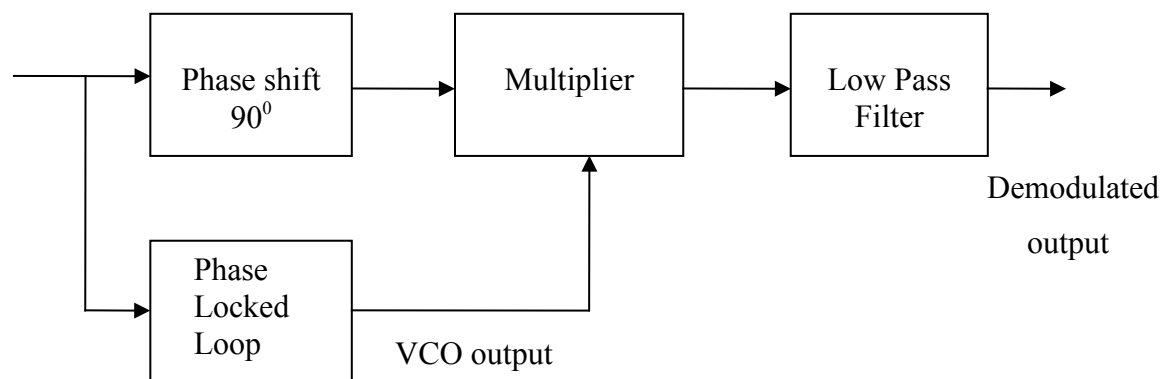
(iv)FM Demodulation:

If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output. The VCO transfer characteristics determine the linearity of the demodulated output. Since, VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulators.

(v)frequency multiplication/division:

The block diagram shown below shows a frequency multiplier/divider using PLL. A divide by N network is inserter between the VCO output and the phase comparator input. In the locked state, the VCO output frequency f_o is given by

$f_o = Nf_s$. The multiplication factor can be obtained by selecting a proper scaling factor N of the counter.

Frequency multiplication can also be obtained by using PLL in its harmonic locking mode. If the input signal is rich in harmonics e.g. square wave, pulse train etc., then the VCO can be directly locked to the n-th harmonic of the input signal without connecting any frequency divider in between. However, as the amplitude of the higher order harmonics becomes less, effective locking may not take place for high values of n. Typically n is kept less than 10.

The circuit of the figure above can also be used for frequency division. Since the VCO output (a square wave) is rich in harmonics, it is possible to lock the m-th harmonic of the VCO output with the input signal f_s. The output fo of VCO is now given by

$f_o = f_s/m$
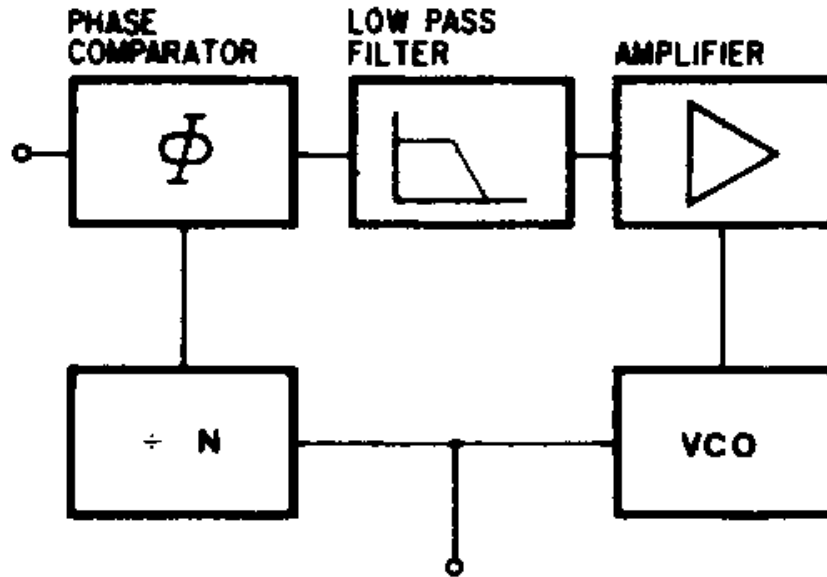
(vi)PLL Frequency Synthesis:

In digital wireless communication systems (GSM, CDMA etc), PLL's are used to provide the Local Oscillator (LO) for up-conversion during transmission, and down-conversion during reception. In most cellular handsets this function has been largely integrated into a single integrated circuit to reduce the cost and size of the handset. However due to the high performance required of base station terminals, the transmission and reception circuits are built with discrete components to achieve the levels of performance required. GSM LO modules are typically built with a Frequency Synthesizer integrated circuit, and discrete resonator VCO's.

Frequency Synthesizer manufacturers include Analog Devices, National Semiconductor and Texas Instruments. VCO manufacturers include Sirenza, Z-Communications, Inc. (Z-COMM) *Principle of PLL synthesizers*

A phase locked loop does for frequency what the Automatic Gain Control does for voltage. It compares the frequencies of two signals and produces an error signal which is proportional to the difference between the input frequencies. The error signal is then low pass filtered and used to drive a voltage-controlled oscillator (VCO) which creates an output frequency. The output frequency is fed through a frequency divider back to the input of the system, producing a negative feedback loop. If the output frequency drifts, the error signal will increase, driving the frequency in the opposite direction so as to reduce the error. Thus the output is *locked* to the frequency at the other input. This input is called the reference and is derived from a crystal oscillator, which is very stable in frequency. The block diagram below shows the basic elements and arrangement of a PLL based frequency synthesizer.
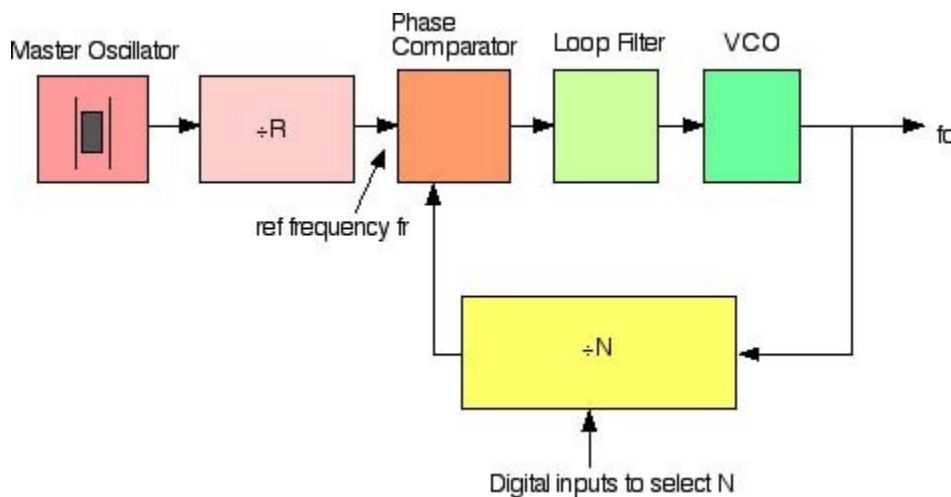
The key to the ability of a frequency synthesizer to generate multiple frequencies is the divider placed between the output and the feedback input. This is usually in the form of a digital counter, with the output signal acting as a clock signal. The counter is preset to some initial count value, and counts down at each cycle of the clock signal. When it reaches zero, the counter output changes state and the count value is reloaded. This circuit is straightforward to implement using flip-flops, and because it is digital in nature, is very easy to interface to other digital components or a microprocessor. This allows the frequency output by the synthesizer to be easily controlled by a digital system.

Example:

Suppose the reference signal is 100 kHz, and the divider can be preset to any value between 1 and 100. The error signal produced by the comparator will only be zero when the output of the divider is also 100 kHz. For this to be the case, the VCO must run at a frequency which is 100 kHz x the divider count value. Thus it will produce an output of 100 kHz for a count of 1, 200 kHz for a count of 2, 1 MHz for a count of 10 and so on. Note that only whole multiples of the reference frequency can be obtained with the simplest integer N dividers. Fractional N dividers are readily available

Practical considerations:

In practice this type of frequency synthesizer cannot operate over a very wide range of frequencies, because the comparator will have a limited bandwidth and may suffer from aliasing problems. This would lead to false locking situations, or an inability to lock at all. In addition, it is hard to make a high frequency VCO that operates over a very wide range. This is due to several factors, but the primary restriction is the limited capacitance range of varactor diodes. However, in most systems where a synthesiser is used, we are not after a huge range, but rather a finite number over some defined range, such as a number of radio channels in a specific band.

Many radio applications require frequencies that are higher than can be directly input to the digital counter. To overcome this, the entire counter could be constructed using high-speed logic such as ECL, or more commonly, using a fast initial division stage called a *prescaler* which reduces the frequency to a manageable level. Since the prescaler is part of the overall division ratio, a fixed prescaler can cause problems designing a system with narrow channel spacings - typically encountered in radio applications. This can be overcome using a dual-modulus prescaler.[11]

Further practical aspects concern the amount of time the system can switch from channel to channel, time to lock when first switched on, and how much noise there is in the output. All of these are a function of the *loop filter* of the system, which is a low-pass filter placed between the output of the frequency comparator and the input of the VCO. Usually the output of a frequency comparator is in the form of short error pulses, but the input of the VCO must be a smooth noise-free DC voltage. (Any noise on this signal naturally causes frequency modulation of the VCO.).

Heavy filtering will make the VCO slow to respond to changes, causing drift and slow response time, but light filtering will produce noise and other problems with harmonics. Thus the design of the filter is critical to the performance of the system and in fact the main area that a designer will concentrate on when building a synthesizer system.

UNIT IV- ANALOG TO DIGITAL & DIGITAL TO ANALOG CONVERTERS

D TO A CONVERTER- SPECIFICATIONS

D/A converters are available with wide range of specifications specified by manufacturer. Some of the important specifications are Resolution, Accuracy, linearity, monotonicity, conversion time, settling time and stability.

Resolution:

Resolution is defined as the number of different analog output voltage levels that can be provided by a DAC. Or alternatively resolution is defined as the ratio of a change in output voltage resulting for a change of 1 LSB at the digital input. Simply, resolution is the value of LSB.

$$\text{Resolution (Volts)} = Vo_{FS} / (2^n - 1) = 1 \text{ LSB increment}$$

Where 'n' is the number of input bits

'Vo_{FS}' is the full scale output voltage.

Example:

Resolution for an 8 – bit DAC for example is said to have

: 8 – bit resolution

: A resolution of 0.392 of full-Scale (1/255)

: A resolution of 1 part in 255.

Thus resolution can be defined in many different ways.

The following table shows the resolution for 6 to 16 bit DACs

S.No.	Bits	Intervals	LSB size (% of full-scale)	LSB size (For a 10 V full-scale)
1.	6	63	1.588	158.8 mV
2.	8	255	0.392	39.2 mV
3.	10	1023	0.0978	9.78 mV
4.	12	4095	0.0244	2.44 mV
5.	14	16383	0.0061	0.61 mV
6.	16	65535	0.0015	0.15 mV

Accuracy:

Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. The ideal converter is the one which does not suffer from any problem. Whereas, the actual converter output deviates due to the drift in component values, mismatches, aging, noise and other sources of errors.

The relative accuracy is the maximum deviation after the gain and offset errors have been removed. Accuracy is also given in terms of LSB increments or percentage of full-scale voltage. Normally, the data sheet of a D/A converter specifies the relative accuracy rather than absolute accuracy.

Linearity:

Linearity error is the maximum deviation in step size from the ideal step size. Some D/A converters are having a linearity error as low as 0.001% of full scale. The linearity of a D/A converter is defined as the precision or exactness with which the digital input is converted into analog output. An ideal D/A converter produces equal increments or step sizes at output for every change in equal increments of binary input.

Monotonicity:

A Digital to Analog converter is said to be monotonic if the analog output increases for an increase in the digital input. A monotonic characteristics is essential in control applications. Otherwise it would lead to oscillations. If a DAC has to be monotonic, the error should be less than $\pm (1/2)$ LSB at each output level. Hence all the D/A converters are designed such that the linearity error satisfies the above condition.

When a D/A Converter doesn't satisfy the condition described above, then, the output voltage may decrease for an increase in the binary input.

Conversion Time:

It is the time taken for the D/A converter to produce the analog output for the given binary input signal. It depends on the response time of switches and the output of the

Amplifier. D/A converters speed can be defined by this parameter. It is also called as setting time.

Settling time:

It is one of the important dynamic parameter. It represents the time it takes for the output to settle within a specified band ± (1/2) LSB of its final value following a code change at the input (Usually a full-scale change). It depends on the switching time of the logic circuitry due to internal parasitic capacitances and inductances. A typical settling time ranges from 100 ns to 10 μs depending on the word length and type of circuit used.

Stability:

The ability of a DAC to produce a stable output all the time is called as Stability. The performance of a converter changes with drift in temperature, aging and power supply variations. So all the parameters such as offset, gain, linearity error & monotonicity may change from the values specified in the datasheet. Temperature sensitivity defines the stability of a D/A converter.

DIGITAL TO ANALOG CONVERSION

A DAC converts an abstract finite-precision number (usually a fixed-point binary number) into a concrete physical quantity (e.g., a voltage or a pressure). In particular, DACs are often used to convert finite-precision time series data to a continually-varying physical signal.

A typical DAC converts the abstract numbers into a concrete sequence of impulses that are then processed by a reconstruction filter using some form of interpolation to fill in data between the impulses. Other DAC methods (e.g., methods based on Delta-sigma modulation) produce a pulse-density modulated signal that can then be filtered in a similar way to produce a smoothly-varying signal.

By the Nyquist–Shannon sampling theorem, sampled data can be reconstructed perfectly provided that its bandwidth meets certain requirements (e.g., a baseband signal with bandwidth less than the Nyquist frequency). However, even with an ideal reconstruction filter, digital sampling introduces quantization that makes perfect reconstruction practically impossible. Increasing the digital resolution (i.e., increasing the number of bits used in each sample) or introducing sampling dither can reduce this error.

DACs are at the beginning of the analog signal chain, which makes them very important to system performance. The most important characteristics of these devices are:

Resolution: This is the number of possible output levels the DAC is designed to reproduce. This is usually stated as the number of bits it uses, which is the base two logarithm of the number of levels. For instance a 1 bit DAC is designed to reproduce 2 (2^1) levels while an 8 bit DAC is designed for 256 (2^8) levels. Resolution is related to the **effective number of bits**(ENOB) which is a measurement of the actual resolution attained by the DAC.

Maximum sampling frequency: This is a measurement of the maximum speed at which the DACs circuitry can operate and still produce the correct output. As stated in the Nyquist–Shannon sampling theorem, a signal must be sampled at over twice the frequency of the desired signal. For instance, to reproduce signals in all the audible spectrum, which includes frequencies of up to 20 kHz, it is necessary to use DACs that operate at over 40 kHz. The CD standard samples audio at 44.1 kHz, thus DACs of this frequency are often used. A common frequency in cheap computer sound cards is 48 kHz—many work at only this frequency, offering the use of other sample rates only through (often poor) internal resampling.

Monotonicity: This refers to the ability of a DAC's analog output to move only in the direction that the digital input moves (i.e., if the input increases, the output doesn't dip before asserting the correct output.) This characteristic is very important for DACs used as a low frequency signal source or as a digitally programmable trim element.

THD+N: This is a measurement of the distortion and noise introduced to the signal by the DAC. It is expressed as a percentage of the total power of unwanted harmonic distortion and noise that accompany the desired signal. This is a very important DAC characteristic for dynamic and small signal DAC applications.

Dynamic range: This is a measurement of the difference between the largest and smallest signals the DAC can reproduce expressed in decibels. This is usually related to DAC resolution and noise floor.

Other measurements, such as phase distortion and sampling period instability, can also be very important for some applications.

BINARY-WEIGHTED RESISTOR DAC

The binary-weighted-resistor DAC employs the characteristics of the inverting summer Op Amp circuit. In this type of DAC, the output voltage is the inverted sum of all the input voltages. If the input resistor values are set to multiples of two: 1R, 2R and 4R, the output voltage would be equal to the sum of V1, V2/2 and V3/4. V1 corresponds to the most significant bit (MSB) while V3 corresponds to the least significant bit (LSB).
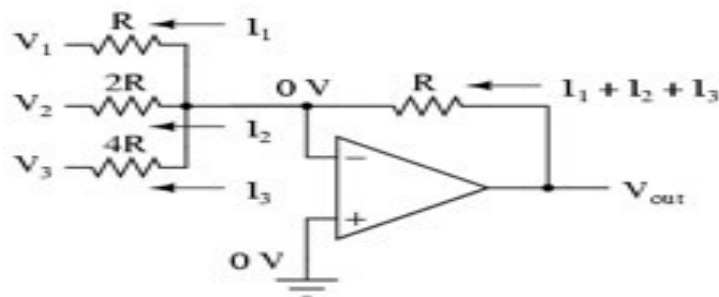
$$V_{out} = -(V_1 + \frac{V_2}{2} + \frac{V_3}{4})$$

The circuit for a 4-bit DAC using binary weighted resistor network is shown below:
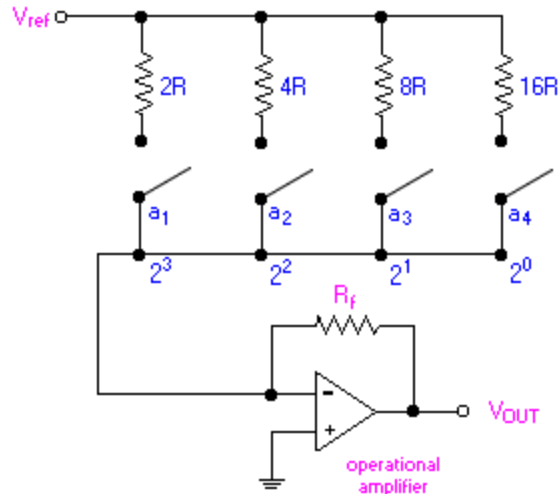
The binary inputs, a_i (where i = 1, 2, 3 and 4) have values of either 0 or 1. The value, 0, represents an open switch while 1 represents a closed switch.

The operational amplifier is used as a summing amplifier, which gives a weighted sum of the binary input based on the voltage, V_{ref}.

For a 4-bit DAC, the relationship between V_{out} and the binary input is as follows:

$$
\begin{aligned}
V_{OUT} &= -iR_f \\
&= -\left[V_{ref}\left(\frac{a_1}{2R} + \frac{a_2}{4R} + \frac{a_3}{8R} + \frac{a_4}{16R}\right)\right]R_f \\
&= -\frac{V_{ref}R_f}{R}\left(\frac{a_1}{2} + \frac{a_2}{4} + \frac{a_3}{8} + \frac{a_4}{16}\right) \\
&= -\frac{V_{ref}R_f}{R}\left(\frac{a_1}{2^1} + \frac{a_2}{2^2} + \frac{a_3}{2^3} + \frac{a_4}{2^4}\right)
\end{aligned}
$$

The negative sign associated with the analog output is due to the connection to a summing amplifier, which is a polarity-inverting amplifier. When a signal is applied to the latter type of amplifier, the polarity of the signal is reversed (i.e. a + input becomes -, or vice versa).

For a n-bit DAC, the relationship between V_{out} and the binary input is as follows:

$$V_{OUT} = -\frac{V_{ref}\,R_f}{R}\sum_{i=1}^{n}\frac{a_i}{2^i}$$

Analog Voltage Output: An Example

As an example, consider the following given parameters: $V_{ref} = 5$ V, $R = 0.5$ k and $R_f = 1$ k. The voltage outputs, V_{out}, corresponding to the respective binary inputs are as follows:

Digital Input				V_{OUT} (Volts)
a_1	a_2	a_3	a_4	
0	0	0	0	0
0	0	0	1	- 0.625
0	0	1	0	- 1.250
0	0	1	1	- 1.875
0	1	0	0	- 2.500
0	1	0	1	- 3.125
0	1	1	0	- 3.750
0	1	1	1	- 4.375
1	0	0	0	- 5.000
1	0	0	1	- 5.625
1	0	1	0	- 6.250
1	0	1	1	- 6.875
1	1	0	0	- 7.500
1	1	0	1	- 8.125
1	1	1	0	- 8.750

| 1 | 1 | 1 | 1 | - 9.375 |

Table 1: Voltage Output of 4-bit DAC using Binary Weighted Resistor Network

The LSB, which is also the incremental step, has a value of - 0.625 V while the MSB or the full scale has a value of - 9.375 V.

Practical Limitations:

- The most significant problem is the large difference in resistor values required between the LSB and MSB, especially in the case of high resolution DACs (i.e. those that has large number of bits). For example, in the case of a 12-bit DAC, if the MSB is 1 k▶, then the LSBis a staggering 2 M▶.
- The maintanence of accurate resistances over a large range of values is problematic. With the current IC fabrication technology, it is difficult to manufacture resistors over a wide resistance range that maintain an accurate ratio especially with variations in temperature.

R-2R LADDER DAC

An enhancement of the binary-weighted resistor DAC is the R-2R ladder network. This type of DAC utilizes Thevenin's theorem in arriving at the desired output voltages. The R-2R network consists of resistors with only two values - R and 2xR. If each input is supplied either 0 volts or reference voltage, the output voltage will be an analog equivalent of the binary value of the three bits. VS2 corresponds to the most significant bit (MSB) while VS0 corresponds to the least significant bit (LSB).
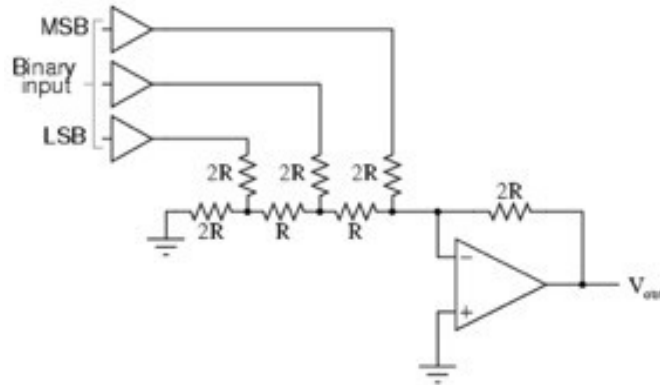
$$Vout = -(VMSB + Vn + VLSB) = -(VRef + VRef/2 + VRef/4)$$

The R/2R DAC

An alternative to the binary-weighted-input DAC is the so-called R/2R DAC, which uses fewer unique resistor values. A disadvantage of the former DAC design was its requirement of several different precise input resistor values: one unique value per binary input bit. Manufacture may be simplified if there are fewer different resistor values to purchase, stock, and sort prior to assembly.

Of course, we could take our last DAC circuit and modify it to use a single input resistance value, by connecting multiple resistors together in series:
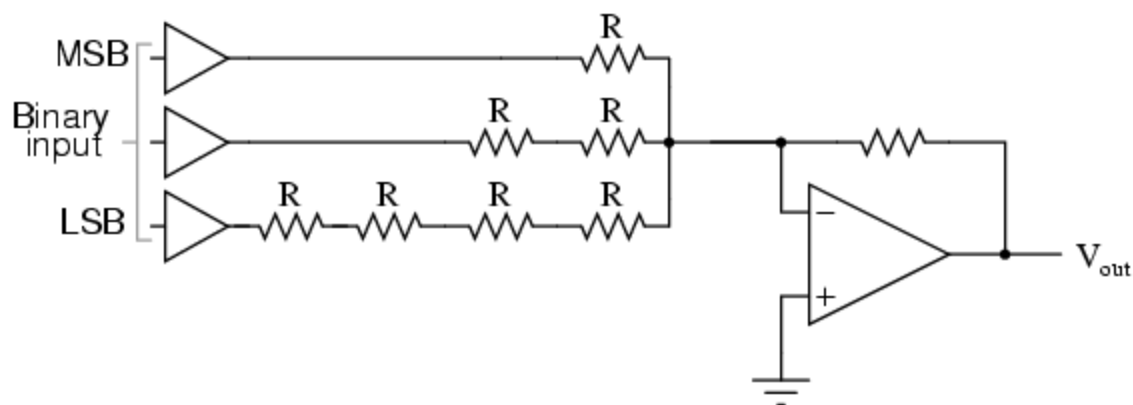
Unfortunately, this approach merely substitutes one type of complexity for another: volume of components over diversity of component values. There is, however, a more efficient design

methodology. By constructing a different kind of resistor network on the input of our summing circuit, we can achieve the same kind of binary weighting with only two kinds of resistor values, and with only a modest increase in resistor count. This "ladder" network looks like this:

R/2R "ladder" DAC
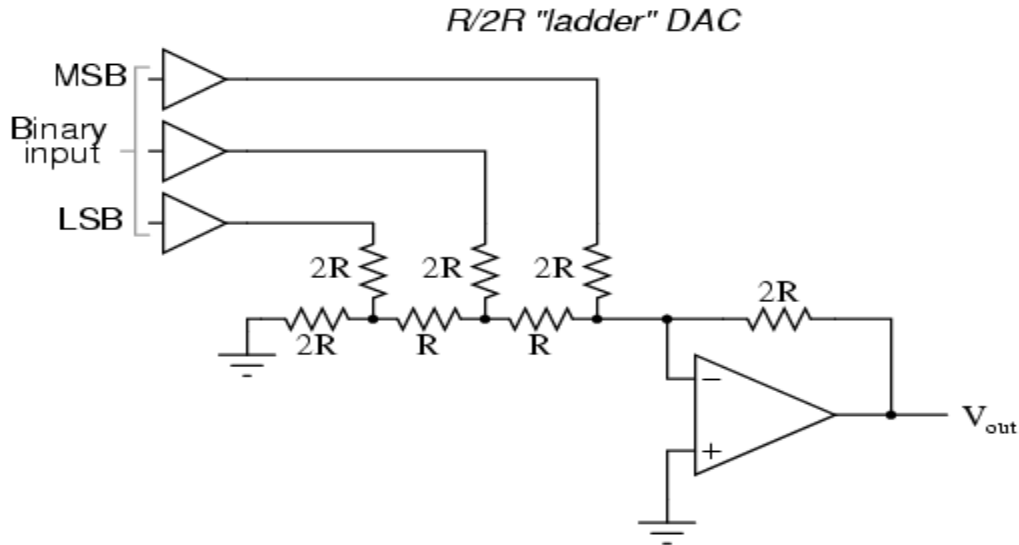
Mathematically analyzing this ladder network is a bit more complex than for the previous circuit, where each input resistor provided an easily-calculated gain for that bit. For those who are interested in pursuing the intricacies of this circuit further, you may opt to use Thevenin's theorem for each binary input (remember to consider the effects of the *virtual ground*), and/or use a simulation program like SPICE to determine circuit response. Either way, you should obtain the following table of figures:

Binary	Output voltage
000	0.00 V
001	-1.25 V
010	-2.50 V
011	-3.75 V
100	-5.00 V
101	-6.25 V

```
-------------------------------
|  110  |    -7.50 V   |
-------------------------------
|  111  |    -8.75 V   |
-------------------------------
```

As was the case with the binary-weighted DAC design, we can modify the value of the feedback resistor to obtain any "span" desired. For example, if we're using +5 volts for a "high" voltage level and 0 volts for a "low" voltage level, we can obtain an analog output directly corresponding to the binary input (011 = -3 volts, 101 = -5 volts, 111 = -7 volts, etc.) by using a feedback resistance with a value of 1.6R instead of 2R.

INVERTED OR CURRENT MODE DAC

As the name implies, Current mode DACs operates based on the ladder currents. The ladder is formed by resistance R in the series path and resistance 2R in the shunt path. Thus the current is divided into $i1$, $i2$, $i3$ …………in in each arm. The currents are either diverted to the ground bus (io) or to the Virtual-ground bus ($\overline{io}$).
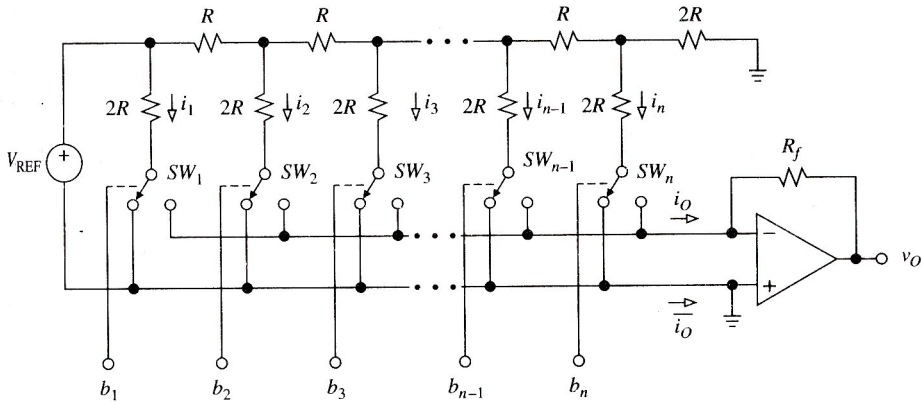
The currents are given as

$i1 = VREF/2R = (VREF/R) 2^{-1}$, $i2 = (VREF)/2)/2R = (VREF/R) 2^{-2}$ .... $i_n = (VREF/R) 2^{-n}$.

And the relationship between the currents are given as

$$i2 = i_1/2$$

$$i3 = i_1/4$$

$$i4 = i_1/8$$

$$in = i_1/2^{n-1}$$

Using the bits to identify the status of the switches, and letting $V_0 = -R_f i_o$ gives

$$V_0 = - (R_f/R)\ V_{REF}\ (b_1 2^{-1} + b_2 2^{-2} + \ldots\ldots.. + b_n 2^{-n})$$

The two currents io and $\overline{io}$ are complementary to each other and the potential of io bus must be sufficiently close to that of the $\overline{io}$ bus. Otherwise, linearity errors will occur. The final op-amp is used as current to voltage converter.

Advantages

1. The major advantage of current mode D/A converter is that the voltage change across each switch is minimal. So the charge injection is virtually eliminated and the switch driver design is made simpler.

2. In Current mode or inverted ladder type DACs, the stray capacitance do not affect the speed of response of the circuit due to constant ladder node voltages. So improved speed performance.

VOLTAGE MODE DAC

This is the alternative mode of DAC and is called so because, the 2R resistance in the shunt path is switched between two voltages named as V_L and V_H. The output of this DAC is obtained from the leftmost ladder node. As the input is sequenced through all the possible binary state starting from All 0s (0…..0) to all 1s (1…..1). The voltage of this node changes in steps of $2^{-n} (V_H - V_L)$ from the minimum voltage of $Vo = V_L$ to the maximum of $Vo = V_H - 2^{-n} (V_H - V_L)$.
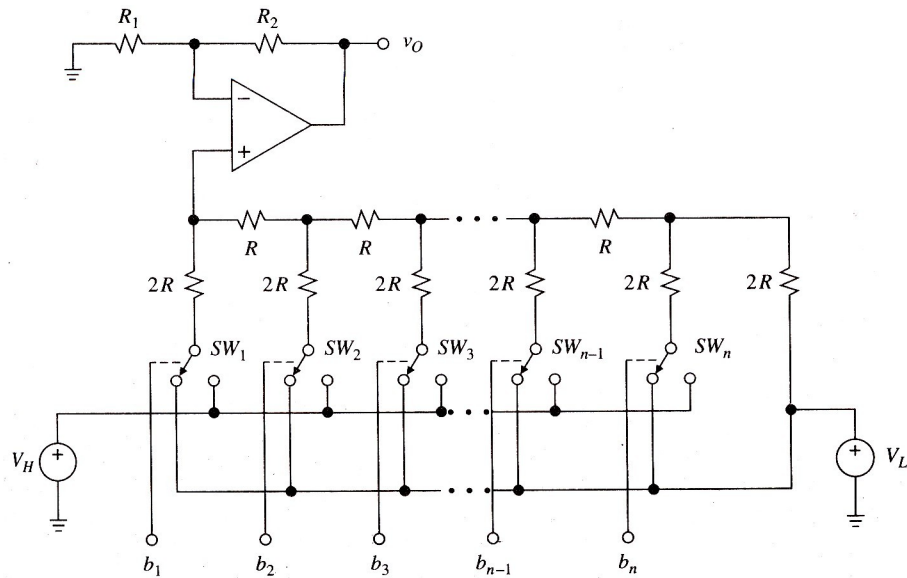
The diagram also shows a non-inverting amplifier from which the final output is taken. Due to this buffering with a non- inverting amplifier, a scaling factor defined by $K = 1 + (R_2/R_1)$ results.

Advantages

1. The major advantage of this technique is that it allows us to interpolate between any two voltages, neither of which need not be a zero.

2. More accurate selection and design of resistors R and 2R are possible and simple construction.

3. The binary word length can be easily increased by adding the required number or
 R-2R sections.

SWITCHES FOR DAC

The Switches which connects the digital binary input to the nodes of a D/A converter is an electronic switch. Although switches can be made of using diodes, Bipolar junction Transistors, Field Effect transistors or MOSFETs, there are four main configurations used as switches for DACs. They are

i) Switches using overdriven Emitter Followers.

ii) Switches using MOS Transistor- Totem pole MOSFET Switch and CMOS Inverter Switch.

iii) CMOS switch for Multiplying type DACs .

iv) CMOS Transmission gate switches.

These configurations are used to ensure the high speed switching operations for different types of DACs.

Switches using overdriven Emitter Followers:

The bipolar transistors have a negligible resistance when they are operated in saturation. The bipolar transistor operating in saturation region indicates a minimum resistance and thus represents ON condition. When they are operating in cut-off region indicates a maximum resistance and thus represents OFF condition.

The circuit shown here is the arrangement of two transistors connected as emitter followers. A silicon transistor operating in saturation will have a offset voltage of 0.2V dropped across them. To have a zero offset voltage condition, the transistors must be overdriven because the saturation factor becomes negative. The two transistors Q_1(NPN) and Q_2(PNP) acts as a double pole switch. The bases of the transistors are driven by +5.75V and -5.75V.

Case 1:

When $V_{B1} = V_{B2} = +5.75V$, Q_1 is in saturation and Q_2 is OFF. And $V_E \approx 5V$ with

$V_{BE1} = V_{BE2} = 0.75V$

Case 2:

When $V_{B1} = V_{B2} = -5.75V$, Q_2 is in saturation and Q_1 is OFF. And $V_E \approx -5V$ with

$V_{BE1} = V_{BE2} = 0.75V$

Thus the terminal B of the resistor R_e is connected to either -5V or +5V depending on the input bit.

Switches using MOS transistor:

i) Totem pole MOSFET Switch:

As shown in the figure, the totem pole MOSFET Switch is connected in series with resistors of R-2R network. The MOSFET driver is connected to the inverting terminal of the summing op-amp. The complementary outputs Q and $\overline{Q}$ drive the gates of the MOSFET M_1 and M_2 respectively. The SR flipflop holds one bit of digital information of the binary word under conversion. Assuming the negative logic (-5V for logic 1 and +5V for logic 0) the operation is given as two cases.

Case 1:

When the bit line is 1 with S=1 and R=0 makes Q=1 and $\overline{Q}$=0. This makes the transistor M_1 ON, thereby connecting the resistor R to reference voltage -V_R. The transistor M_2 remains in OFF condition.

Case 2:

When the bit line is 0 with S=0 and R=1 makes Q=0 and $\overline{Q}$=1. This makes the transistor M_2 ON, thereby connecting the resistor R to Ground. The transistor M_1 remains in OFF condition.

ii) CMOS Inverter Switch:

The figure of CMOS inverter is shown here. It consists of a CMOS inverter connected with an op-amp acting as a buffer. The buffer drives the resistor R with a very low output impedance. Assuming positive logic (+5V for logic 1 and 0V for logic 0), the operation can be explained in two cases.

Case1:

When the complement of the bit line $\overline{Q}$ is low, M_1 becomes ON connecting V_R to the non-inverting input of the op-amp. This drives the resistor R HIGH.

Case2:

When the complement of the bit line $\overline{Q}$ is high, M_2 becomes ON connecting Ground to the non-inverting input of the op-amp. This pulls the resistor R LOW (to ground).

CMOS switch for Multiplying type DACs:

The circuit diagram of CMOS Switch is shown here. The heart of the switching element is formed by transistors M_1 and M_2. The remaining transistors accept TTl or CMOS compatible logic inputs and provides the anti-phase gate drives for the transistors M_1 and M_2. The operation for the two cases is as follows.

Case 1:

When the logic input is 1, M_1 is ON and M_2 is OFF. Thus current I_K is diverted to Io' bus.

Case 2:

When the logic input is 0, M_2 is ON and M_1 is OFF. Thus current I_K is diverted to Io bus.

CMOS Transmission gate switches:

The disadvantage of using individual NMOS and PMOS transistors are threshold voltage drop (NMOS transistor passing only minimum voltage of V_R - V_{TH} and PMOS transistor passing

minimum voltage of V_{TH}). This is eliminated by using transmission gates which uses a parallel connection of both NMOS and PMOS. The arrangement shown here can pass voltages from V_R to 0V acting as a ideal switch. The following cases explain the operation.

Case 1:

When the bit-line b_k is HIGH, both transistors M_n and M_p are ON, offering low resistance over the entire range of bit voltages.

Case 2:

When the bit-line b_k is LOW, both the transistors are OFF, and the signal transmission is inhibited (Withdrawn).

Thus the NMOS offers low resistance in the lower portion of the signal and PMOS offers low resistance in the upper portion of the signal. As a combination, they offer a low parallel resistance throughout the operating range of voltage. Wide varieties of these kinds of switches were available. Example: CD4066 and CD4051.

HIGH SPEED SAMPLE AND HOLD CIRCUITS

Introduction:

Sample-and-hold (S/H) is an important analog building block with many applications, including analog-to-digital converters (ADCs) and switched-capacitor filters. The function of the S/H circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing.

Taking advantages of the excellent properties of MOS capacitors and switches, traditional switched capacitor techniques can be used to realize different S/H circuits [1]. The simplest S/H circuit in MOS technology is shown in Figure 1, where *Vin* is the input signal, *M1* is an MOS transistor operating as the sampling switch, *Ch* is the hold capacitor, *ck* is the clock signal, and *Vout* is the resulting sample-and-hold output signal.

Ch

As depicted by Figure 1, in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward. Whenever
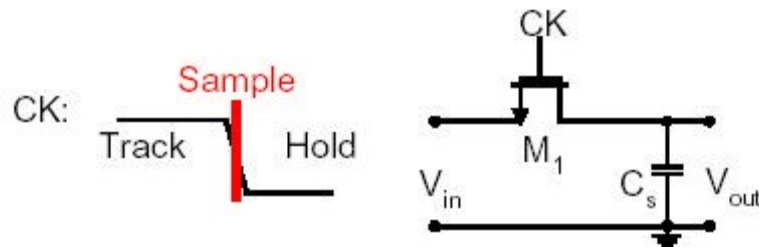
Figure 1: Simplest sample-and-hold circuit in MOS technology.

As depicted by Figure 1, in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward. Whenever *ck* is high, the MOS switch is on, which in turn allows *Vout* to track *Vin*. On the other hand, when *ck* is low, the MOS switch is off. During this time, *Ch* will keep *Vout* equal to the value of *Vin* at the instance when *ck* goes low. Unfortunately, in reality, the performance of this S/H circuit is not as ideal as described above. The two major types of errors occur. They are charge injection and clock feed through, that are associated with this S/H implementation. Three new S/H techniques, all of which try to minimize the errors caused by charge injection and/or clock feed through.

Alternative CMOS Sample-and-Hold Circuits:
This section covers three alternative CMOS S/H circuits that are developed with the intention to minimize charge injection and/or clock feedthrough.
Series Sampling:
The S/H circuit of Figure 1 is classified as parallel sampling because the hold capacitor is in parallel with the signal. In parallel sampling, the input and the output are dc-coupled. On the other hand, the S/H circuit shown in Figure 2 is referred to as series sampling because the hold capacitor is in series with the signal.
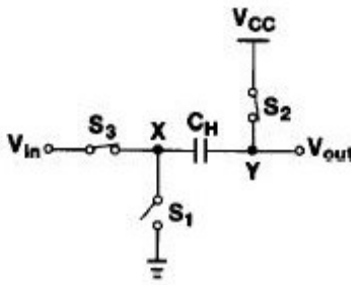
Figure 2: Series sampling.

When the circuit is in sample mode, both switches $S2$ and $S3$ are on, while $S1$ is off. Then, $S2$ is turned off first, which means $Vout$ is equal to VCC (or VDD for most circuits) and the voltage drop across Ch will be $VCC – Vin$. Subsequently, $S3$ is turned off and $S1$ is turned on simultaneously. By grounding node X, $Vout$ is now equal to $VCC – Vin$, and the drop from VCC to $VCC – Vin$ is equal to the instantaneous value of the input.

As a result, this is actually an inverted S/H circuit, which requires inversion of the signal at a later stage. Since the hold capacitor is in series with the signal, series sampling can isolate the common-mode levels of the input and the output. This is one advantage of series sampling over parallel sampling. In addition, unlike parallel sampling, which suffers from signal-dependent charge injection, series sampling does not exhibit such behavior because $S2$ is turned off before $S3$. Thus, the fact that the gate-to-source voltage, VGS, of $S2$ is constant means that charge injection coming from $S2$ is also constant (as opposed to being signal-dependent), which means this error can be easily eliminated through differential operation.

On the other hand, series sampling suffers from the nonlinearity of the parasitic capacitance at node Y. This parasitic capacitance introduces distortion to the sample-and hold value, thus mandating that Ch be much larger than the parasitic capacitance. On top of this disadvantage, the settling time of the S/H circuit during hold mode is longer for series sampling than for parallel sampling. The reason for this is because the value of

Vout in series sampling is being reset to *VCC* (or *VDD*) for every sample, but this is not the case for parallel sampling.

Switched Op-Amp Based Sample-and-Hold Circuit:

This S/H technique takes advantage of the fact that when a MOS transistor is in the saturation region, the channel is pinched off and disconnected from the drain. Therefore, if the hold capacitor is connected to the drain of the MOS transistor, charge injection will only go to the source junction, leaving the drain unaffected. Based on this concept, a switched op-amp (SOP) based S/H circuit, as shown in Figure 3.
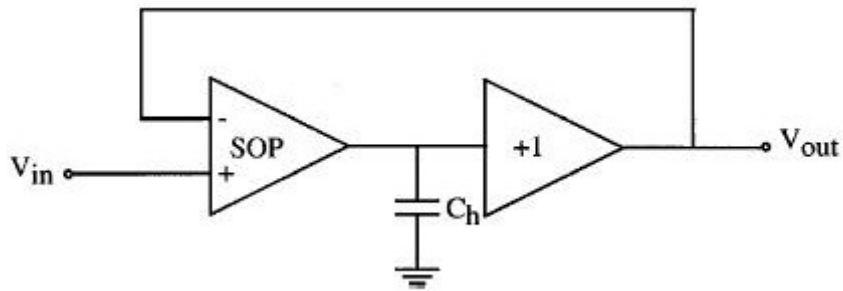
Figure 3: Switched op-amp based sample and hold circuit.

During sample mode, the SOP behaves just like a regular op-amp, in which the value of the output follows the value of the input. During hold mode, the MOS transistors at the output node of the SOP are turned off while they are still operating in saturation, thus preventing any channel charge from flowing into the output of the SOP. In addition, the SOP is shut off and its output is held at high impedance, allowing the charge on *Ch* to be preserved throughout the hold mode. On the other hand, the output buffer of this S/H circuit is always operational during sample and hold mode and is always providing the voltage on *Ch* to the output of the S/H circuit.

With the increasing demand for high-resolution and high-speed in date acquisition systems, the performance of the S/H circuits is becoming more and more important. This is especially true in ADCs since the performance of S/H circuits greatly affects the speed and accuracy of ADCs. The fastest S/H circuits operate in open loop, but when such circuits are implemented in CMOS technology, their accuracy is low. S/H circuits

that operate in closed loop configuration can achieve high resolution, but their requirements for high gain circuit block, such as an op-amp, limits the speed of the circuits. As a result, better and faster S/H circuits must be developed.

At the same time, the employment of low-voltage in VLSI technology requires that the analog circuits be low-voltage as well. As a result of this, new researches in analog circuits are now shifted from voltage-mode to current-mode. The advantages of current mode circuits include low-voltage, low-power, and high-speed. Therefore, future researches of S/H circuit should also shift toward current-mode S/H techniques.
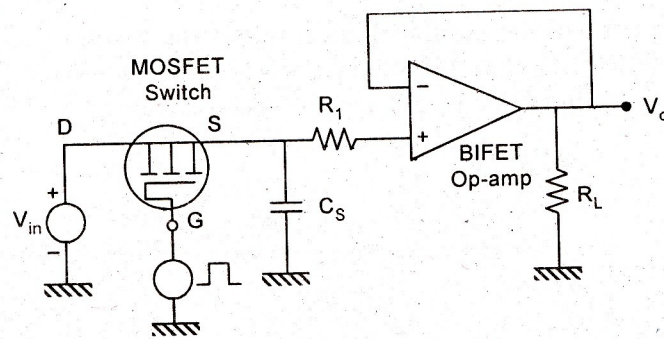
The above figure shows a sample and hold circuit with MOSFET as Switch acting as a sampling device and also consists of a holding capacitor Cs to store the sample values until the next sample comes in. This is a high speed circuit as it is apparent that CMOS switch has a very negligible propagation delay.

Sample-and-hold (S/H) is an important analog building block that has many applications. The simplest S/H circuit can be constructed using only one MOS transistor and one hold capacitor. However, due to the limitations of the MOS transistor switches, errors due to charge injection and clock feed through restrict the performance of S/H circuits. As a result, different S/H techniques and architectures are developed with the intention to reduce or eliminate these errors. Three of these alternative S/H circuits: series sampling, SOP based S/H circuit, and bottom plate S/H circuit with bootstrapped switch, more new S/H techniques and architectures need to be proposed in order

to meet the increasing demand for high-speed, low-power, and low voltage S/H circuits for data acquisition systems.

LF 398 IC- Functional Diagram
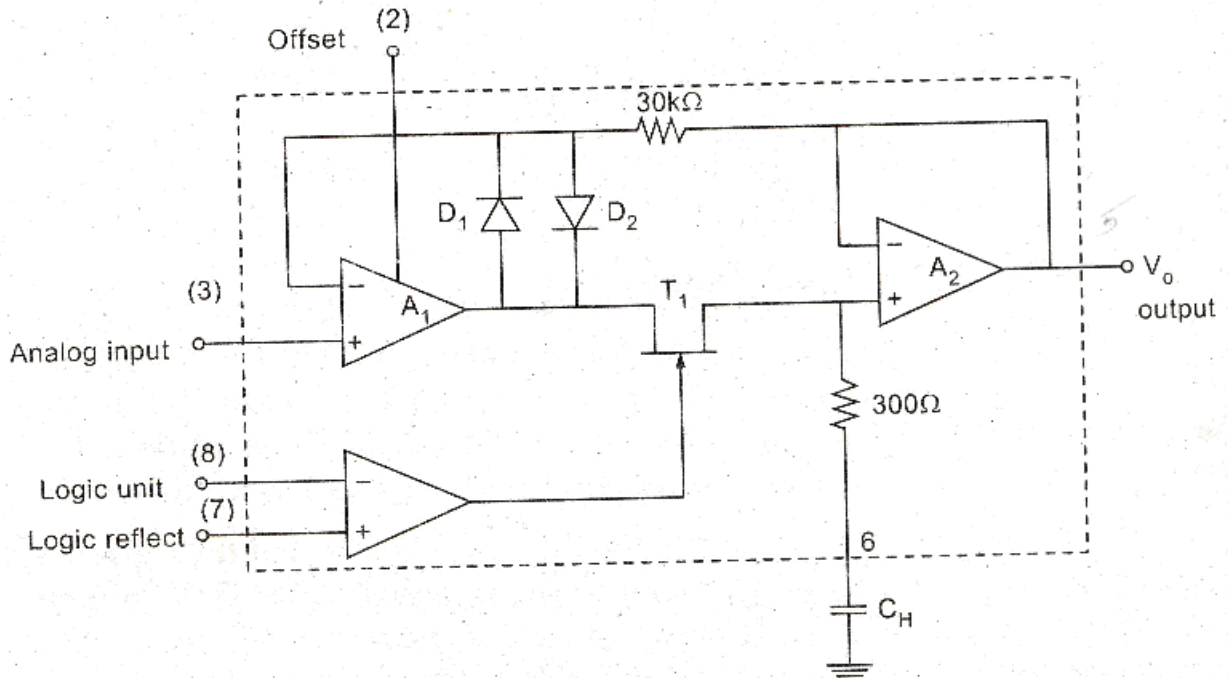
Connection Diagram
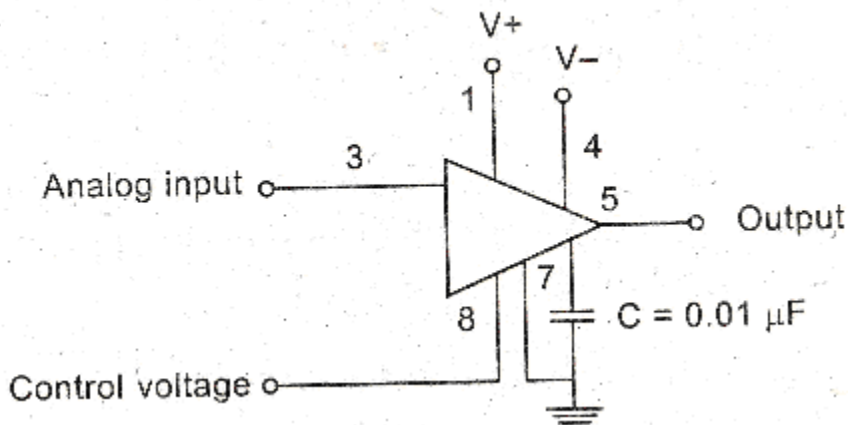
A TO D CONVERTER- SPECIFICATIONS

Like DAC, ADCs are also having many important specifications. Some of them are Resolution, Quantization error, Conversion time, Analog error, Linearity error, DNL error, INL error & Input voltage range.

Resolution:

The resolution refers to the finest minimum change in the signal which is accepted for conversion, and it is decided with respect to number of bits. It is given as $1/2^n$, where 'n' is the number of bits in the digital output word. As it is clear, that the resolution can be improved by increasing the number of bits or the number of bits representing the given analog input voltage.

Resolution can also be defined as the ratio of change in the value of input voltage V_i, needed to change the digital output by 1 LSB. It is given as

$$\text{Resolution} = Vi_{FS} / (2^n - 1)$$

Where 'V_{iFS}' is the full-scale input voltage.

'n' is the number of output bits.

Quantization error:

If the binary output bit combination is such that for all the values of input voltage V_i between any two voltage levels, there is a unavoidable uncertainty about the exact value of V_i when the output is a particular binary combination. This uncertainty is termed as quantization error. Its value is $\pm$ (1/2) LSB. And it is given as,

$$Q_E = Vi_{FS} / 2(2^n - 1)$$

Where 'Vi_{FS}' is the full-scale input voltage

'n' is the number of output bits.

Maximum the number of bits selected, finer the resolution and smaller the quantization error.

Conversion Time:

It is defined as the total time required for an A/D converter to convert an analog signal to digital output. It depends on the conversion technique and propagation delay of the circuit components.

Analog error:

An error occurring due to the variations in DC switching point of the comparator, resistors, reference voltage source, ripples and noises introduced by the circuit components is termed as Analog error.

Linearity Error:

It is defined as the measure of variation in voltage step size. It indicates the difference between the transitions for a minimum step of input voltage change. This is normally specified as fraction of LSB.

DNL (Differential Non-Linearity) Error:

The analog input levels that trigger any two successive output codes should differ by 1 LSB. Any deviation from this 1 LSB value is called as DNL error.

INL (Integral Non-Linearity Error:

The deviation of characteristics of an ADC due to missing codes causes INL error. The maximum deviation of the code from its ideal value after nulling the offset and gain errors is called as Integral Non-Linearity Error.

Input Voltage Range:

It is the range of voltage that an A/D converter can accept as its input without causing any overflow in its digital output.

<div align="center">

ANALOG SWITCHES

</div>

There were two types of analog switches. Series and Shunt switch. The Switch operation is shown for both the cases $V_{GS}=0$ $V_{GS}= V_{Gs(off)}$

(i) Series switch

(ii) At $V_{GS} = 0$

(iii) At $V_{GS} = V_{GS(OFF)}$

Fig.4.2

(i) Shunt switch

(ii) At $V_{GS} = 0$ $R_{DS} \ll R_D$

Fig.4.1

(iii) At $V_{GS} = V_{GS(OFF)}$ $R_{DS} \approx \infty$
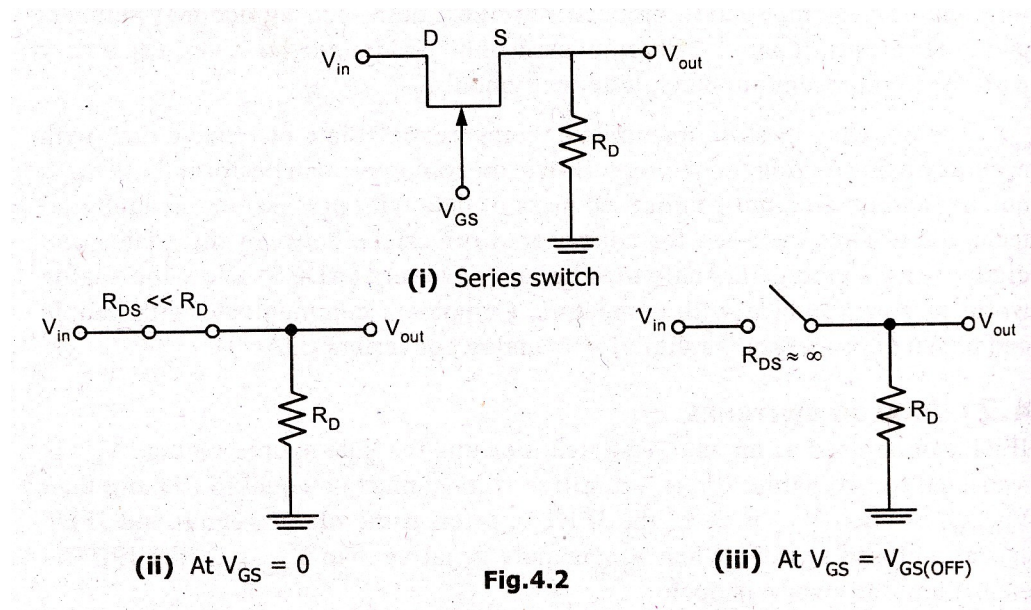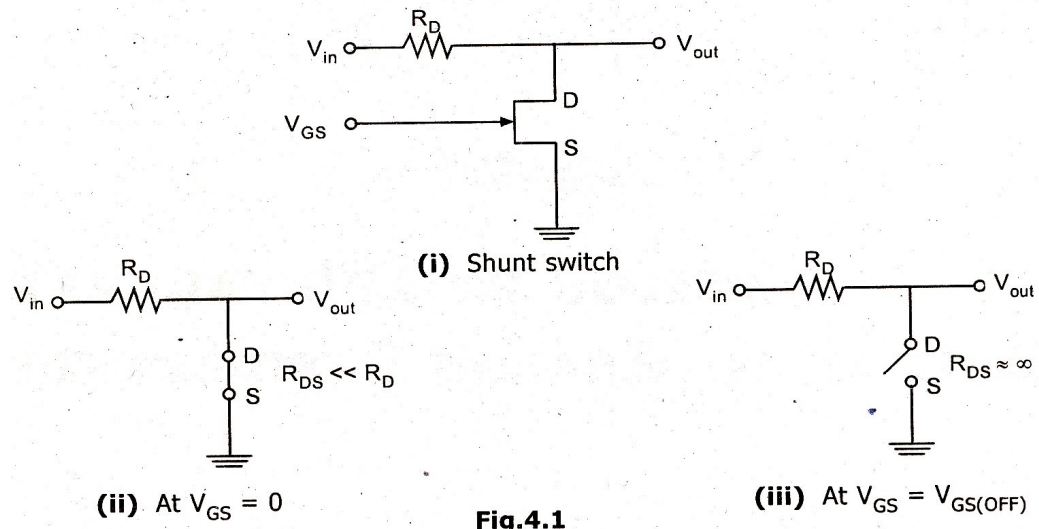
ANALOG TO DIGITAL CONVERSION

The natural state of audio and video signals is analog. When digital technology was not yet around, they are recorded or played back in analog devices like vinyl discs and cassette tapes. The storage capacity of these devices is limited and doing multiple runs of re-recording and editing produced poor signal quality. Developments in digital technology like the CD, DVD, Blu-ray, flash devices and other memory devices addressed these problems. For these devices to be used, the analog signals are first converted to digital signals using analog to digital conversion (ADC). For the recorded audio and video signals to be heard and viewed again, the reverse process of digital to analog conversion (DAC) is used. ADC and DAC are also used in interfacing digital circuits to analog systems. Typical applications are control and monitoring of temperature, water level, pressure and other real-world data.

An ADC inputs an analog signal such as voltage or current and outputs a digital signal in the form of a binary number. A DAC, on the other hand, inputs the binary number and outputs the corresponding analog voltage or current signal.
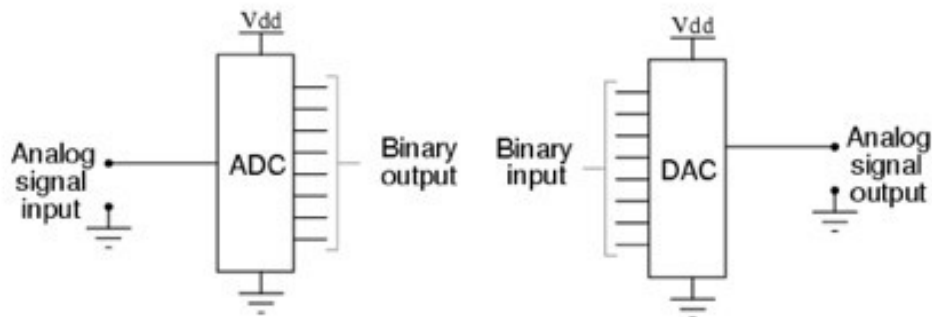
Sampling rate

The analog signal is continuous in time and it is necessary to convert this to a flow of digital values. It is therefore required to define the rate at which new digital values are sampled from the analog signal. The rate of new values is called the *sampling rate* or *sampling frequency* of the converter.

A continuously varying band limited signal can be sampled (that is, the signal values at intervals of time T, the sampling time, are measured and stored) and then the original signal can be *exactly* reproduced from the discrete-time values by an interpolation formula. The accuracy is limited by quantization error. However, this faithful reproduction is only possible if the sampling rate is higher than twice the highest frequency of the signal. This is essentially what is embodied in the Shannon-Nyquist sampling theorem.

Since a practical ADC cannot make an instantaneous conversion, the input value must necessarily be held constant during the time that the converter performs a conversion (called the*conversion time*). An input circuit called a sample and hold performs this task—in most cases by using a capacitor to store the analog voltage at the input, and using an electronic switch or gate to disconnect the capacitor from the input. Many ADC integrated circuits include the sample and hold subsystem internally.

Accuracy

An ADC has several sources of errors. Quantization error and (assuming the ADC is intended to be linear) non-linearity is intrinsic to any analog-to-digital conversion. There is also a so-called *aperture error* which is due to a clock jitter and is revealed when digitizing a time-variant signal (not a constant value).

These errors are measured in a unit called the *LSB*, which is an abbreviation for least significant bit. In the above example of an eight-bit ADC, an error of one LSB is 1/256 of the full signal range, or about 0.4%.

Quantization error

Quantization error is due to the finite resolution of the ADC, and is an unavoidable imperfection in all types of ADC. The magnitude of the quantization error at the sampling instant is between zero and half of one LSB.

In the general case, the original signal is much larger than one LSB. When this happens, the quantization error is not correlated with the signal, and has a uniform distribution. Its RMS value is the standard deviation of this distribution, given by $\frac{1}{\sqrt{12}}\text{LSB} \approx 0.289\,\text{LSB}$. In the eight-bit ADC example, this represents 0.113% of the full signal range.

At lower levels the quantizing error becomes dependent of the input signal, resulting in distortion. This distortion is created after the anti-aliasing filter, and if these distortions are above 1/2 the sample rate they will alias back into the audio band. In order to make the quantizing error independent of the input signal, noise with amplitude of 1 quantization step is added to the signal. This slightly reduces signal to noise ratio, but completely eliminates the distortion. It is known as dither.

Non-linearity

All ADCs suffer from non-linearity errors caused by their physical imperfections, resulting in their output to deviate from a linear function (or some other function, in the case of a deliberately non-linear ADC) of their input. These errors can sometimes be mitigated by calibration, or prevented by testing.

Important parameters for linearity are integral non-linearity (INL) and differential non-linearity (DNL). These non-linearities reduce the dynamic range of the signals that can be digitized by the ADC, also reducing the effective resolution of the ADC.

Types of ADC

Direct-conversion ADC/Flash type ADC:

This process is extremely fast with a sampling rate of up to 1 GHz. The resolution is however, limited because of the large number of comparators and reference voltages required. The input signal is fed simultaneously to all comparators. A priority encoder then generates a digital output that corresponds with the highest activated comparator.
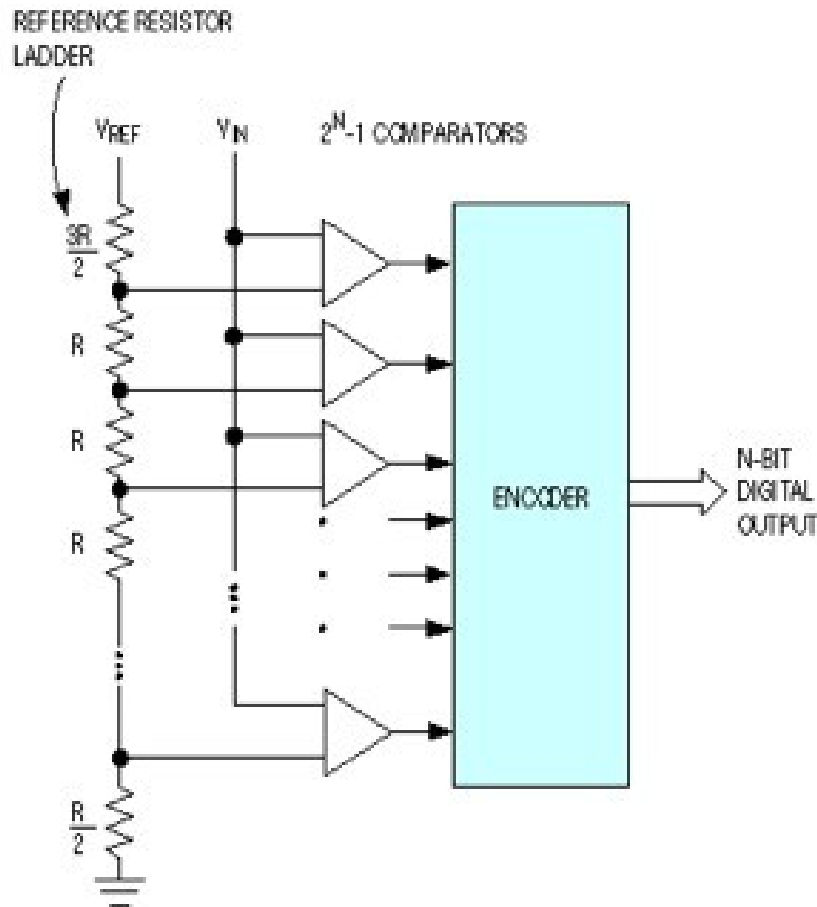
Successive-approximationADCs

Successive-approximation ADC is a conversion technique based on a successive-approximation register (SAR). This is also called bit-weighing conversion that employs a comparator to weigh the applied input voltage against the output of an N-bit digital-to-analog converter (DAC). The final

result is obtained as a sum of N weighting steps, in which each step is a single-bit conversion using the DAC output as a reference. SAR converters sample at rates up to 1Mbps, requires a low supply current, and the cheapest in terms of production cost.

A successive-approximation ADC uses a comparator to reject ranges of voltages, eventually settling on a final voltage range. Successive approximation works by constantly comparing the input voltage to the output of an internal digital to analog converter (DAC, fed by the current value of the approximation) until the best approximation is achieved. At each step in this process, a binary value of the approximation is stored in a successive approximation register (SAR). The SAR uses a reference voltage (which is the largest signal the ADC is to convert) for comparisons. For example if the input voltage is 60 V and the reference voltage is 100 V, in the 1st clock cycle, 60 V is compared to 50 V (the reference, divided by two. This is the voltage at the output of the internal DAC when the input is a '1' followed by zeros), and the voltage from the comparator is positive (or '1') (because 60 V is greater than 50 V). At this point the first binary digit (MSB) is set to a '1'. In the 2nd clock cycle the input voltage is compared to 75 V (being halfway between 100 and 50 V: This is the output of the internal DAC when its input is '11' followed by zeros) because 60 V is less than 75 V, the comparator output is now negative (or '0'). The second binary digit is therefore set to a '0'. In the 3rd clock cycle, the input voltage is compared with 62.5 V (halfway between 50 V and 75 V: This is the output of the internal DAC when its input is '101' followed by zeros). The output of the comparator is negative or '0' (because 60 V is less than 62.5 V) so the third binary digit is set to a 0. The fourth clock cycle similarly results in the fourth digit being a '1' (60 V is greater than 56.25 V, the DAC output for '1001' followed by zeros). The result of this would be in the binary form 1001. This is also called *bit-weighting conversion*, and is similar to a binary. The analogue value is rounded to the nearest binary value below, meaning this converter type is mid-rise (see above). Because the approximations are successive (not simultaneous), the conversion takes one clock-cycle for each bit of resolution desired. The clock frequency must be equal to the sampling frequency multiplied by the number of bits of resolution desired. For example, to sample audio at 44.1 kHz with 32 bit resolution, a clock frequency of over 1.4 MHz would be required. ADCs of this type have good resolutions and quite wide ranges. They are more complex than some other designs.
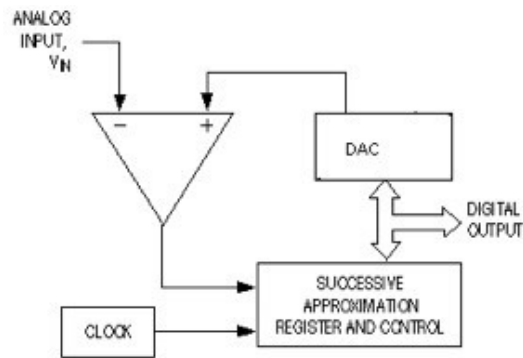
IntegratingADCs

In an integrating ADC, a current, proportional to the input voltage, charges a capacitor for a fixed time interval T charge. At the end of this interval, the device resets its counter and applies an opposite-polarity negative reference voltage to the integrator input. Because of this, the capacitor is discharged by a constant current until the integrator output voltage zero again. The T discharge interval is proportional to the input voltage level and the resultant final count provides the digital output, corresponding to the input signal. This type of ADCs is extremely slow devices with low input bandwidths. Their advantage, however, is their ability to reject high-frequency noise and AC line noise such as 50Hz or 60Hz. This makes them useful in noisy industrial environments and typical application is in multi-meters.

An integrating ADC (also dual-slope or multi-slope ADC) applies the unknown input voltage to the input of an integrator and allows the voltage to ramp for a fixed time period (the run-up period). Then a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero (the run-down period). The input voltage is computed as a function of the reference voltage, the constant run-up time period, and the measured run-down time period. The run-down time measurement is usually made in units of the converter's clock, so longer integration times allow for higher resolutions. Likewise, the speed of the converter can be improved by sacrificing resolution. Converters of this type (or variations on the concept) are used in most digital voltmeters for their linearity and flexibility.
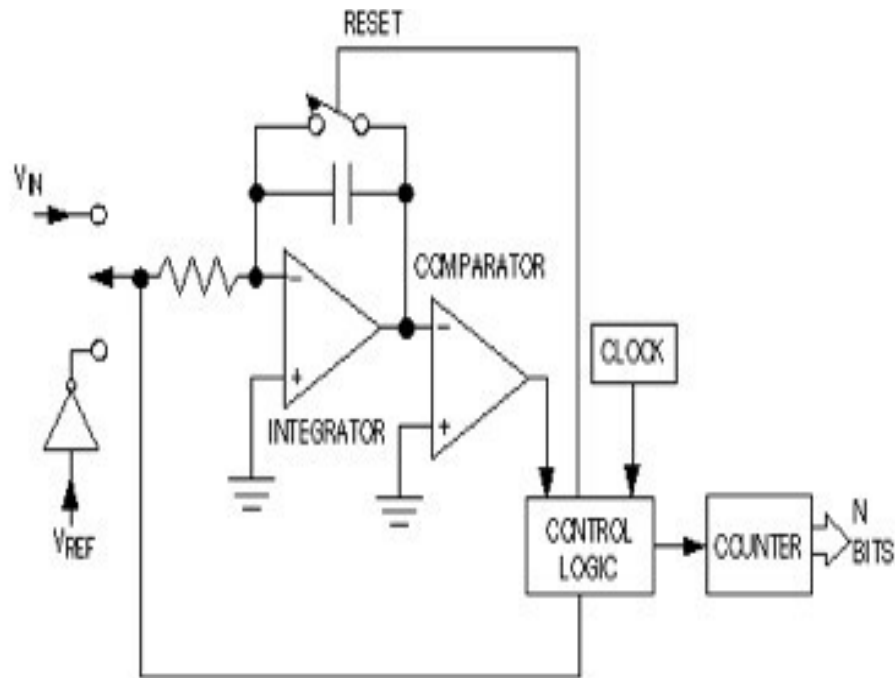
Sigma-delta ADCs/ Over sampling Converters:

It consist of 2 main parts - modulator and digital filter. The modulator includes an integrator and a comparator with a feedback loop that contains a 1-bit DAC. The modulator oversamples the input signal, converting it to a serial bit stream with a frequency much higher than the required sampling rate. This is then transform by the output filter to a sequence of parallel digital words at the sampling rate. The characteristics of sigma-delta converters are high resolution, high accuracy, low noise and low cost. Typical applications are for speech and audio.

A **Sigma-Delta ADC** (also known as a Delta-Sigma ADC) oversamples the desired signal by a large factor and filters the desired signal band. Generally a smaller number of bits than required are converted using a Flash ADC after the Filter. The resulting signal, along with the error generated by the discrete levels of the Flash, is fed back and subtracted from the input to the filter. This negative feedback has the effect of noise shaping the error due to the Flash so that it does not appear in the desired signal frequencies. A digital filter (decimation filter) follows the ADC which reduces the sampling rate, filters off unwanted noise signal and increases the resolution of the output. (sigma-delta modulation, also called delta-sigma modulation)

A/D Using Voltage to time conversion:

The Block diagram shows the basic voltage to time conversion type of A to D converter. Here the cycles of variable frequency source are counted for a fixed period. It is possible to make an A/D converter by counting the cycles of a fixed-frequency source for a variable period. For this, the analog voltage required to be converted to a proportional time period.

As shown in the diagram, A negative reference voltage $-V_R$ is applied to an integrator, whose output is connected to the inverting input of the comparator. The output of the comparator is at 1 as long as the output of the integrator Vo is less than Va. At $t = T$, Vc goes low and switch S remains open. When V_{EN} goes high, the switch S is closed, thereby discharging the capacitor. Also the NAND gate is disabled. The waveforms are shown here.
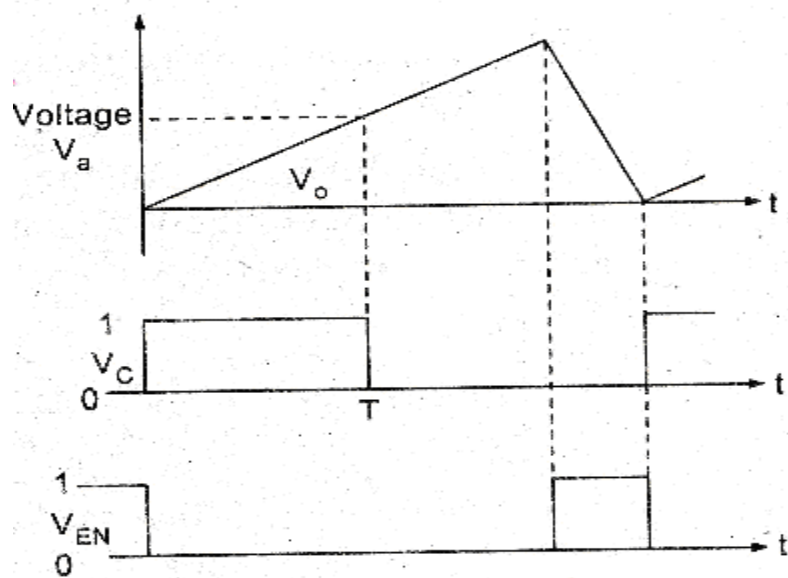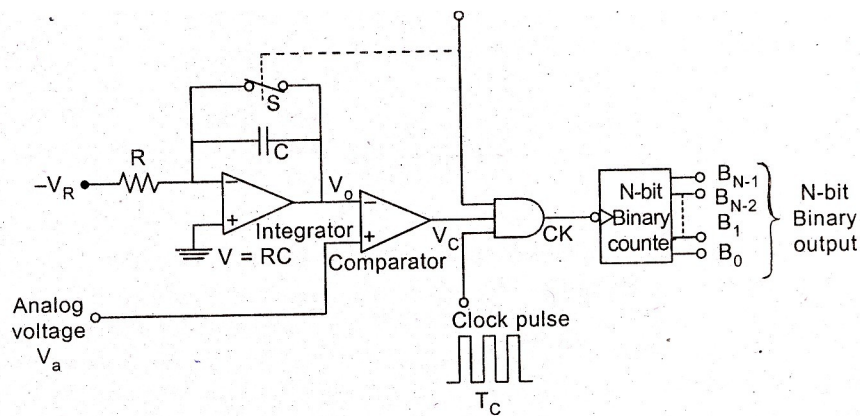
UNIT V – WAVEFORM GENERATORS AND SPECIAL FUNCTION ICs

BASICS OF OSCILLATORS:

Criteria for oscillation:

The canonical form of a feedback system is shown in Figure 1, and Equation 1 describes the performance of any feedback system (an amplifier with passive feedback Components constitutes a feedback system).
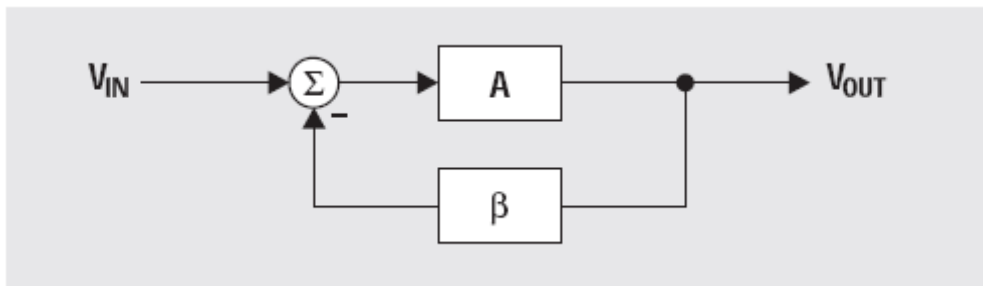
Figure 1: Canonical form of feedback circuit

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \qquad\qquad (1)$$

Oscillation results from an unstable state; i.e., the feedback system can't find a stable state because its transfer function can't be satisfied. Equation 1 becomes unstable when $(1+A\beta) = 0$ because A/0 is an undefined state. Thus, the key to designing an oscillator is to insure that $A\beta = -1$ (called the Barkhausen criterion), or using complex math the equivalent expression is $A\beta = 1 \angle -180°$. The $-180°$ phase shift criterion applies to negative feedback systems, and $0°$ phase shift applies to positive feedback systems.

The output voltage of a feedback system heads for infinite voltage when $A\beta = -1$. When the output voltage approaches either power rail, the active devices in the amplifiers change gain, causing the value of A to change so the value of $A\beta \neq 1$; thus, the charge to infinite voltage slows down and eventually halts. At this point one of three things can occur. First, nonlinearity in saturation or cutoff can cause the system to become stable and lock up. Second, the initial charge can cause the system to saturate (or cut off) and stay that way for a long time before it becomes linear and heads for the opposite power rail. Third, the system stays linear and reverses direction, heading for the opposite power rail. Alternative two produces highly distorted oscillations (usually quasi square waves),
and the resulting oscillators are called relaxation oscillators. Alternative three produces sine wave oscillators.

All oscillator circuits were built with op amps, 5% resistors, and 20% capacitors; hence, component tolerances cause differences between ideal and measured values.

Phase Shift in Oscillators:

The $180°$ phase shift in the equation $A\beta = 1 \angle -180°$ is introduced by active and passive components. Like any well-designed feedback circuit, oscillators are made dependent on passive component phase shift because it is accurate and almost drift-free. The phase shift contributed by active components is minimized because it varies with temperature, has a wide initial tolerance, and is device dependent. Amplifiers are selected such that they contribute little or no phase shift at the oscillation frequency. A single pole RL or RC circuit contributes up to $90°$ phase shift per pole, and because $180°$ is required for oscillation, at least two poles must be used in oscillator design.

An LC circuit has two poles; thus, it contributes up to 180° phase shift per pole pair, but LC and LR oscillators are not considered here because low frequency inductors are expensive, heavy, bulky, and non-ideal. LC oscillators are designed in high-frequency applications, beyond the frequency range of voltage feedback op amps, where the inductor size, weight, and cost are less significant. Multiple RC sections are used in low-frequency oscillator design in lieu of inductors.

Phase shift determines the oscillation frequency because the circuit oscillates at the frequency that accumulates −180° phase shift. The rate of change of phase with frequency, $d\phi/dt$, determines frequency stability. When buffered RC sections (an op amp buffer provides high input and low-output impedance) are cascaded, the phase shift multiplies by the number of sections, n (see Figure 2).
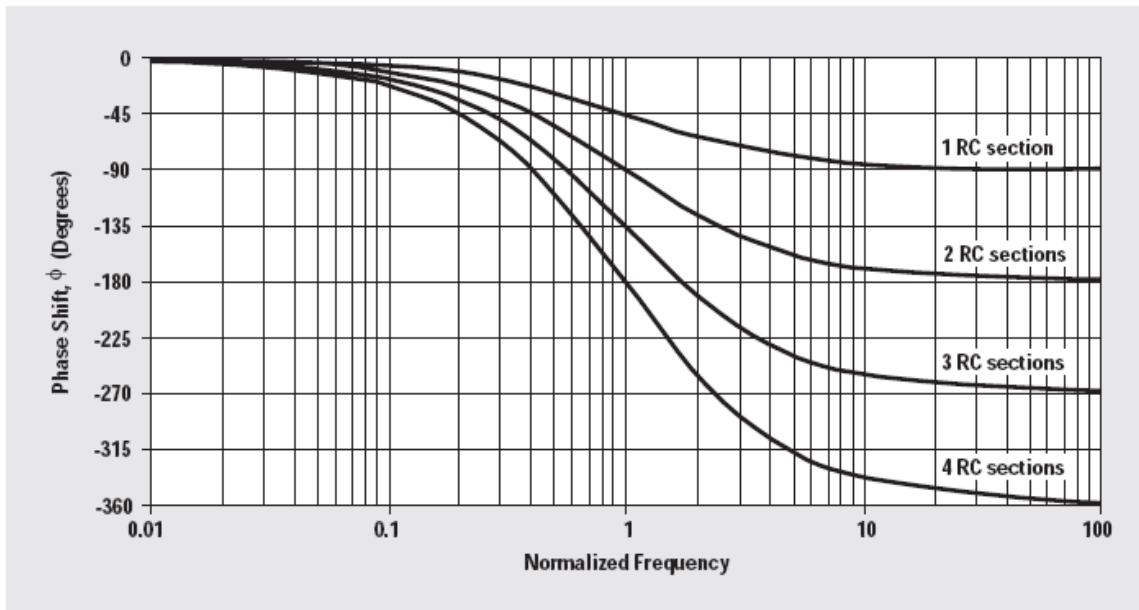
Figure 2: Phase plot of RC sections

Although two cascaded RC sections provide 180° phase shift, $d\phi/dt$ at the oscillator frequency is low, thus oscillators made with two cascaded RC sections have poor frequency stability. Three equal cascaded RC filter sections have a higher $d\phi/dt$, and the resulting oscillator has improved frequency stability. Adding a fourth RC section produces an oscillator with an excellent $d\phi/dt$, thus this is the most stable oscillator configuration. Four sections are the maximum number used

because op amps come in quad packages, and the four-section oscillator yields four sine waves that are 45° phase shifted relative to each other, so this oscillator can be used to obtain sine/cosine or quadrature sine waves.

Crystal or ceramic resonators make the most stable oscillators because resonators have an extremely high $d\phi/dt$ resulting from their non-linear properties. Resonators are used for high-frequency oscillators, but low-frequency oscillators do not use resonators because of size, weight, and cost restrictions. Op amps are not used with crystal or ceramic resonator oscillators because op amps have low bandwidth. Experience shows that it is more cost-effective to build a high-frequency crystal oscillator and count down the output to obtain a low frequency than it is to use a low-frequency resonator.

Gain in Oscillators:

The oscillator gain must equal one ($A\beta = 1 \angle -180°$) at the oscillation frequency. The circuit becomes stable when the gain exceeds one and oscillations cease. When the gain exceeds one with a phase shift of $-180°$, the active device non-linearity reduces the gain to one. The non-linearity happens when the amplifier swings close to either power rail because cutoff or saturation reduces the active device (transistor) gain. The paradox is that worst-case design practice requires nominal gains exceeding one for manufacturability, but excess gain causes more distortion of the output sine wave.

When the gain is too low, oscillations cease under worst-case conditions, and when the gain is too high, the output wave form looks more like a square wave than a sine wave. Distortion is a direct result of excess gain overdriving the amplifier; thus, gain must be carefully controlled in low distortion oscillators. Phase-shift oscillators have distortion, but they achieve low-distortion output voltages because cascaded RC sections act as distortion filters. Also, buffered phase-shift oscillators have low distortion because the gain is controlled and distributed among the buffers. Some circuit configurations (Wien-bridge) or low distortion specifications require an auxiliary circuit to adjust the gain. Auxiliary circuits range from inserting a non-linear component in the feedback loop, to automatic gain control (AGC) loops, to limiting by external components.

SINE WAVE GENERATORS (OSCILLATORS)

The sine wave is certainly one of the most fundamental waveforms. A variety of circuits and techniques have been developed for the generation of sine waves. The conventional sine wave oscillator circuits use phase shifting techniques that usually employ

- Two RC tuning networks, and
- Complex amplitude limiting circuitry

RC PHASE SHIFT OSCILLATOR
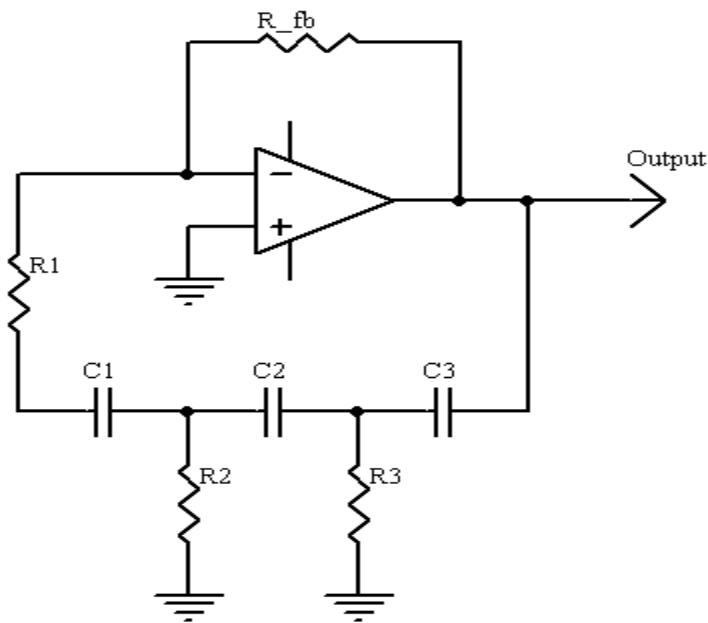
RC phase shift oscillator using op-amp in inverting amplifier introduces the phase shift of 180^0 between input and output. The feedback network consists of 3 RC sections each producing 60^0 phase shift. Such a RC phase shift oscillator using op-amp is shown in the figure.

The output of amplifier is given to feedback network. The output of feedback network drives the amplifier. The total phase shift around a loop is 180^0 of amplifier and 180^0 due to 3 RC section, thus 360^0. This satisfies the required condition for positive feedback and circuit works as an oscillator.

Without the simplification of all the resistors and capacitors having the same value, the calculations become more complex:

$$f_{\text{oscillation}} = \frac{1}{2\pi\sqrt{R_2 R_3 (C_1 C_2 + C_1 C_3 + C_2 C_3) + R_1 R_3 (C_1 C_2 + C_1 C_3) + R_1 R_2 C_1 C_2}}$$

Oscillation criterion:

$$R_{\text{feedback}} = 2(R_1 + R_2 + R_3) + \frac{2R_1 R_3}{R_2} + \frac{C_2 R_2 + C_2 R_3 + C_3 R_3}{C_1}$$

$$+ \frac{2C_1 R_1 + C_1 R_2 + C_3 R_3}{C_2} + \frac{2C_1 R_1 + 2C_2 R_1 + C_1 R_2 + C_2 R_2 + C_2 R_3}{C_3}$$

$$+ \frac{C_1 R_1^2 + C_3 R_1 R_3}{C_2 R_2} + \frac{C_2 R_1 R_3 + C_1 R_1^2}{C_3 R_2} + \frac{C_1 R_1^2 + C_1 R_1 R_2 + C_2 R_1 R_2}{C_3 R_3}$$

Phase Shift Oscillator Types

i) RC Phase shift oscillator:

A phase-shift oscillator can be built with one op amp as shown in Figure 5. The normal assumption is that the phase-shift sections are independent of each other.
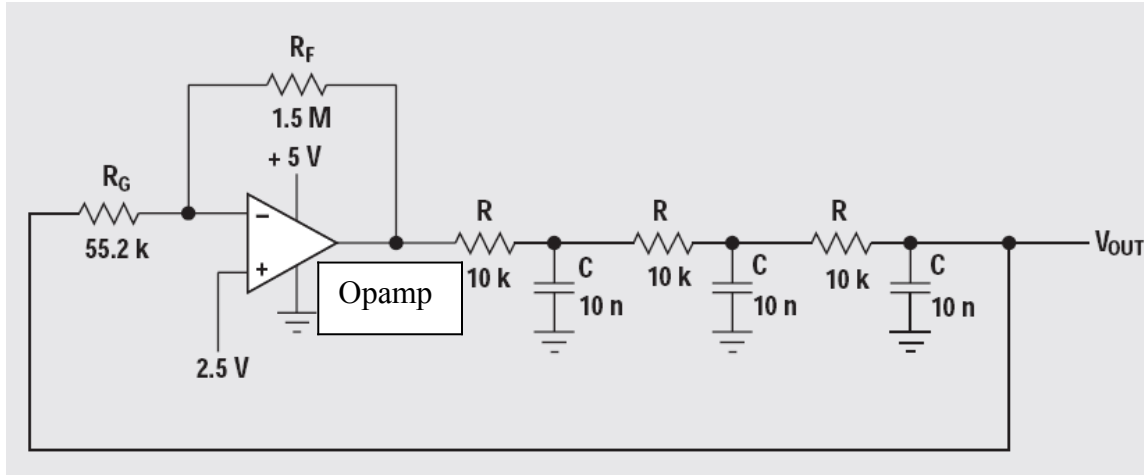
Figure 5: RC Phase Shift Oscillator using one op-amp

The Equation 3 is written:

$$A\beta = A\left(\frac{1}{RCs+1}\right)^3 \qquad (3)$$

The loop phase shift is $-180°$ when the phase shift of each section is $-60°$, and this occurs when ω = $2\pi f$ = $1.732/RC$ because the tangent $60° = 1.73$. The magnitude of β at this point is $(1/2)^3$, so the gain, A, must be equal to 8 for the system gain to be equal to 1. The oscillation frequency with the component values shown in Figure 5 is 3.76 kHz rather than the calculated oscillation frequency of 2.76 kHz. Also, the gain required to start oscillation is 26 rather than the calculated gain of 8. These discrepancies are partially due to component variations, but the biggest contributing factor is the incorrect assumption that the RC sections do not load each other. This circuit configuration was very popular when active components were large and expensive, but now op amps are inexpensive and small and come four in a package, so the single op amp phase-shift oscillator is losing popularity.

ii) Quadrature Phase shift oscillator:

The quadrature oscillator is another type of phase-shift oscillator, but the three RC sections are configured so that each section contributes 90° of phase shift. The outputs are labeled sine and cosine (quadrature) because there is a 90° phase shift between op amp outputs (see Figure 6).
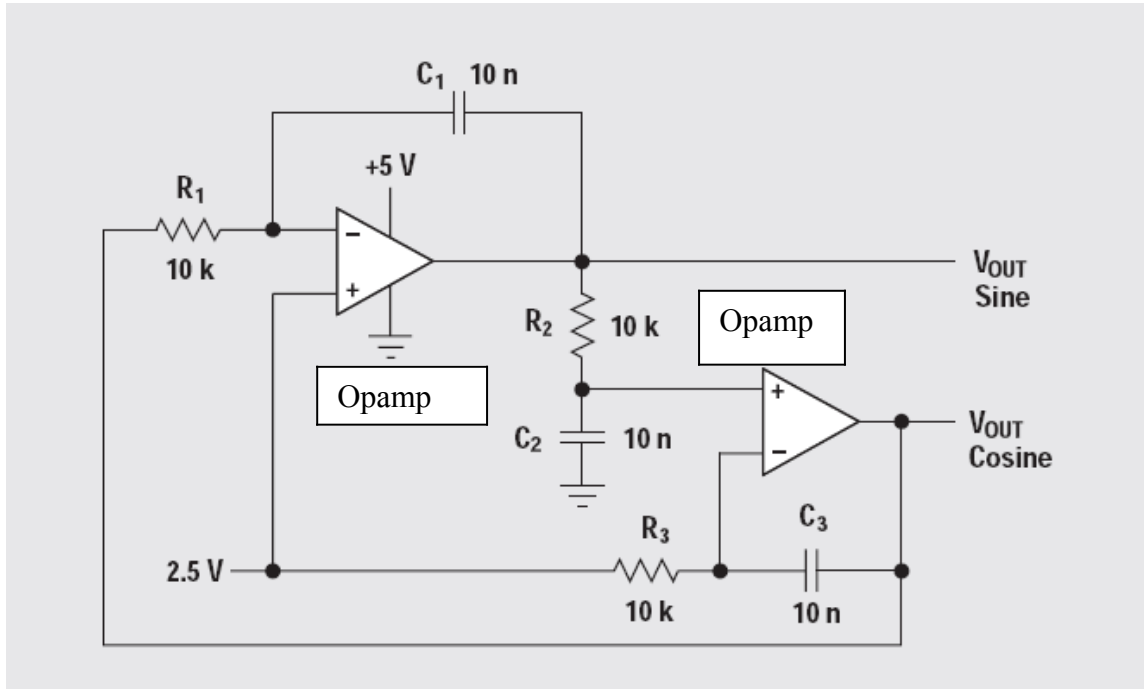
Figure 6: Quadrature Phase Shift Oscillator

The loop gain is calculated in Equation 4.

$$A\beta = \left(\frac{1}{R_1 C_1 s}\right)\left(\frac{R_3 C_3 s + 1}{R_3 C_3 s (R_2 C_2 s + 1)}\right) \quad \text{(4)}$$

When $R_1 C_1 = R_2 C_2 = R_3 C_3$, Equation 4 reduces to Equation 5

$$A\beta = \frac{1}{(RCs)^2} \quad \text{(5)}$$

When $\omega = 1/RC$, Equation 5 reduces to $1 \angle -180°$, so oscillation occurs at $\omega = 2\pi f = 1/RC$. The test circuit oscillated at 1.65 kHz rather than the calculated 1.59 kHz, and the discrepancy is attributed to component variations.

Op amp oscillators are restricted to the lower end of the frequency spectrum because op amps do not have the required bandwidth to achieve low phase shift at high frequencies. The new current feedback op amps are very hard to use in oscillator circuits because they are sensitive to feedback capacitance. Voltage feedback op amps are limited to a few hundred kHz because they accumulate too much phase shift.

Wien Bridge Oscillator:

Figure 3 gives the Wien-bridge circuit configuration. The loop is broken at the positive input, and the return signal is calculated in Equation 2 below.
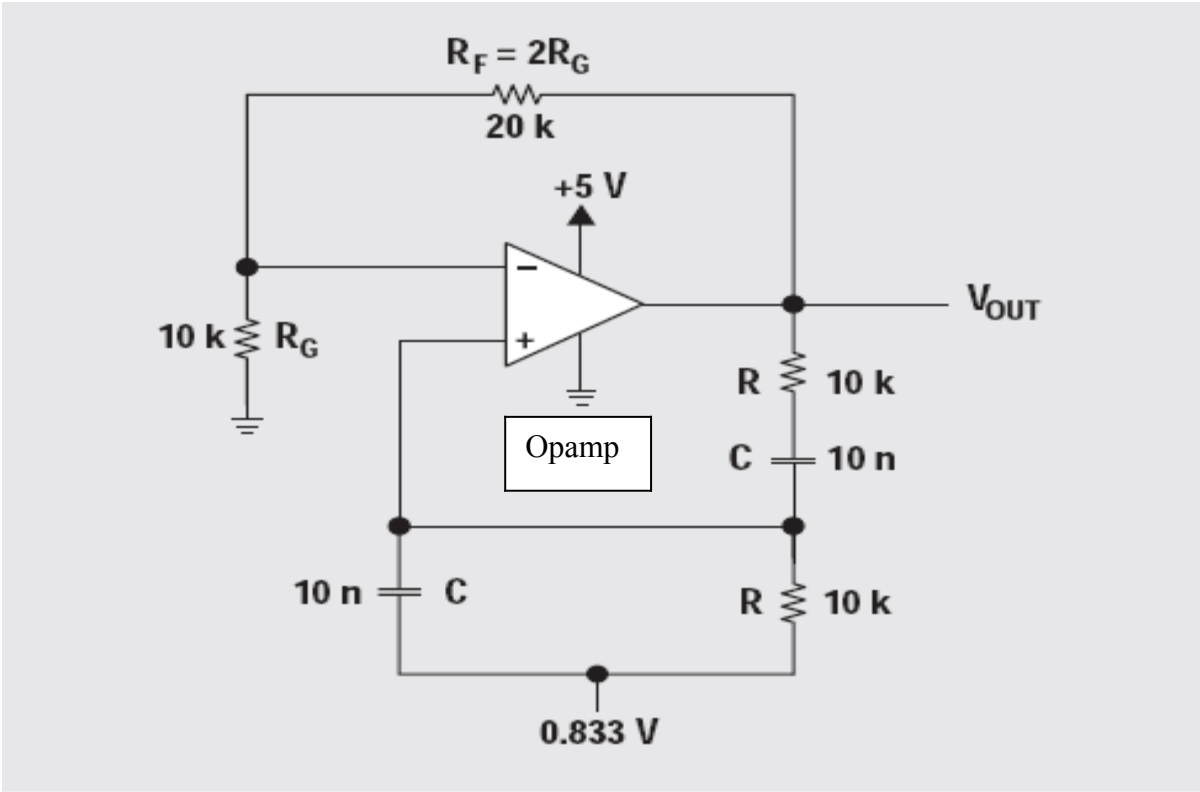
Figure 3: Wien Bridge Circuit Schematic

$$\frac{V_{RETURN}}{V_{OUT}} = \frac{\dfrac{R}{RCs+1}}{\dfrac{R}{RCs+1}+R+\dfrac{1}{Cs}} = \frac{1}{3+RCs+\dfrac{1}{RCs}} = \frac{1}{3+j\left(RC\omega-\dfrac{1}{RC\omega}\right)}, \qquad (2)$$

where s = jω and j = √−1.

When ω = 2πf = 1/RC, the feedback is in phase (this is positive feedback), and the gain is 1/3, so oscillation requires an amplifier with a gain of 3. When R_F = $2R_G$, the amplifier gain is 3 and oscillation occurs at f = 1/2πRC. The circuit oscillated at 1.65 kHz rather than 1.59 kHz with the component values shown in Figure 3, but the distortion is noticeable.
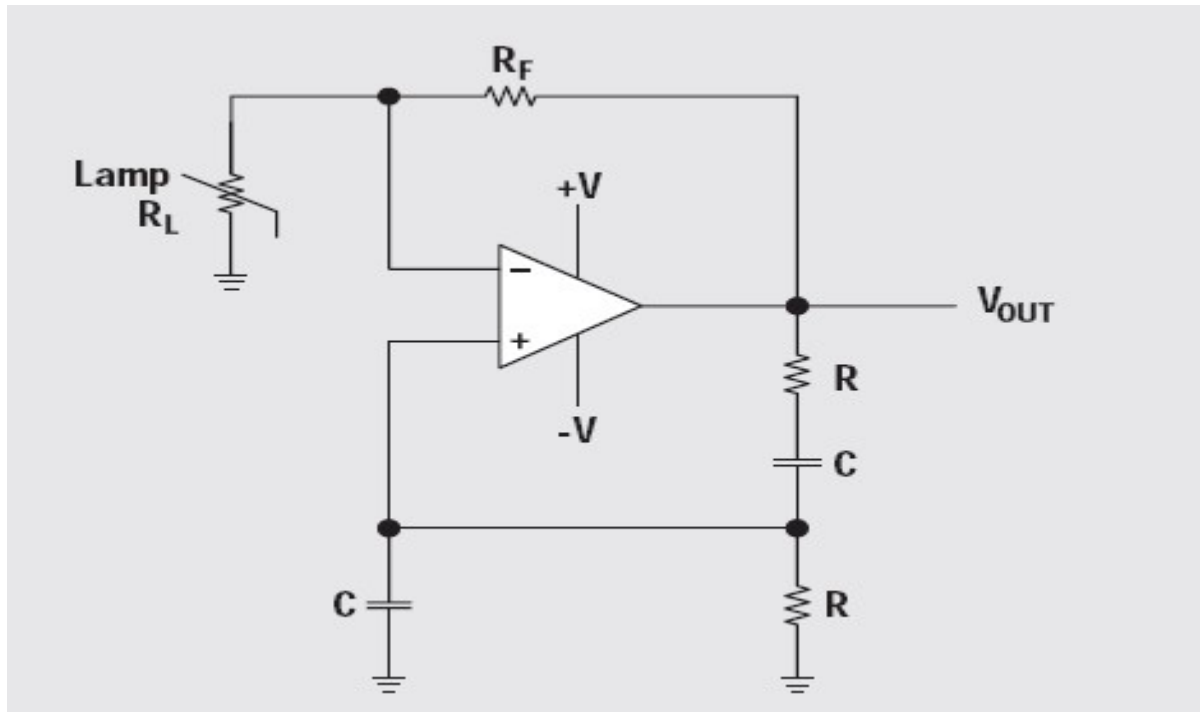
Figure 4: Wien Bridge Circuit Schematic with non-linear feedback

Figure 4 shows a Wien-bridge circuit with non-linear feedback. The lamp resistance, R_L, is nominally selected as half the feedback resistance, R_F, at the lamp current established by R_F and R_L. The non-linear relationship between the lamp current and resistance keeps output voltage changes small.

Some circuits use diode limiting in place of a non-linear feedback component. The diodes reduce the distortion by providing a soft limit for the output voltage. AGC must be used when neither of these techniques yields low distortion.

Generally in an oscillator, amplifier stage introduces 180^0 phase shift, to obtain a phase shift of 360^0 (2π radians) around a loop. This is required condition for any oscillator. But Wien bridge oscillator uses a non-inverting amplifier and hence does not provide any phase shift during amplifier stage. As total phase shift required is 0^0 or $2n\pi$ radians, in Wien bridge type no phase shift is necessary through feedback. Thus the total phase shift around a loop is 0^0. Let us study the basic version of the Wien bridge oscillator and its analysis.

A basic Wien bridge used in this oscillator and an amplifier stage is shown in figure.
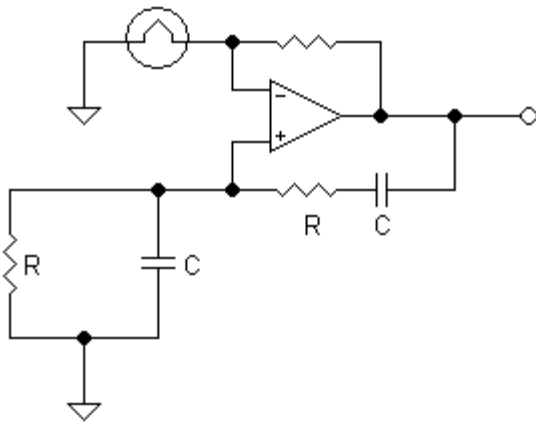
If a voltage source is applied directly to the input of an **ideal** amplifier with feedback, the input current will be:

$$i_{in} = \frac{v_{in} - v_{out}}{Z_f}$$

Where v_{in} is the input voltage, v_{out} is the output voltage, and Z_f is the feedback impedance. If the voltage gain of the amplifier is defined as:

$$A_v = \frac{v_{out}}{v_{in}}$$

And the input admittance is defined as:

$$Y_i = \frac{i_{in}}{v_{in}}$$

Input admittance can be rewritten as:

$$Y_i = \frac{1 - A_v}{Z_f}$$

For the Wien bridge, Z_f is given by:

$$Z_f = R + \frac{1}{j\omega C}$$

$$Y_i = \frac{(1 - A_v)(\omega^2 C^2 R + j\omega C)}{1 + (\omega C R)^2}$$

If A_v is greater than 1, the input admittance is a negative resistance in parallel with an inductance. The inductance is:

$$L_{in} = \frac{\omega^2 C^2 R^2 + 1}{\omega^2 C (A_v - 1)}$$

If a capacitor with the same value of C is placed in parallel with the input, the circuit has a natural resonance at:

$$\omega = \frac{1}{\sqrt{L_{in} C}}$$

Substituting and solving for inductance yields:

$$L_{in} = \frac{R^2 C}{A_v - 2}$$

If A_v is chosen to be 3:

$L_{in} = R^2 C$

Substituting this value yields:

$$\omega = \frac{1}{RC}$$

Or:

$$f = \frac{1}{2\pi RC}$$

Similarly, the input resistance at the frequency above is:

$$R_{in} = \frac{-2R}{A_v - 1}$$

For $A_v = 3$:

$R_{in} = -R$

If a resistor is placed in parallel with the amplifier input, it will cancel some of the negative resistance. If the net resistance is negative, amplitude will grow until clipping occurs. Similarly, if the net resistance is positive, oscillation amplitude will decay. If a resistance is added in parallel with exactly the value of R, the net resistance will be infinite and the circuit can sustain stable oscillation at any amplitude allowed by the amplifier.

Notice that increasing the gain makes the net resistance more negative, which increases amplitude. If gain is reduced to exactly 3 when a suitable amplitude is reached, stable, low distortion oscillations will result. Amplitude stabilization circuits typically increase gain until a suitable output amplitude is reached. As long as R, C, and the amplifier are linear, distortion will be minimal.

MULTIVIBRATORS

Astable Multivibrator

The two states of circuit are only stable for a limited time and the circuit switches between them with the output alternating between positive and negative saturation values. Analysis of this circuit starts with the assumption that at time $t=0$ the output has just switched to state 1, and the transition would have occurred when
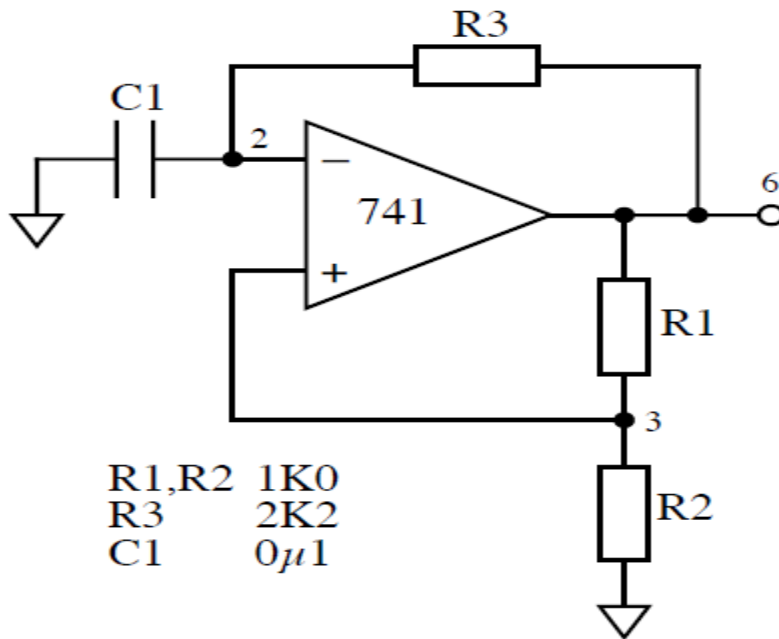
An op-amp Astable multivibrator is also called as free running oscillator. The basic principle of generation of square wave is to force an op-amp to operate in the saturation region ($\pm$Vsat). A fraction $\beta = \dfrac{R2}{R1 + R2}$ of the output is feedback to the positive input terminal of op-amp. The charge in the capacitor increases & decreases upto a threshold value called $\pm\beta$Vsat. The charge in the capacitor triggers the op-amp to stay either at +Vsat or −Vsat. Asymmetrical square wave can also be generated with the help of zener diodes. Astable multivibrator do not require a external trigger pulse for its operation & output toggles from one state to another and does not contain a stable state. Astable multivibrator are mainly used in timing applications & waveforms generators.

Design

An Square Wave Generator at $f_0 = 1$ KHz.

1. The expression of f_o is obtained from the charging period t1 & t2 of capacitor as

$$f_o = \frac{1}{2RC \ln[1 + 2R_1 / R_2]}$$

2. To simplify the above expression, the value of R1 & R2 should be taken as R2 = 1.16R, such that f_o simplifies to $f_o = \frac{1}{2RC}$

3. Assume the value of R1 and find R2. R2 = 1.16KΩ (10K)

4. Assume the value of C & Determine R from $f_o = \frac{1}{2RC}$

5. Calculate the threshold point from

$$|V_T| \text{ or } |\beta V_{SAT}| = \frac{R1}{R1 + R2} |\beta V_{SAT}| \quad \text{where } \beta \text{ is the feedback ratio.}$$

Monostable Multivibrator using Op-amp:

circuit diagram:
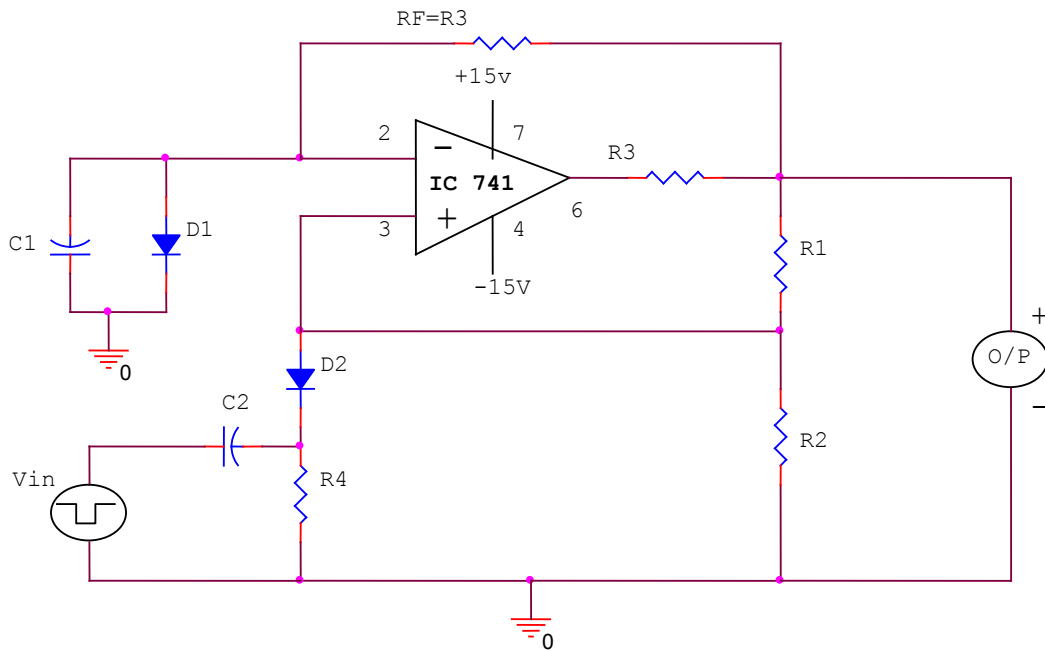
Output Waveform:
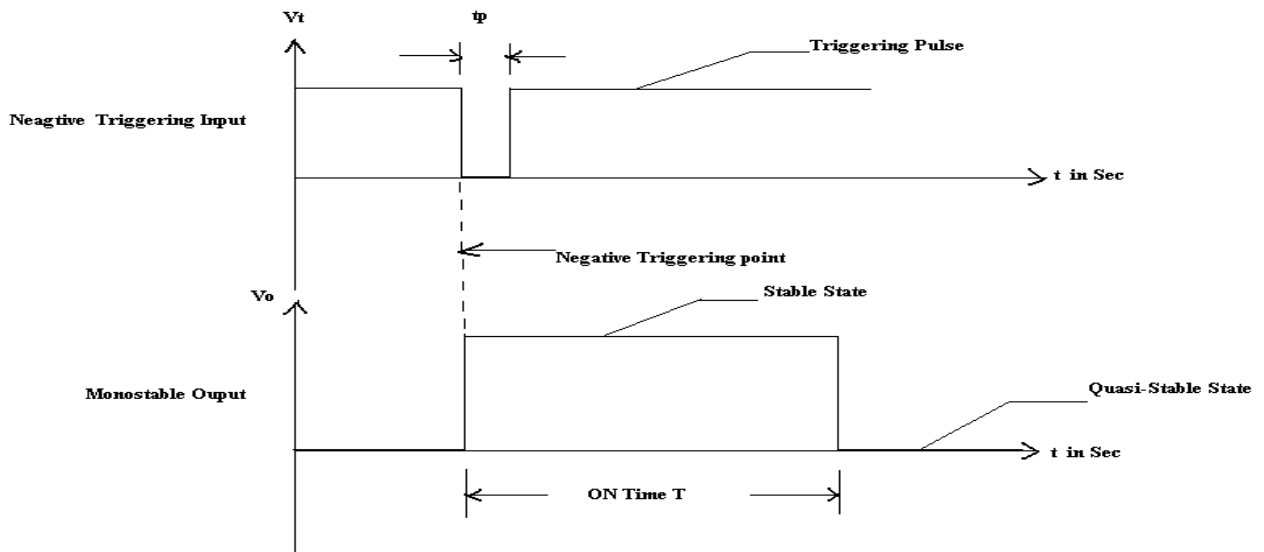
A multivibrator which has only one stable and the other is quasi stable state is called as Monostable multivibrator or one-short multivibrator. This circuit is useful for generating signal output pulse of adjustable time duration in response to a triggering signal. The width of the output pulse depends only on the external components connected to the op-amp. Usually a negative trigger pulse is given to make the output switch to other state. But, it then return to its stable state after a time interval determining by circuit components. The pulse width T can be given as T = 0.69RC. for Monostable operation the triggering pulse width Tp should be less then T, the pulse width of Monostable multivibrator. This circuit is also called as time delay circuit or gating circuit.

Design:

1. Calculating β from expression

$$\beta = \frac{R1}{R1 + R2}$$

2. The value of R & C from the pulse width time expression.

$$T = RC \ln \frac{(1 + V_D / V_{sat})}{1 - \beta}$$

$$T = RC \ln \frac{(1 + V_D / V_{sat})}{0.5}$$

$$T \equiv 0.69RC.$$

3. Triggering pulse width T_p must be much smaller then T. $T_p < T$.

TRIANGULAR WAVE GENERATOR

Circuit:
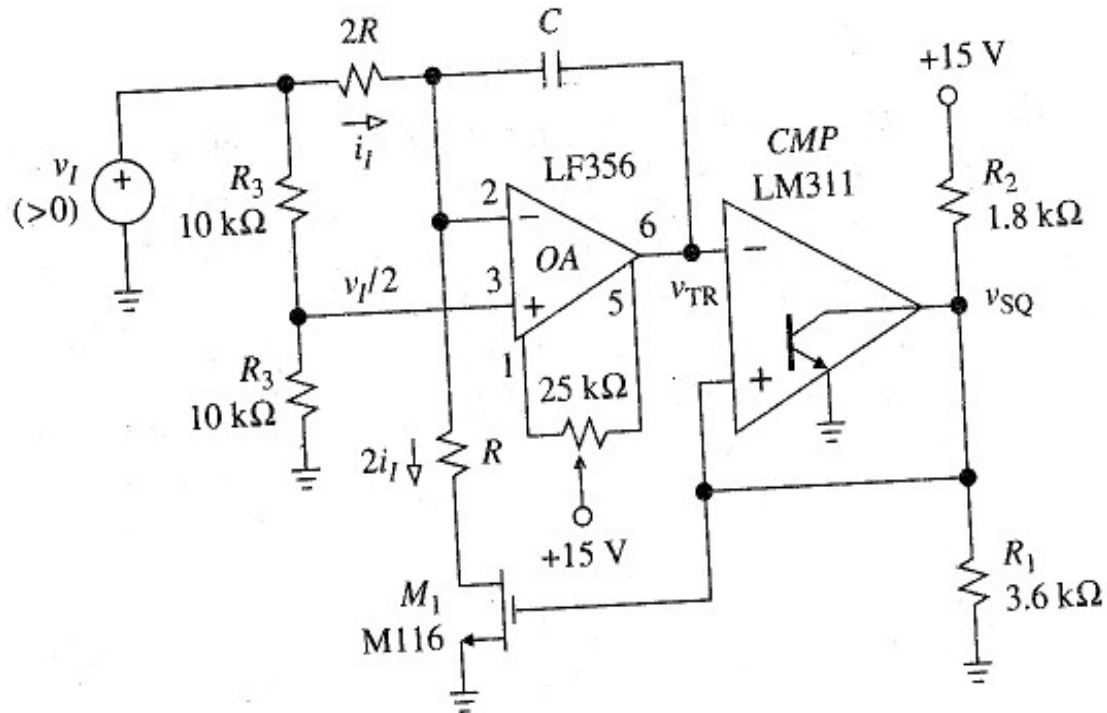
This signal generator gives you two waveforms for the price of one: a triangle-wave and a square-wave. The central component of this circuit is the integrator capacitor CI. Basically we are interested in performing two functions on CI: *charge it, discharge it - repeat indefinitely*. The output waveforms are shown here and it is apparent that a square wave generator followed by an integrator acts as a triangular wave generator.
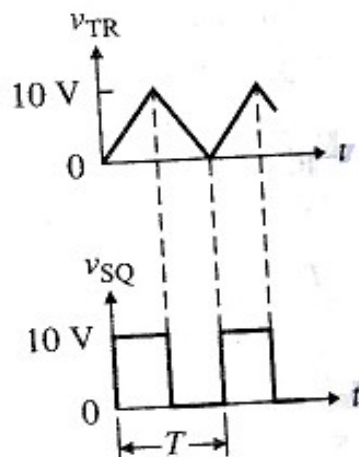
Suppose our design calls for a +/-10 V triangle wave, cruising along at 10 kHz. This means that Vth+ = +10 V and Vth- = -10 V. Given VP = +5 V, VN = -5 V, let's choose R2 = 10 kΩ and then calculate R1 = 20 kΩ from the equation above. If the value of Capacitor is1 nf, then what value of RI is needed for 10 kHz (T = 100 μs) can be calculated, because Vo needs to swing ΔVo = 10 - (-10) = 20 V in an interval ΔT = 50 μs, we solve the above equation in the Linear Ramps section for RI.

Changing the voltage thresholds also changes the time required to reach the thresholds. Also, make sure Vth+ and Vth- are not outside the +/-15V limits of the op amp model. And don't forget the option of changing the reverse voltage of the zener diode via the BV parameter. Just remember the charging currents and thresholds will change too.
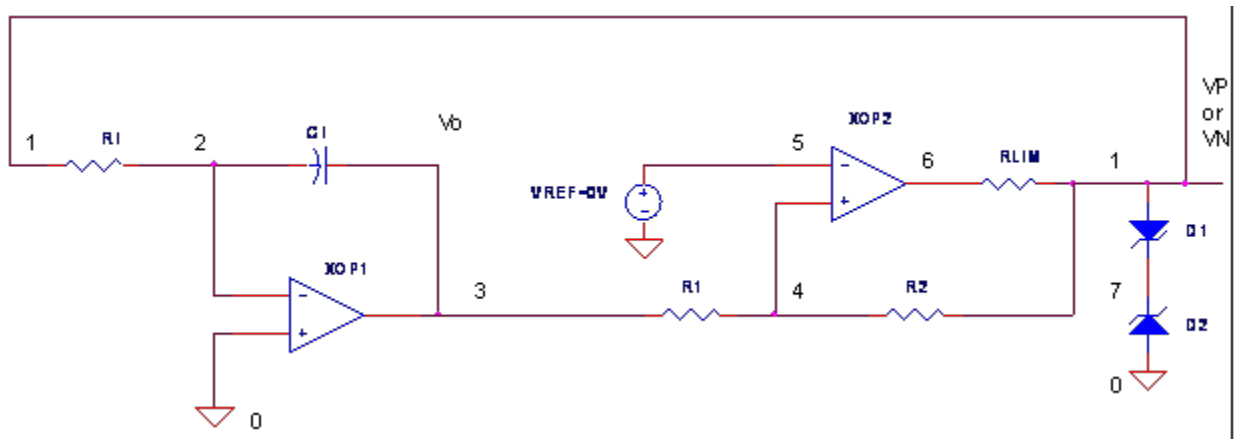
You may have noticed that the triangle peaks and period may not accurately meet our +/-10V swing at 100 us. The main reason is that our current source and thresholds are derived from zener diodes - not exactly the most accurate reference. Some designs use improved means for deriving and switching the current sources that charge CI.

LINEAR RAMP GENERATOR

A triangle wave implies that the circuit generates a linear voltage ramp. One way to achieve this goal is by charging discharging CI with a constant current. The Op Amp Integrator provides a handy way to accomplish this.
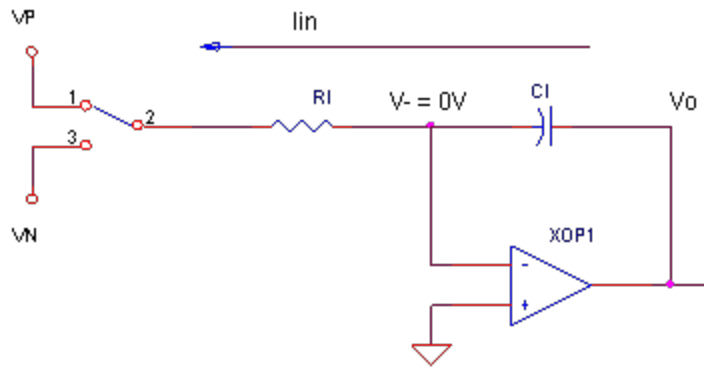
Ramp Up

Connect RI to VN and With V- held at the virtual ground (0V), a constant current flows from V- to VN.

Iin = VN / RI.

CI integrates *Iin* creating a positive linear ramp at Vo. The ramp is linear because Vo changes proportionally to the time elapsed ΔT.

ΔVo = - VN / (CI · RI) · ΔT

Ramp Down   Connect RI to VP and a constant current flows from VP to V-, *Iin = - VP / RI*. Now Vo ramps down linearly

ΔVo = - VP / (CI · RI) · ΔT

RampUp:*ΔVo/ΔT= -VN/(CIRI)*
Ramp Down:*ΔVo /ΔT = - VP / (CI · RI)*

These equations show you the parameters available to control the ramp up / down speeds. There is a possibility of creating asymmetrical voltage swings by including a reference voltage VREF to the comparator's negative input. (Actually, its been there all along, just set to 0V.) VREF let's you place the thresholds more freely - they can now both be positive or negative. Basically, VREF can shift the thresholds up or down as shown in the equation.

$$Vth+ = VREF \cdot (R1+R2)/R2 - VN \cdot R1/R2$$
$$Vth- = VREF \cdot (R1+R2)/R2 - VP \cdot R1 / R2$$

Pick new thresholds by including VREF. For example, set R1 = R2 = 10k and VREF = 2.5 V. Run a new simulation and check your new triangle boundaries. Make sure your Vth+ and Vth- are not outside the +/-15V limits of the op amp model.

It is not confined to equal ramp up and down rates. New voltage source VREF2 and connect it to the integrator's positive input. For example, add VREF and change. For example, set VREF2 to a voltage like 2V. With VREF2 = 2V, VP = 5V, VN = -5 V and RI = 12.5 kohms, you get unequal constant currents of Iin+ = -0.24 mA and Vin- = 0.56 mA.

Upper and Lower Bounds

When do we switch from charging to discharging CI? Basically, there is a need to pick two levels - *an upper and a lower threshold* - to define the bounds of the triangle wave. The circuit ramps up or down, reversing at the upper and lower thresholds.

- With one leg of RI at VN, the output **ramps up** until the **Upper Threshold (Vth+)** is reached. Then RI is switched from VN to VP.

- With one leg of RI at VP, the output **ramps down** until the **Lower Threshold (Vth-)** is reached. Then RI is switched from VP to VN.

Comparator :

Replacing the switch and VP/VN levels in the simplified circuit above. An Op Amp Comparator with two thresholds. This simple yet wondrous circuit changes it's output state from VN to VP (or vise-versa) depending on the upper Vth+ and lower Vth- thresholds.

$$Vth+ = -VN \cdot R1/R2$$
$$Vth- = -VP \cdot R1 / R2$$

Comparator Working:

- o   When Vin > Vth+, the output switches to VP, the POSITIVE output state.

- o   When Vin < Vth-, the output switches to VN, the NEGATIVE output state.

Zener diodes D1 and D2 set the positive and negative output levels:

$$VP=VfD1+VZD2$$
$$VN = VfD2 + VZD1.$$

These output levels do double duty. Not only do they set the comparator thresholds, but also set the voltage levels for the next stage - the integrator.

SAW-TOOTH WAVE GENERATOR

Circuit Diagram:
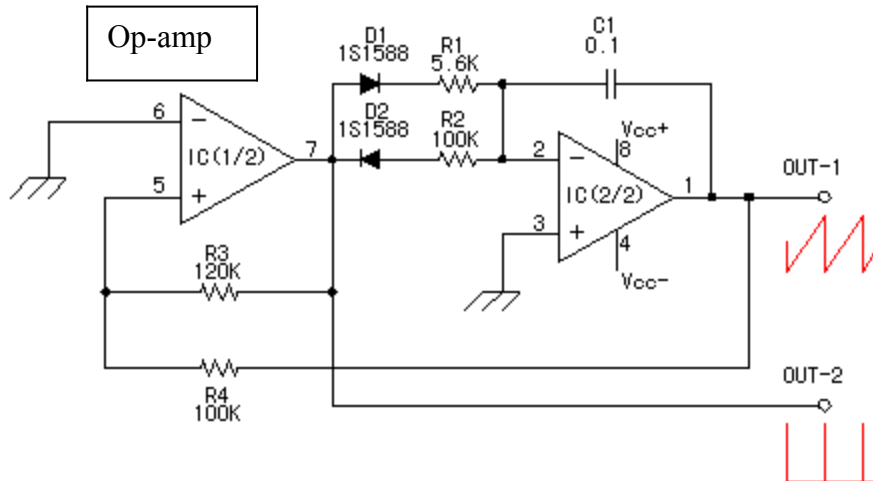
Output Waveform:
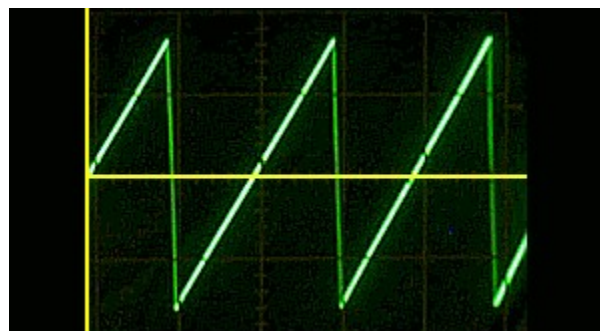
The sawtooth wave oscillator which used the operational amplifier. The composition of this circuit is the same as the triangular wave oscillator basically and is using two operational amplifiers. At the circuit diagram above, IC(1/2) is the Schmitt circuit and IC(2/2) is the integration circuit. The difference with the triangular wave oscillator is to be changing the time of the charging and the discharging of the capacitor. When the output of IC(1/2) is positive voltage, it charges rapidly by the small resistance(R1) value.(When the integration output voltage falls) When the output of IC(1/2) is negative voltage, it is made to charge gradually at the big resistance(R2) value. The output waveform of the integration circuit becomes a form like the tooth of the saw. Such voltage is used for the control of the electron beam (the scanning line) of the television, When picturing a picture at the cathode-ray tube, an electron beam is moved comparative slow. (When the electron beam moves from the left to the right on the screen)

When turning back, it is rapidly moved.(When moving from the right to the left)

Like the triangular wave oscillator, the line voltage needs both of the positive power supply and the negative power supply. Also, to work in the oscillation, the condition of R3>R4 is necessary. However, when making the value of R4 small compared with R3, the output voltage becomes small. The near value is good for R3 and R4. You may make opposite if not oscillating using the resistor with the same value. The circuit diagram above is using the resistor with the value which is different to make oscillate surely.

The oscillation frequency can be calculated by the following formula.

$$f = \frac{1}{2C(R_1 + R_2)} \left(\frac{R_3}{R_4} \right)$$

When calculating at the value which is shown with the circuit diagram, the oscillation frequency is as follows.

$f = (1/2C(R_1+R_2))\times(R_3/R_4)$
$ = (1/(2\times0.1\times10^{-6}\times(5.6\times10^3+100\times10^3)))\times(120\times10^3/100\times10^3)$
$ = (1/(21.12\times10^{-3}))\times1.2$
$ = 56.8\ Hz$

A Typical Sawtooth Wave Generator Circuit

The circuit shown here is an another example of a sawtooth wave generator. Like the previous circuit this circuit produces two outputs. One is the V_{ST}, the sawtooth voltage from the integrator. And the another output from the comparator switching from negative saturation to zero level as shown in the output waveform. The output from the integrator acts as a comparision voltage for the comparator with the threshold voltage generated from the potential divider.
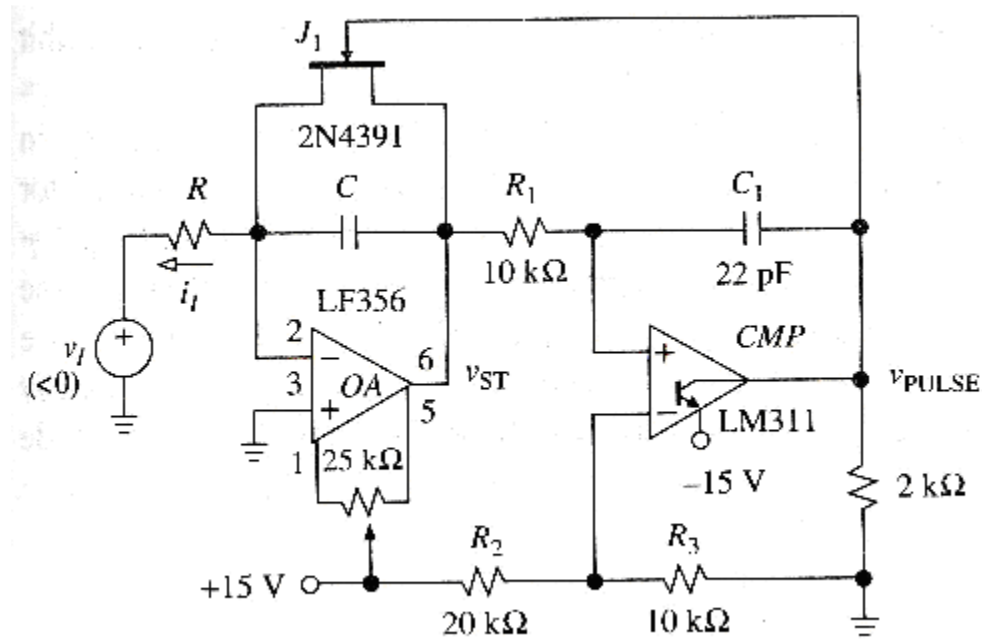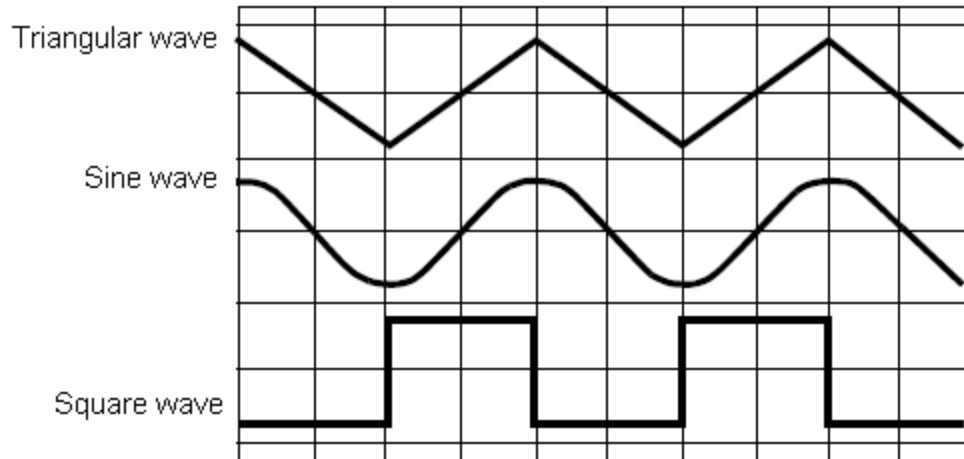

OUPUT WAVEFORM
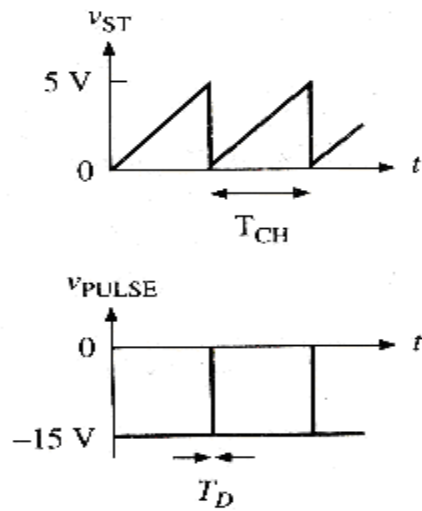
FUNCTION GENERATOR IC 8038:
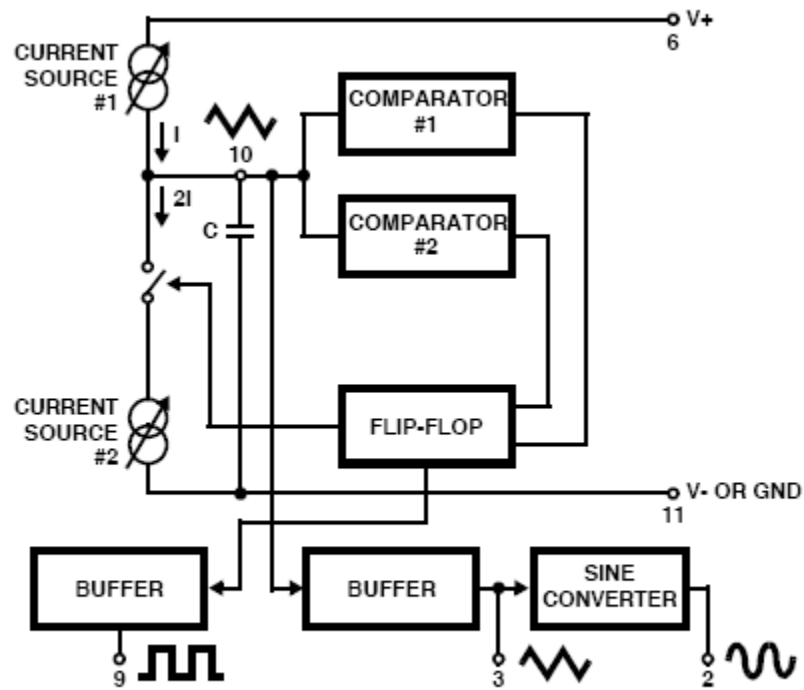
Fig: Functional block diagram of Function generator

Output Waveform:

It consists of two current sources, two comparators, two buffers, one FF and a sine wave converter.

Pin description:

Pin 1 & Pin 12: Sine wave adjusts:

The distortion in the sine wave output can be reduced by adjusting the 100KΩ pots connected between pin12 & pin11 and between pin 1 & 6.

Pin 2 Sine Wave Output:

Sine wave output is available at this pin. The amplitude of this sine wave is 0.22 Vcc.
Where $\pm 5V \leq Vcc \leq \pm 15$ V.

Pin 3 Triangular Wave output:

Triangular wave is available at this pin. The amplitude of the triangular wave is 0.33Vcc.
Where $\pm 5V \leq Vcc \leq \pm 15$ V.

Pin 4 & Pin 5 Duty cycle / Frequency adjust:

The symmetry of all the output wave forms & 50% duty cycle for the square wave output is adjusted by the external resistors connected from Vcc to pin 4. These external resistors & capacitors at pin 10 will decide the frequency of the output wave forms.

Pin 6   + Vcc:

Positive supply voltage the value of which is between 10 & 30V is applied to this pin.

Pin 7 : FM Bias:

This pin along with pin no8 is used to TEST the IC 8038.

Pin9 : Square Wave Output:

A square wave output is available at this pin. It is an open collector output so that this pin can be connected through the load to different power supply voltages. This arrangement is very useful in making the square wave output.

Pin 10 : Timing Capacitors:

The external capacitor C connected to this pin will decide the output frequency along with the resistors connected to pin 4 & 5.

Pin 11 : -V_{EE} or Ground:

If a single polarity supply is to be used then this pin is connected to supply ground & if ($\pm$) supply voltages are to be used then (-) supply is connected to this pin.

Pin 13 & Pin 14: NC (No Connection)

Important features of IC 8038:
1. All the outputs are simultaneously available.
2. Frequency range : 0.001Hz to 500kHz
3. Low distortion in the output wave forms.
4. Low frequency drift due to change in temperature.
5. Easy to use.

Parameters:

(i) Frequency of the output wave form:

- The output frequency dependent on the values of resistors R1 & R2 along with the external capacitor C connected at pin 10.
- If $R_A = R_B = R$ & if R_C is adjusted for 50% duty cycle then

$$fo = \frac{0.3}{RC} \; ; \quad R_A = R1, \; R_B = R3, \; R_C = R2$$

(ii) Duty cycle / Frequency Adjust : (Pin 4 & 5):

Duty cycle as well as the frequency of the output wave form can be adjusted by controlling the values of external resistors at pin 4 & 5.

- The values of resistors R_A & R_B connected between Vcc * pin 4 & 5 respectively along with the capacitor connected at pin 10 decide the frequency of the wave form.
- The values of R_A & R_B should be in the range of 1kΩ to 1MΩ.

(iii) FM Bias:

- The FM Bias input (pin7) corresponds to the junction of resistors R1 & R2.
- The voltage Vin is the voltage between Vcc & pin8 and it decides the output frequency.
- The output frequency is proportional to Vin as given by the following expression
    For $R_A = R_B$ (50% duty cycle).

$$fo = \frac{1.5 Vin}{CRAVcc} \qquad ; \; \text{where C is the timing capacitor}$$

- With pin 7 & 8 connected to each other the output frequency is given by

$$fo = \frac{0.3}{RC}$$

where $R = R_A = R_B$ for 50% duty cycle.

- This is because $Vin = \frac{R1}{R1 + R2} \, Vcc$

(iv) FM Sweep input (pin 8):

- This input should be connected to pin 7, if we want a constant output frequency.
- But if the output frequency is supposed to vary, then a variable dc voltage should be applied to this pin.
- The voltage between Vcc & pin 8 is called Vin and it decides the output frequency as,

$$fo = \frac{1.5 \, Vin}{C \, R_A \, Vcc}$$

A potentiometer can be connected to this pin to obtain the required variable voltage required to change the output frequency.

THE 555 TIMER IC

The 555 is a monolithic timing circuit that can produce accurate & highly stable time delays or oscillation. The timer basically operates in one of two modes: either

(i)   Monostable (one - shot) multivibrator or

(ii)   Astable (free running) multivibrator

The important features of the 555 timer are these:

(i)   It operates on +5v to +18 v supply voltages

(ii)   It has an adjustable duty cycle

(iii)   Timing is from microseconds to hours

(iv)   It has a current o/p

PIN CONFIGURATION OF 555 TIMER:
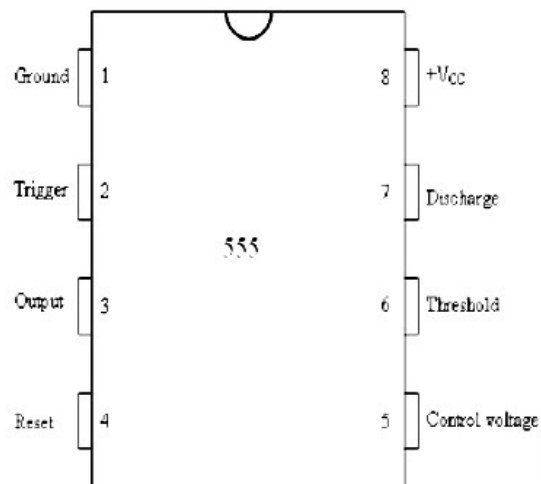
Pin description:

Pin 1: Ground:

All voltages are measured with respect to this terminal.

Pin 2: Trigger:

The o/p of the timer depends on the amplitude of the external trigger pulse applied to this pin.

Pin 3: Output:

There are 2 ways a load can be connected to the o/p terminal either between pin3 & ground or between pin 3 & supply voltage

(Between Pin 3 & Ground➔ ON load)

(Between Pin 3 & + Vcc ➔ OFF load)

(i)   When the input is low:

The load current flows through the load connected between Pin 3 & +Vcc in to the output terminal & is called the sink current.

(ii)   When the output is high:

The current through the load connected between Pin 3 & +Vcc (i.e. ON load) is zero. However the output terminal supplies current to the normally OFF load. This current is called the source current.

Pin 4: Reset:

The 555 timer can be reset (disabled) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to +Vcc to avoid any false triggering.

Pin 5: Control voltage:

An external voltage applied to this terminal changes the threshold as well as trigger voltage. In other words by connecting a potentiometer between this pin & GND, the pulse width of the output waveform can be varied. When not used, the control pin should be bypassed to ground with 0.01 capacitor to prevent any noise problems.

Pin 6: Threshold:

This is the non inverting input terminal of upper comparator which monitors the voltage across the external capacitor.

Pin 7: Discharge:

This pin is connected internally to the collector of transistor Q1.

When the output is high Q1 is OFF.

When the output is low Q is (saturated) ON.

Pin 8: +Vcc:

The supply voltage of +5V to +18V is applied to this pin with respect to ground.

Block Diagram of 555 Timer IC:
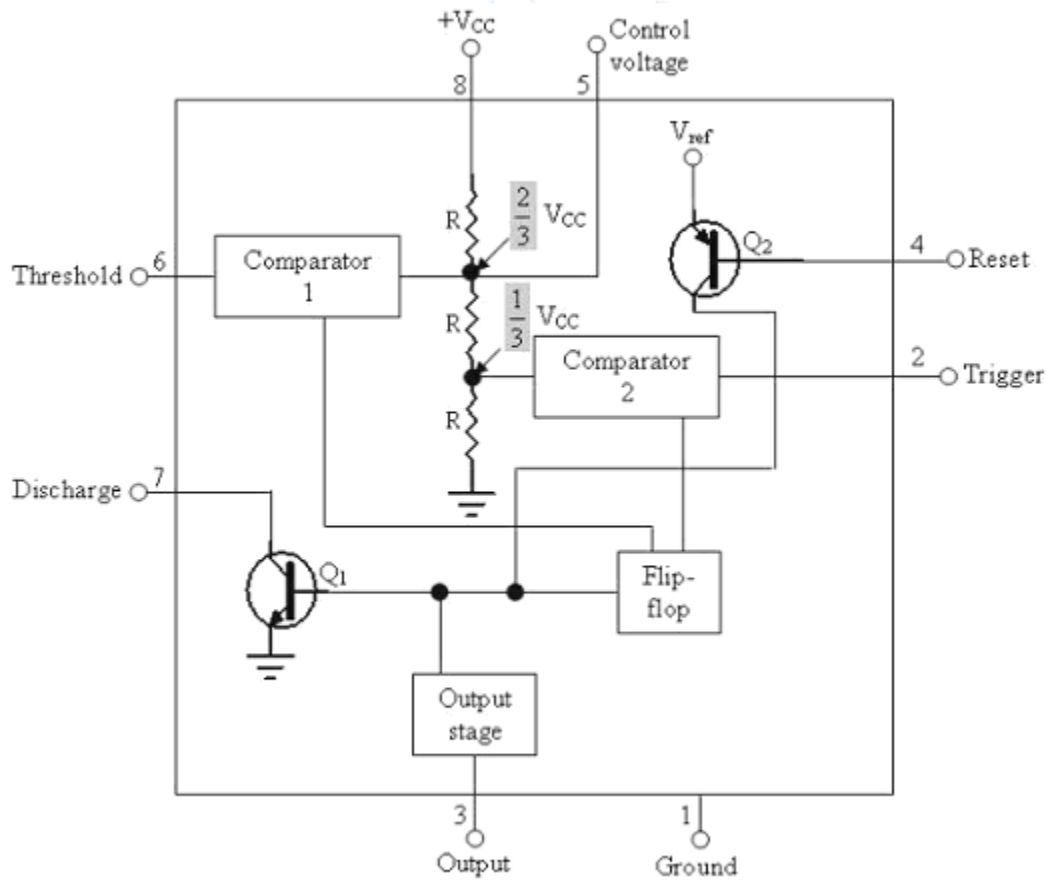
From the above figure, three 5k internal resistors act as voltage divider providing bias voltage of 2/3 Vcc to the upper comparator & 1/3 Vcc to the lower comparator. It is possible to vary time electronically by applying a modulation voltage to the control voltage input terminal (5).

(i) In the Stable state:

The output of the control $\overline{FF}$ is high. This means that the output is low because of power amplifier which is basically an inverter. Q = 1; Output = 0

(ii) At the Negative going trigger pulse:

The trigger passes through (Vcc/3) the output of the lower comparator goes high & sets the FF. Q = 1; $\overline{Q}$ = 0

(iii) At the Positive going trigger pulse: It passes through 2/3Vcc, the output of the upper comparator goes high and resets the FF. Q = 0; $\overline{Q}$ = 1

The reset input (pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator.

Monostable Operation:
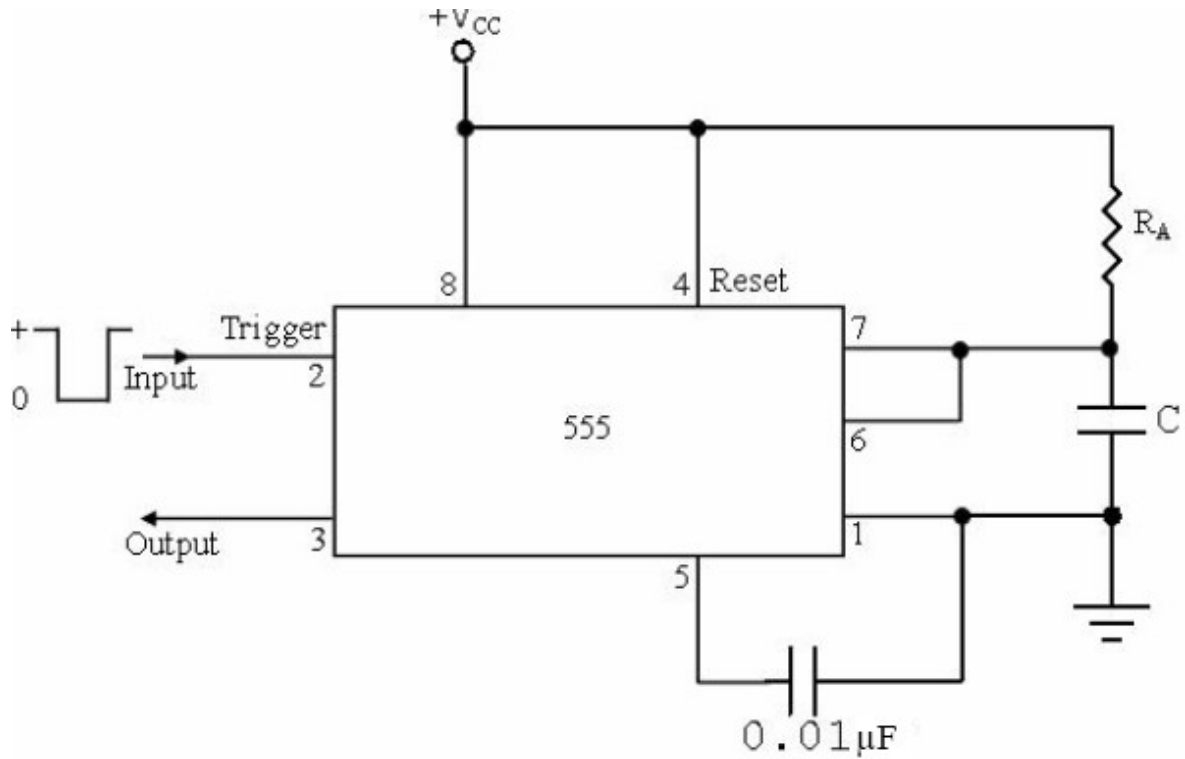
Fig : 555 connected as a Monostable Multivibrator

Model Graph:
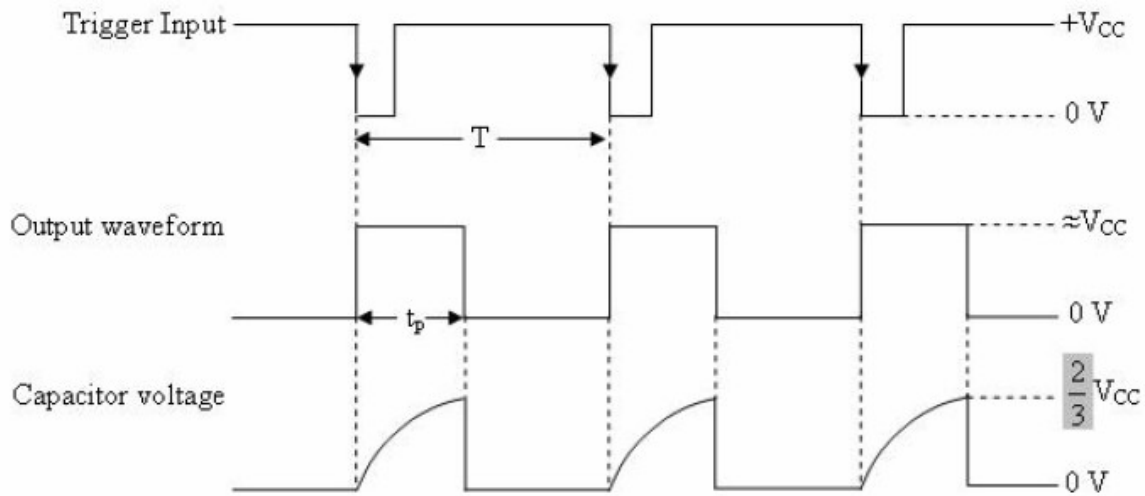
Initially when the output is low, i.e. the circuit is in a stable state, transistor Q1 is ON & capacitor C is shorted to ground. The output remains low. During negative going trigger pulse, transistor Q1

is OFF, which releases the short circuit across the external capacitor C & drives the output high. Now the capacitor C starts charging toward Vcc through R_A. When the voltage across the capacitor equals 2/3 Vcc, upper comparator switches from low to high. i.e. Q = 0, the transistor Q1 = OFF ; the output is high.

(a)

(b)

(c)

(d)

(e)
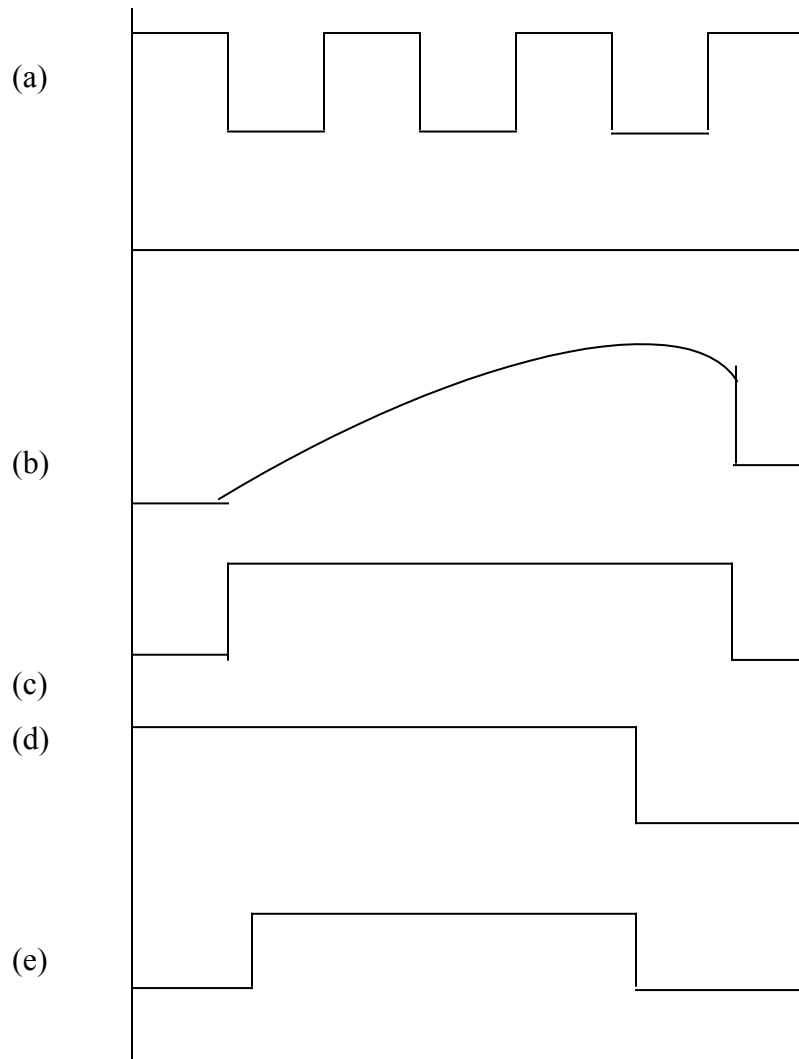
Since C is unclamped, voltage across it rises exponentially through R towards Vcc with a time constant RC (fig b) as shown in below. After the time period, the upper comparator resets the FF, i.e. Q = 1, Q1 = ON; the output is low.[i.e discharging the capacitor C to ground potential (fig c)]. The voltage across the capacitor as in fig (b) is given by

$$Vc = Vcc \ (1-e^{-t/RC}) \ \dots\dots\dots\dots \ (1)$$

Therefore At   t = T,   Vc = 2/3 Vcc

$$2/3 \ Vcc = Vcc(1-e^{-T/RC})$$

or

$$T = RC \ ln \ (1/3)$$

Or

$$T = 1.1RC \ seconds \qquad \dots\dots\dots\dots \ (2)$$

If the reset is applied Q2 = OFF, Q1 = ON, timing capacitor C immediately discharged. The output now will be as in figure (d & e). If the reset is released output will still remain low until a negative going trigger pulse is again applied at pin 2.

Applications of Monostable Mode of Operation:

(a) Frequency Divider:

The 555 timer as a monostable mode. It can be used as a frequency divider by adjusting the length of the timing cycle t_p with respect to the time period T of the trigger input. To use the monostable multivibrator as a divide by 2 circuit, the timing interval t_p must be a larger than the time period of the trigger input. [Divide by 2➔ t_p > T of the trigger]

By the same concept, to use the monostable multivibrator as a divide by 3 circuit, t_p must be slightly larger than twice the period of the input trigger signal & so on, [divide by 3 ➔ t_p > 2T of trigger]
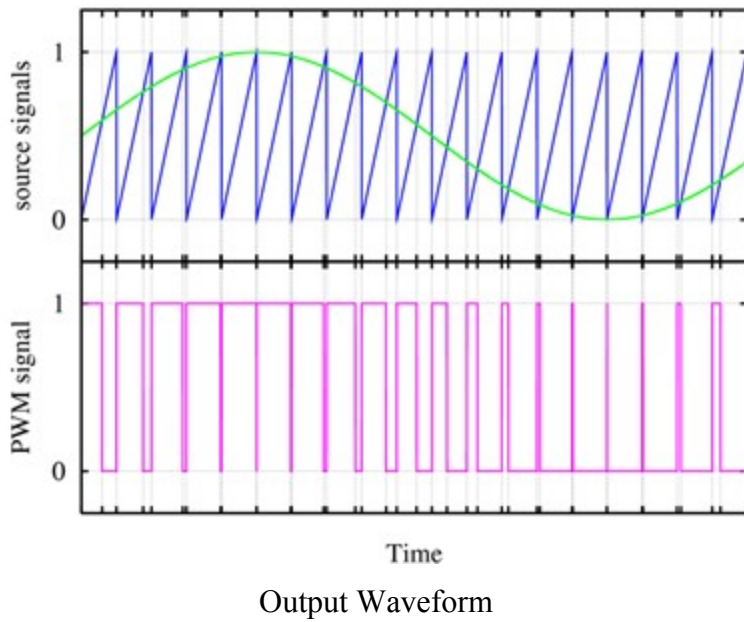
(b) Pulse width modulation:
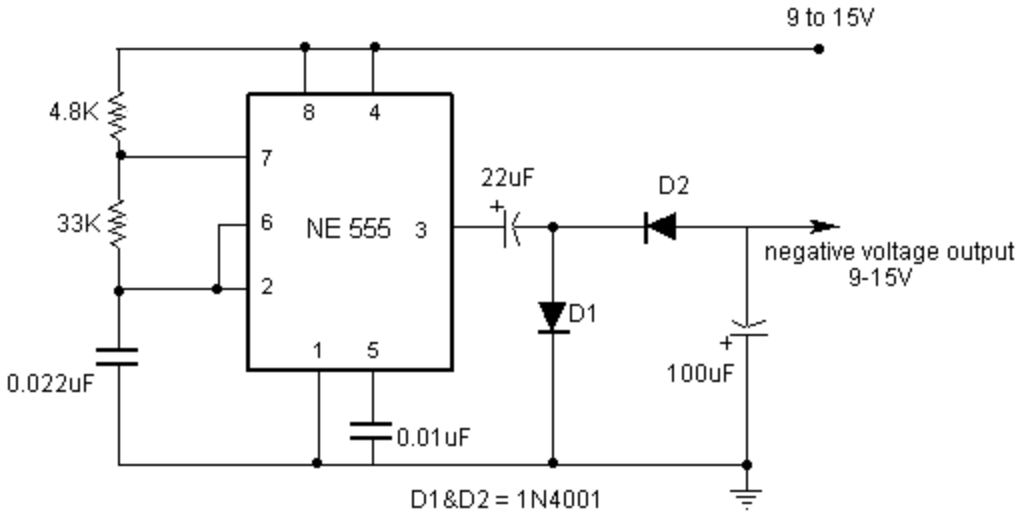
Fig: Pulse Width Modulation

Output Waveform

Pulse width of a carrier wave changes in accordance with the value of a incoming (modulating signal) is known as PWM. It is basically monostable multivibrator. A modulating

signal is fed in to the control voltage (pin 5). Internally, the control voltage is adjusted to 2/3 Vcc externally applied modulating signal changes the control voltage level of upper comparator. As a result, the required to change the capacitor up to threshold voltage level changes, giving PWM output.

(c) Pulse Stretcher:

This application makes use of the fact that the output pulse width (timing interval) of the monostable multivibrator is of longer duration than the negative pulse width of the input trigger. As such, the output pulse width of the monostable multivibrator can be viewed as a stretched version of the narrow input pulse, hence the name " Pulse stretcher". Often, narrow –pulse width signals are not suitable for driving an LED display, mainly because of their very narrow pulse widths. In other words, the LED may be flashing but not be visible to the eye because its on time is infinitesimally small compared to its off time. The 55 pulse stretcher can be used to remedy this problem. The LED will be ON during the timing interval $t_p = 1.1R_AC$ which can be varied by changing the value of R_A & C.
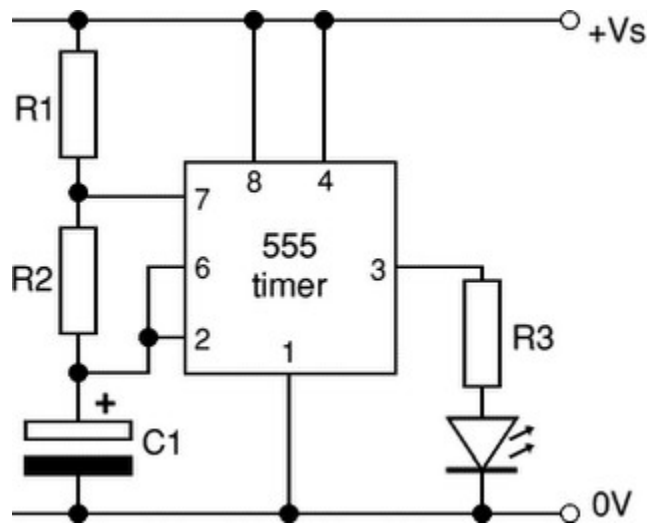
Fig: Pulse Stretcher

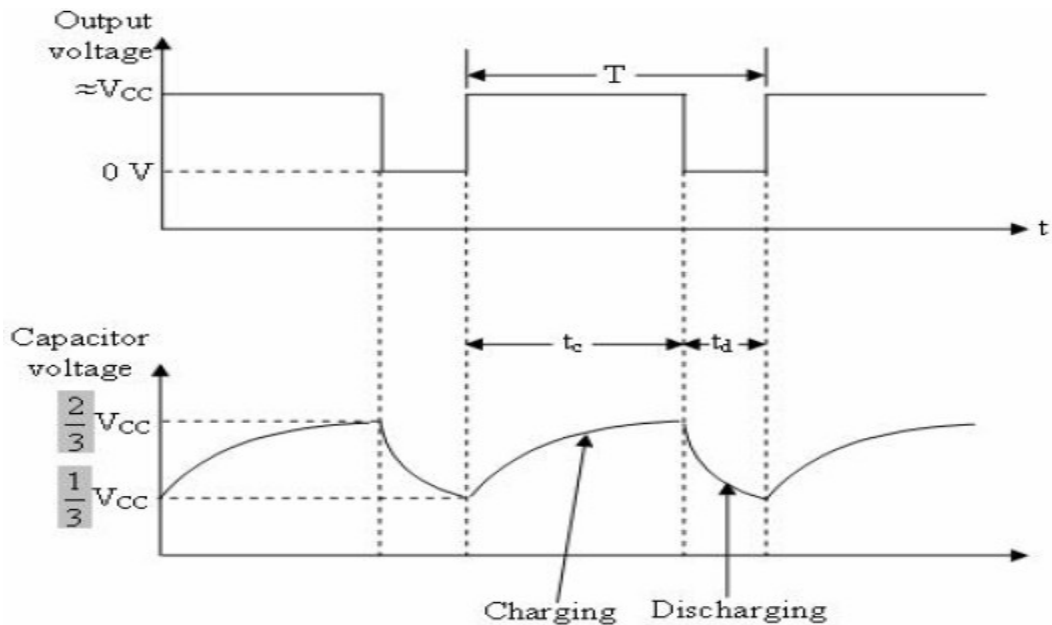**The 555 timer as an Astable Multivibrator:**

An Astable multivibrator, often called a free running multivibrator, is a rectangular wave generating circuit. Unlike the monostable multivibrator, this circuit does not require an

external trigger to change the state of the output, hence the name free running. However, the time during which the output is either high or low is determined by 2 resistors and capacitors, which are externally connected to the 55 timer.

Fig: Astable Multivibrator
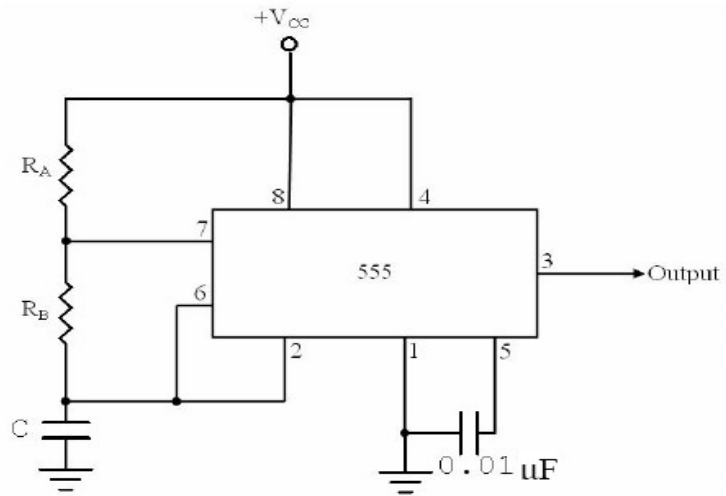
Model Graph

The above figures show the 555 timer connected as an astable multivibrator and its model graph

Initially, when the output is high :

Capacitor C starts charging toward Vcc through R_A & R_B. However, as soon as voltage across the capacitor equals 2/3 Vcc. Upper comparator triggers the FF & output switches low.

When the output becomes Low:

Capacitor C starts discharging through R_B and transistor Q1, when the voltage across C equals 1/3 Vcc, lower comparator output triggers the FF & the output goes High. Then cycle repeats. The capacitor is periodically charged & discharged between 2/3 Vcc & 1/3 Vcc respectively. The time during which the capacitor charges from 1/3 Vcc to 2/3 Vcc equal to the time the output is high & is given by

$$t_c = (R_A + R_B)C \ln 2 \ldots\ldots\ldots\ldots (1) \text{ Where } [\ln 2 = 0.69]$$

$$= 0.69 (R_A + R_B)C$$

Where R_A & R_B are in ohms. And C is in farads.

Similarly, the time during which the capacitors discharges from 2/3 Vcc to 1/3 Vcc is equal to the time, the output is low and is given by,

$$t_c = R_B C \ln 2$$

$$t_d = 0.69 R_B C \ldots\ldots\ldots\ldots\ldots (2)$$

where R_B is in ohms and C is in farads.

Thus the total period of the output waveform is

$$T = t_c + t_d = 0.69 (R_A + 2R_B)C \ldots\ldots\ldots\ldots (3)$$

This, in turn, gives the frequency of oscillation as, $f_0 = 1/T = 1.45/(R_A + 2R_B)C \ldots\ldots\ldots (4)$

Equation 4 indicates that the frequency f_0 is independent of the supply voltage Vcc. Often the term duty cycle is used in conjunction with the astable multivibrator. The duty cycle is the ratio of the time t_c during which the output is high to the total time period T. It is generally expressed as a percentage.

$$\% \text{ duty cycle} = (t_c / T)* 100$$

$$\% \text{ DC} = [(R_A+R_B)/ /(R_A+2R_B)] * 100$$

Astable Multivibrator Applications:
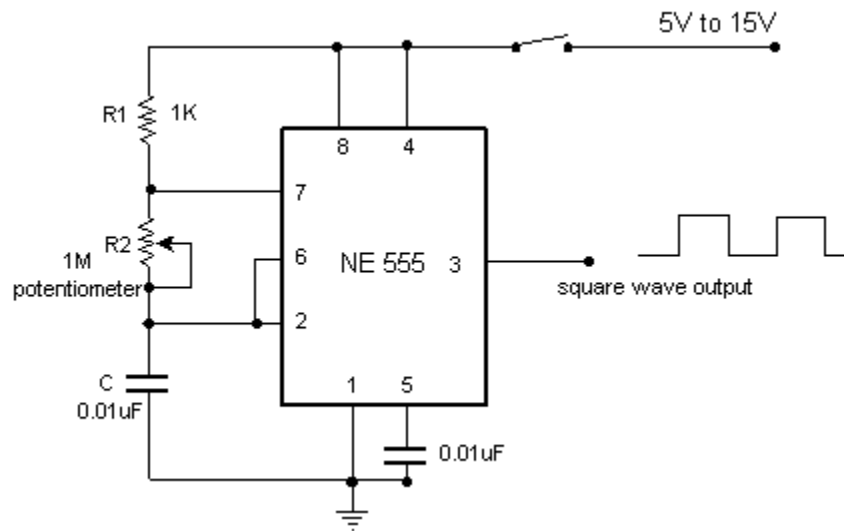
(a) Square wave oscillator:

Fig: Square Wave Oscillator

With out reducing $R_A = 0$ ohm, the astable multivibrator can be used to produce square wave output. Simply by connecting diode D across Resistor R_B. The capacitor C charges through R_A & diode D to approximately

2/3 Vcc & discharges through R_B & Q1 until the capacitor voltage equals approximately 1/3 Vcc, then the cycle repeats.

To obtain a square wave output, R_A must be a combination of a fixed resistor & potentiometer so that the potentiometer can be adjusted for the exact square wave.

(b) Free – running Ramp generator:

Circuit   *Trigger and Ramp Waveforms*
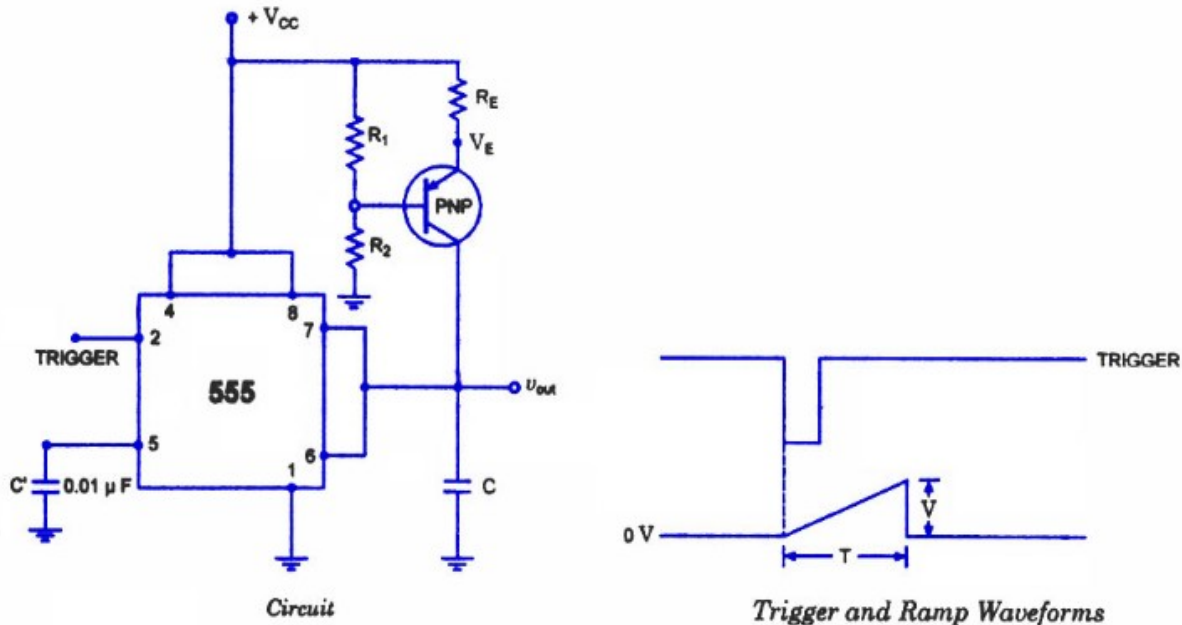
Ramp Generator Using The Timer 555

- The astable multivibrator can be used as a free – running ramp generator when resistor R_A & R_B are replaced by a current mirror.
- The current mirror starts charging capacitor C toward Vcc at a constant rate.
- When voltage across **C equals to 2/3 Vcc**, upper comparator turns transistor Q1 ON & C rapidly discharges through transistor Q1.
- When voltage across **C equals to 1/3 Vcc**, lower comparator switches transistor OFF & then capacitor C starts charging up again..
- Thus the charge – discharge cycle keeps repeating.
- The discharging time of the capacitor is relatively negligible compared to its charging time.
- The time period of the ramp waveform is equal to the charging time & is approximately is given by,

$$T = \text{Vcc}C/3I_C \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(1)}$$

$$I_C = (\text{Vcc} - V_{BE})/R = \text{constant current}$$

Therefore the free – running frequency of ramp generator is

$$f_0 = 3I_C/\text{Vcc } C \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots.\text{(2)}$$
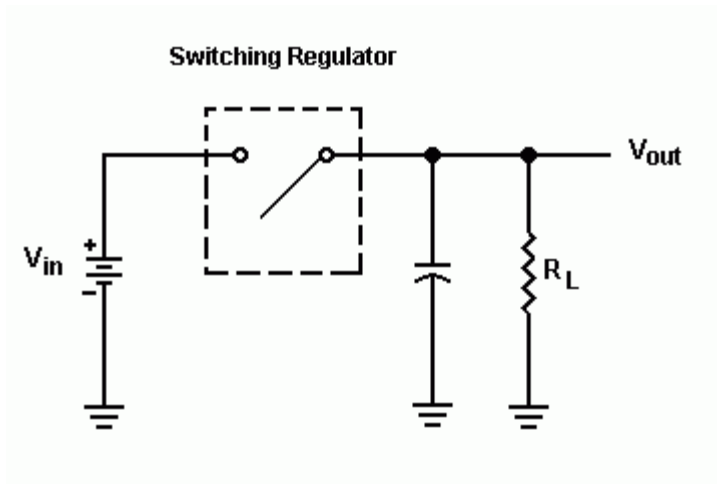
SWITCHING REGULATORS

Introduction

The switching regulator is increasing in popularity because it offers the advantages of higher power conversion efficiency and increased design flexibility (multiple output voltages of different polarities can be generated from a single input voltage).

Although most power supplies used in amateur shacks are of the linear regulator type, an increasing number of switching power supplies have become available to the amateur. For most amateurs the switching regulator is still somewhat of a mystery. One might wonder why we even bother with these power supplies, when the existing linear types work just fine. The primary advantage of a switching regulator is very high efficiency, a lot less heat and smaller size. To understand how these black boxes work lets take a look at a traditional linear regulator at right. As we see in the diagram, the linear regulator is really nothing more than a variable resistor. The resistance of the regulator varies in accordance with the load resulting in a constant output voltage
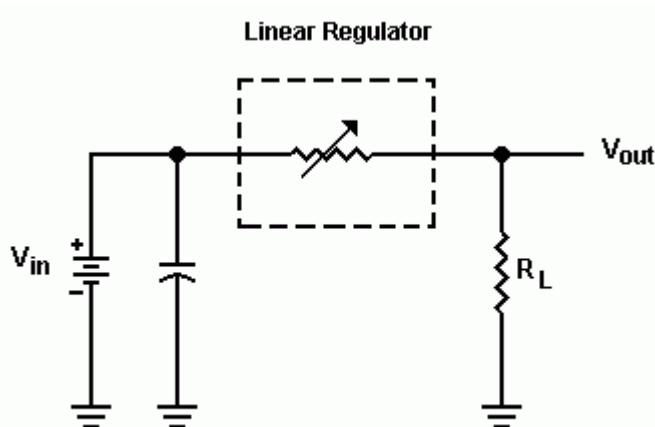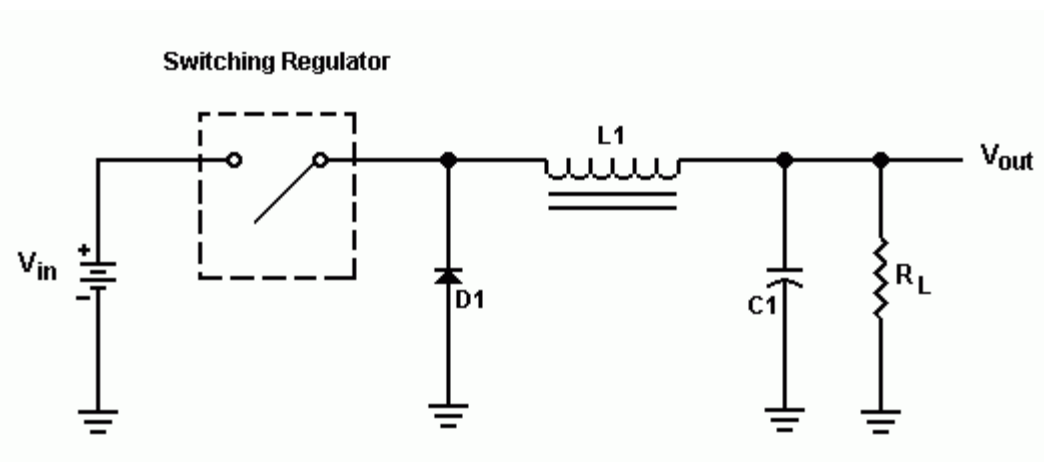

Linear Regulator

The primary filter capacitor is placed on the input to the regulator to help filter out the 60 cycle ripple. The linear regulator does an excellent job but not without cost. For example, if the output voltage is 12 volts and the input voltage is 24 volts then we must drop 12 volts across the regulator. At output currents of 10 amps this translates into 120 watts (12 volts times 10 amps) of heat energy that the regulator must dissipate. Is it any wonder why we have to use those massive heat sinks? As we can see this results in a mere 50% efficiency for the linear regulator and a lot of wasted power which is normally transformed into heat.

Switching Regulator

The time that the switch remains closed during each switch cycle is varied to maintain a constant output voltage. Notice that the primary filter capacitor is on the output of the regulator and not the input. As is apparent, the switching regulator is much more efficient than the linear regulator achieving efficiencies as high as 80% to 95% in some circuits. The obvious result is smaller heat sinks, less heat and smaller overall size of the power supply.

The previous diagram is really an over simplification of a switching regulator circuit. An actual switching regulator circuit more closely resembles the circuit below: Now lets take a look   at   a   very   basic   switching   regulator   at   right. As we see can see, the switching regulator is really nothing more than just a simple switch. This switch goes on and off at a fixed rate usually between 50Khz to 100Khz as set by the circuit.

Switching Regulator

As we see above the switching regulator appears to have a few more components than a linear regulator. Diode D1 and Inductor L1 play a very specific role in this circuit and are found in almost every switching regulator. First, diode D1 has to be a Schottky or other very fast switching diode. A 1N4001 just won't switch fast enough in this circuit. Inductor L1 must be a type of core that does not saturate under high currents. Capacitor C1 is normally a low ESR (Equivalent Series Resistance) type.

To understand the action of D1 and L1, lets look at what happens when S1 is closed as indicated below:
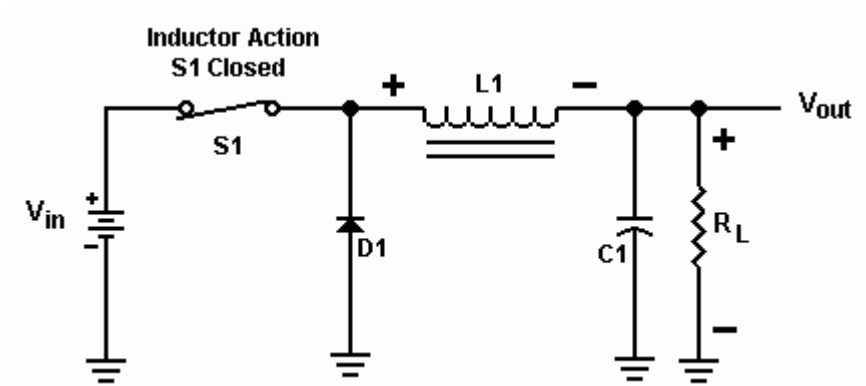
As we see above, L1, which tends to oppose the rising current, begins to generate an electromagnetic field in its core. Notice that diode D1 is reversed biased and is essentially an open circuit at this point. Now lets take a look at what happens when S1 opens below:
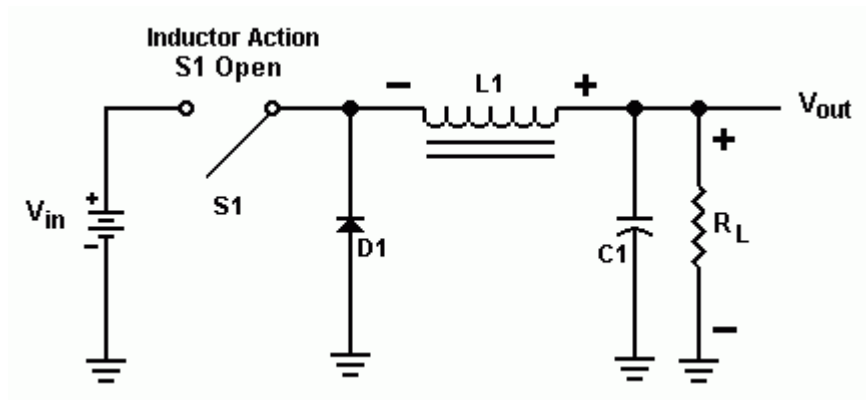
As we see in this diagram the electromagnetic field that was built up in L1 is now discharging and generating a current in the reverse polarity. As a result, D1 is now

conducting and will continue until the field in L1 is diminished. This action is similar to the charging and discharging of capacitor C1. The use of this inductor/diode combination gives us even more efficiency and augments the filtering of C1.

Because of the unique nature of switching regulators, very special design considerations are required. Because the switching system operates in the 50 to 100 kHz region and has an almost square waveform, it is rich in harmonics way up into the HF and even the VHF/UHF region. Special filtering is required, along with shielding, minimized lead lengths and all sorts of toroidal filters on leads going outside the case. The switching regulator also has a minimum load requirement, which is determined by the inductor value. Without the minimum load, the regulator will generate excessive noise and harmonics and could even damage itself. (This is why it is not a good idea to turn on a computer switching power supply without some type of load connected.) To meet this requirement, many designers use a cooling fan and or a minimum load which switches out when no longer needed.

Fortunately, recent switching regulator IC's address most of these design problems quite well. Because of lowered component costs as well as a better understanding of switching regulator technology, we are starting to see even more switching power supplies replacing traditionally linear only applications. It is no doubt that we will see fewer linear power supplies being used in the future.

In this article we addressed basic switching regulator design concepts and it is hoped that amateurs will begin to look at switching regulators much more seriously when they decide to replace an old power supply. In a future construction article, we will review an actual switching regulator circuit.

IC VOLTAGE REGULATORS

Four most commonly used switching converter types:

Buck: used the reduce a DC voltage to a lower DC voltage.

Boost: provides an output voltage that is higher than the input.

Buck-Boost (invert): an output voltage is generated opposite in polarity to the input.

Flyback: an output voltage that is less than or greater than the input can be generated, as well as multiple outputs.

Converters:

Push-Pull: A two-transistor converter that is especially efficient at low input voltages.

Half-Bridge: A two-transistor converter used in many off-line applications.

Full-Bridge: A four-transistor converter (usually used in off-line designs) that can

generate the highest output power of all the types listed.

Application information will be provided along with circuit examples that illustrate some applications of Buck, Boost, and Flyback regulators.

Switching Fundamentals

The law of inductance

If a voltage is forced across an inductor, a current will flow through that inductor (and this current will vary with time). The current flowing in an inductor will be time-varying even if the forcing voltage is constant. It is equally correct to say that if a time-varying current is forced to flow in an inductor, a voltage across the inductor will result. The fundamental law that defines the relationship between the voltage and current in an inductor is given by the equation:

$$v = L \ (di/dt)$$

Two important characteristics of an inductor that follow directly from the law of inductance are:

1) A voltage across an inductor results only from a current that changes with time. A steady (DC) current flowing in an inductor causes no voltage across it (except for the tiny voltage drop across the copper used in the windings).

2) A current flowing in an inductor can not change value instantly (in zero time), as this would require infinite voltage to force it to happen. However, the faster the current is changed in an inductor, the larger the resulting voltage will be. Note: Unlike the current flowing in the inductor, the voltage across it can change instantly (in zero time). The principles of inductance are illustrated by the information contained in Figure.
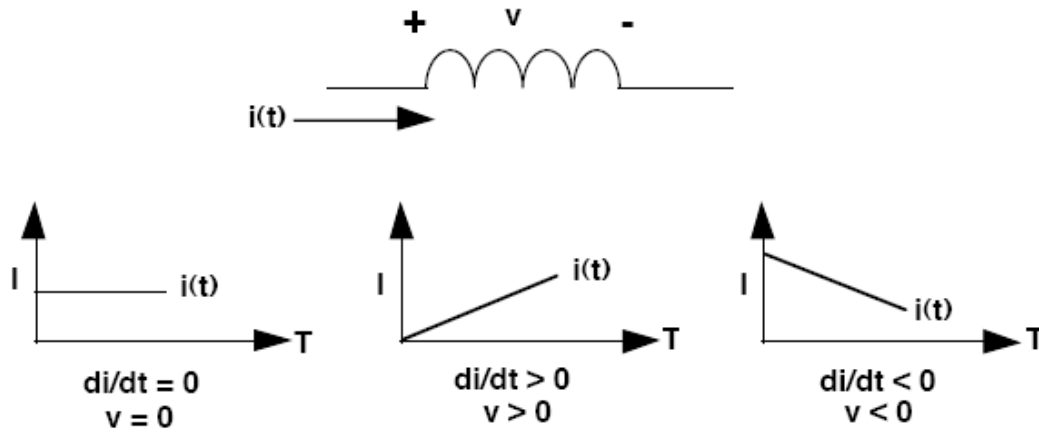
The important parameter is the di/dt term, which is simply a measure of how the current changes with time. When the current is plotted versus time, the value of di/dt is defined as the slope of the current plot at any given point. The graph on the left shows that current which is constant with time has a di/dt value of zero, and results in no voltage across the inductor. The center graph shows that a current which is increasing with time has a positive di/dt value, resulting in a positive inductor voltage.

Current that decreases with time (shown in the right-hand graph) gives a negative value for di/dt and inductor voltage. It is important to note that a linear current ramp in an inductor (either up or down) occurs only when it has a constant voltage across it.

Transformer Operation:

A transformer is a device that has two or more magnetically-coupled windings. The basic operation is shown in Figure. The action of a transformer is such that a time-varying (AC) voltage or current is transformed to a higher or lower value, as set by the transformer turns ratio. The transformer does not add power, so it follows that the power (V X I) on either side must be constant. That is the reason that the winding with more turns has higher voltage but lower current, while the winding with less turns has lower voltage but higher current.

$$V_B = V_A \frac{N2}{N1} \qquad I_B = I_A \frac{N1}{N2} \qquad\qquad V_B = -V_A \frac{N2}{N1} \qquad I_B = -I_A \frac{N1}{N2}$$
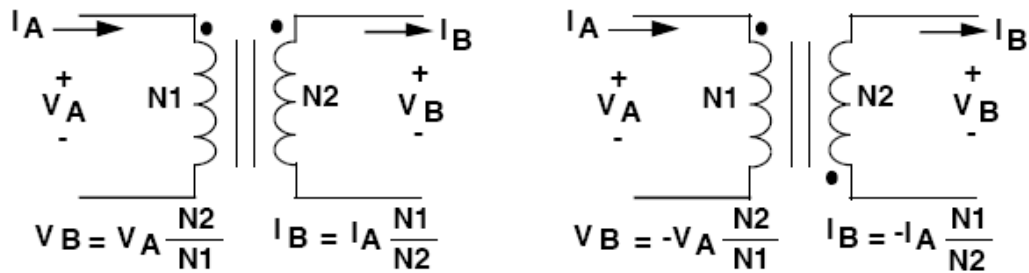
The dot on a transformer winding identifies its polarity with respect to another winding, and reversing the dot results in inverting the polarity.

Example of Transformer Operation:

An excellent example of how a transformer works can be found under the hood of your car, where a transformer is used to generate the 40 kV that fires car's spark plugs.

Spark Firing Circuit:

The "coil" used to generate the spark voltage is actually a transformer, with a very high secondary-to-primary turns ratio. When the points first close, current starts to flow in the primary winding and eventually reaches the final value set by the 12V battery and the current limiting resistor. At this time, the current flow is a fixed DC value, which means no voltage is generated across either winding of the transformer.
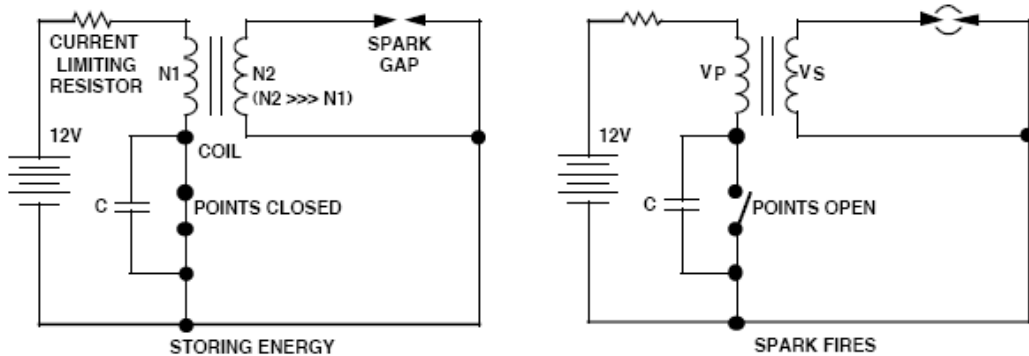
When the points open, the current in the primary winding collapses very quickly, causing a large voltage to appear across this winding. This voltage on the primary is magnetically coupled to (and

stepped up by) the secondary winding, generating a voltage of 30 kV - 40 kV on the secondary side. As explained previously, the law of inductance says that it is not possible to instantly break the current flowing in an inductor (because an infinite voltage would be required to make it happen).

This principle is what causes the arcing across the contacts used in switches that are in circuits with highly inductive loads. When the switch just begins to open, the high voltage generated allows electrons to jump the air gap so that the current flow does not actually stop instantly. Placing a capacitor across the contacts helps to reduce this arcing effect. In the automobile ignition, a capacitor is placed across the points to minimize damage due to arcing when the points "break" the current flowing in the low-voltage coil winding (in car manuals, this capacitor is referred to as a "condenser").

Pulse Width Modulation (PWM):

All of the switching converters that will be covered in this paper use a form of output voltage regulation known as Pulse Width Modulation (PWM). Put simply, the feedback loop adjusts (corrects) the output voltage by changing the ON time of the switching element in the converter. As an example of how PWM works, we will examine the result of applying a series of square wave pulses to an L-C filter (see Figure).
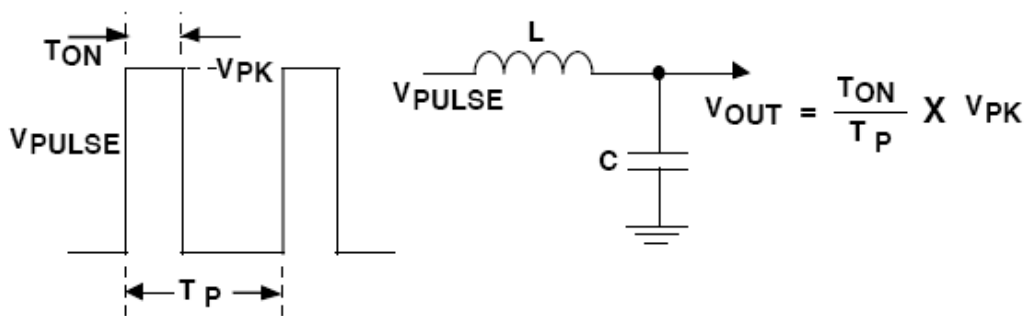

The series of square wave pulses is filtered and provides a DC output voltage that is equal to the peak pulse amplitude multiplied times the duty cycle (duty cycle is defined as the switch ON time divided by the total period). This relationship explains how the output voltage can be directly controlled by changing the ON time of the switch.

Switching Converter Topologies

The most commonly used DC-DC converter circuits will now be presented along with

the basic principles of operation.

Buck Regulator:

The most commonly used switching converter is the Buck, which is used to down-convert a DC

voltage to a lower DC voltage of the same polarity. This is essential in systems that use distributed

power rails (like 24V to 48V), which must be locally converted to 15V, 12V or 5V with very little

power loss. The Buck converter uses a transistor as a switch that alternately connects and

disconnects the input voltage to an inductor (see Figure).
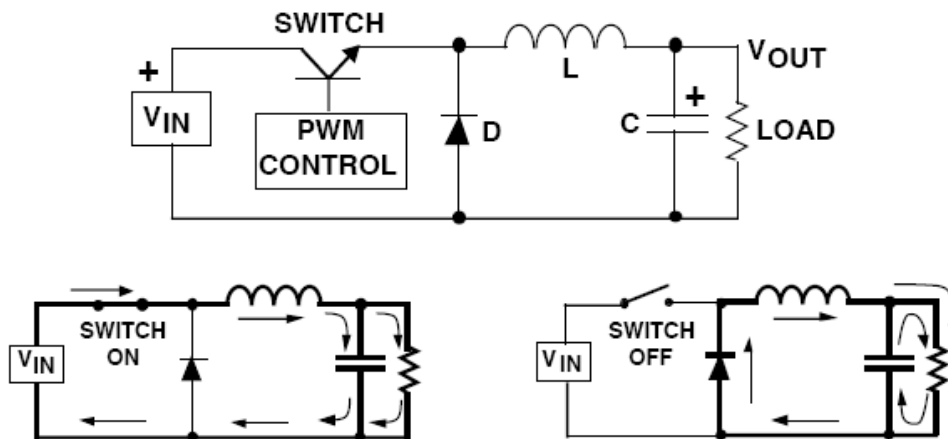
The lower diagrams show the current flow paths (shown as the heavy lines) when the switch is on

and off. When the switch turns on, the input voltage is connected to the inductor. The difference

between the input and output voltages is then forced across the inductor, causing current through

the inductor to increase. During the on time, the inductor current flows into both the load and the

outputcapacitor (the capacitor charges during this time).

When the switch is turned off, the input voltage applied to the inductor is removed. However, since

the current in an inductor can not change instantly, the voltage across the inductor will adjust to

hold the current constant. The input end of the inductor is forced negative in voltage by the

decreasing current, eventually reaching the point where the diode is turned on. The inductor

current then flows through the load and back through the diode. The capacitor discharges into the

load during the off time, contributing to the total current being supplied to the load (the total load current during the switch off time is the sum of the inductor and capacitor current).
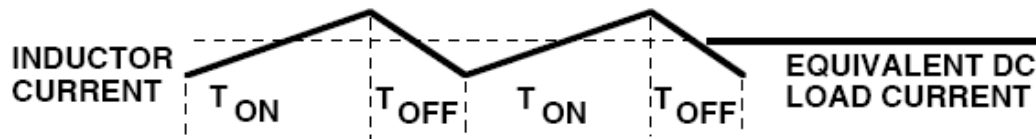

FIGURE 30. BUCK REGULATOR INDUCTOR CURRENT

The shape of the current flowing in the inductor is similar to previous figure. As explained, the current through the inductor ramps up when the switch is on, and ramps down when the switch is off. The DC load current from the regulated output is the average value of the inductor current. The peak-to-peak difference in the inductor current waveform is referred to as the inductor ripple current, and the inductor is typically selected large enough to keep this ripple current less than 20% to 30% of the rated DC current.

Continuous vs. Discontinuous operation

In most Buck regulator applications, the inductor current never drops to zero during
Full-load operation (this is defined as continuous mode operation). Overall performance is usually better using continuous mode, and it allows maximum output power to be obtained from a given input voltage and switch current rating. In applications where the maximum load current is fairly low, it can be advantageous to design for discontinuous mode operation. In these cases, operating in discontinuous mode can result in a smaller overall converter size (because a smaller inductor can be used).Discontinuous mode operation at lower load current values is generally harmless, and even converters designed for continuous mode operation at full load will become discontinuous as the load current is decreased (usually causing no problems).

Boost Regulator:

The Boost regulator takes a DC input voltage and produces a DC output voltage that is higher in value than the input (but of the same polarity). The Boost regulator is shown in Figure, along with

details showing the path of current flow during the switch on and off time. Whenever the switch is on, the input voltage is forced across the inductor which causes the current through it to increase (ramp up).
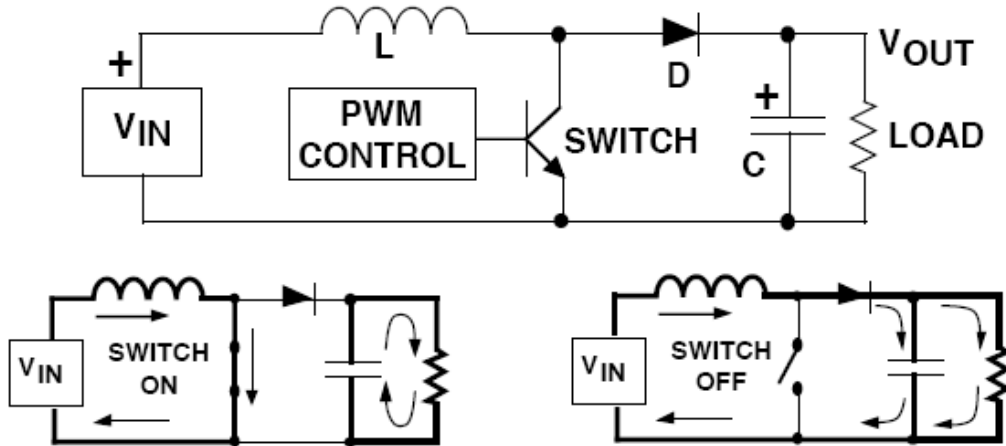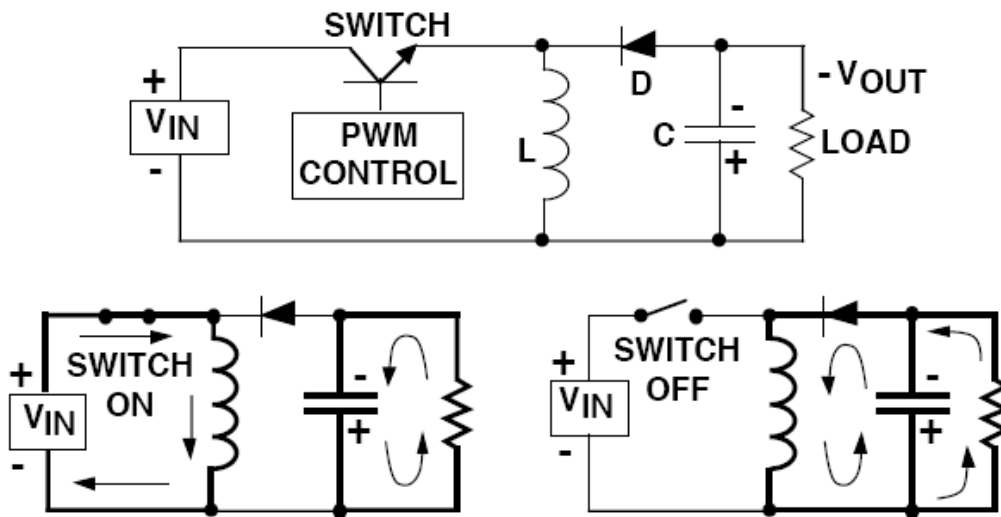

When the switch is off, the decreasing inductor current forces the "switch" end of the inductor to swing positive. This forward biases the diode, allowing the capacitor to charge up to a voltage that is higher than the input voltage. During steady-state operation, the inductor current flows into both the output capacitor and the load during the switch off time. When the switch is on, the load current is supplied only by the capacitor.

Output Current and Load power:

An important design consideration in the Boost regulator is that the output load current and the switch current are not equal, and the maximum available load current is always less than the current rating of the switch transistor. It should be noted that the maximum total power available for conversion in any regulator is equal to the input voltage multiplied times the maximum average input current (which is less than the current rating of the switch transistor). Since the output voltage of the Boost is higher than the input voltage, it follows that the output current must be lower than the input current.

**Buck-Boost (Inverting) Regulator:**

The Buck-Boost or Inverting regulator takes a DC input voltage and produces a DC output voltage that is opposite in polarity to the input. The negative output voltage can be either larger or smaller in magnitude than the input voltage. The Inverting regulator is shown in Figure.

When the switch is on, the input voltage is forced across the inductor, causing an increasing current flow through it. During the on time, the discharge of the output capacitor is the only source of load current. This requires that the charge lost from the output capacitor during the on time be replenished during the off time. When the switch turns off, the decreasing current flow in the inductor causes the voltage at the diode end to swing negative. This action turns on the diode, allowing the current in the inductor to supply both the output capacitor and the load. As shown, the load current is supplied by inductor when the switch is off, and by the output capacitor when the switch is on.

Flyback Regulator:

The Flyback is the most versatile of all the topologies, allowing the designer to create one or more output voltages, some of which may be opposite in polarity. Flyback converters have gained popularity in battery-powered systems, where a single voltage must be converted into the required system voltages (for example, +5V, +12V and -12V) with very high power conversion efficiency. The basic single-output flyback converter is shown in Figure.
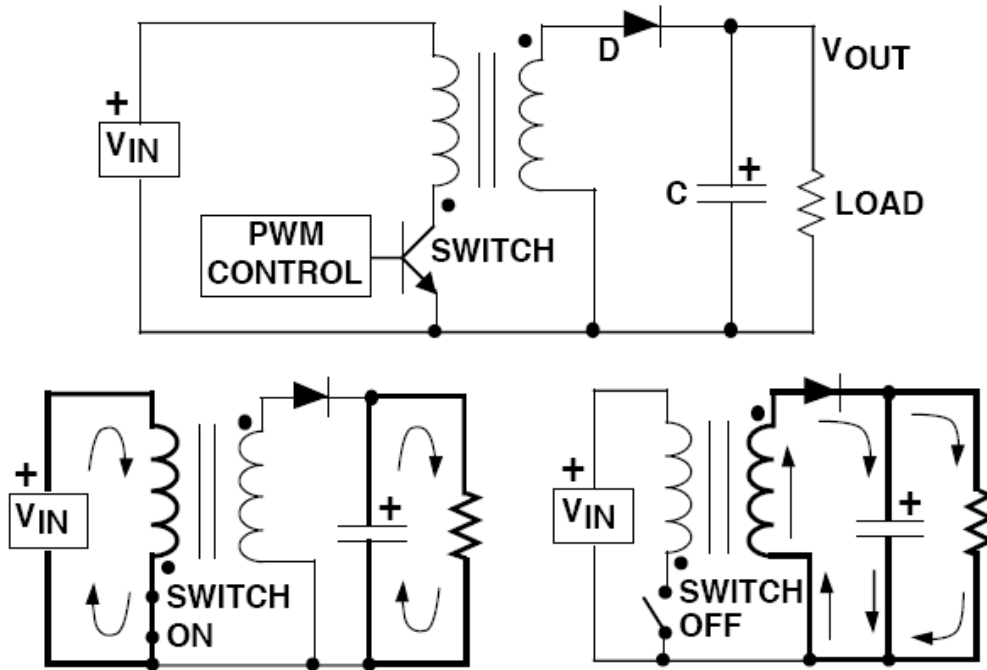
The most important feature of the Flyback regulator is the transformer phasing, as shown by the dots on the primary and secondary windings.   When the switch is on, the input voltage is forced across the transformer primary which causes an increasing flow of current through it.   Note that the polarity of the voltage on the primary is dot-negative (more negative at the dotted end), causing a voltage with the same polarity to appear at the transformer secondary (the magnitude of the secondary voltage is set by the transformer seconday-to-primary turns ratio).

The dot-negative voltage appearing across the secondary winding turns off the diode, reventing current flow in the secondary winding during the switch on time.   During this time, the load current must be supplied by the output capacitor alone. When the switch turns off, the decreasing current flow in the primary causes the voltage at the dot end to swing positive. At the same time, the primary voltage is reflected to the secondary with the same polarity. The dot-positive voltage occurring across the secondary winding turns on the diode, allowing current to flow into both the load and the output capacitor. The output capacitor charge lost to the load during the switch on time is replenished during the switch off time. Flyback converters operate in either   continuous mode (where the secondarycurrent is always >0) or discontinuous mode (where the secondary current falls to zero on each cycle).

Generating Multiple Outputs:

Another big advantage of a Flyback is the capability of providing multiple outputs .In such applications, one of the outputs (usually the highest current) is selected to provide PWM feedback to the control loop, which means this output is directly regulated. The other secondary winding(s) are indirectly regulated, as their pulse widths will follow the regulated winding.   The load regulation on the unregulated secondaries is not great (typically 5 - 10%), but is adequate for many applications.

If tighter regulation is needed on the lower current secondaries, an LDO post-regulator is an excellent solution. The secondary voltage is set about 1V above the desired output voltage, and the LDO provides excellent output regulation withvery little loss of efficiency.
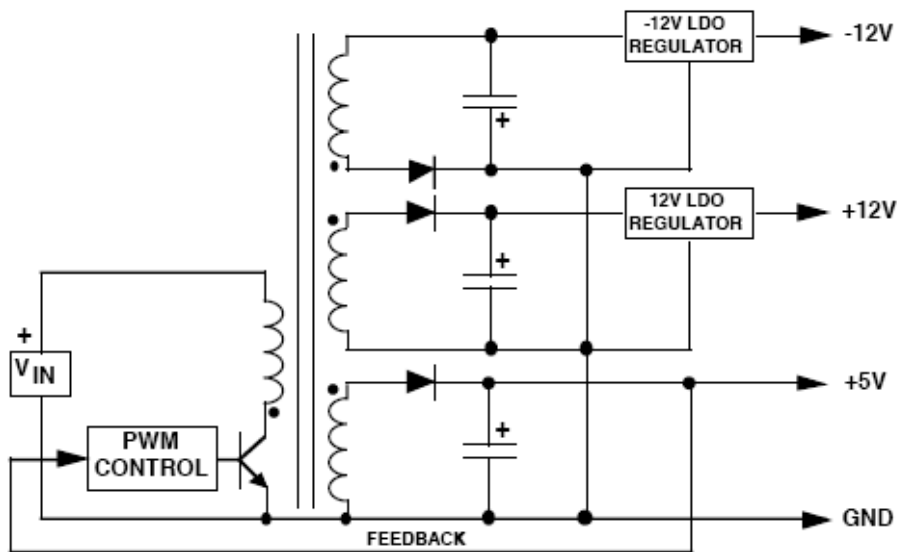
The Push-Pull converter uses two to transistors perform DC-DC conversion.The converter operates by turning on each transistor on alternate cycles (the two transistors are never on at the same time). Transformer secondary current flows at the same time as primary current (when either of the switches is on). For example, when transistor "A" is turned on, the input voltage is forced across the upper primary winding with dot-negative polarity. On the secondary side, a dot-negative voltage will appear across the winding which turns on the bottom diode.This allows current to flow into the inductor to supply both the output capacitor and the load. When transistor "B" is on, the input voltage is forced across the lower primary winding with dot-positive polarity.
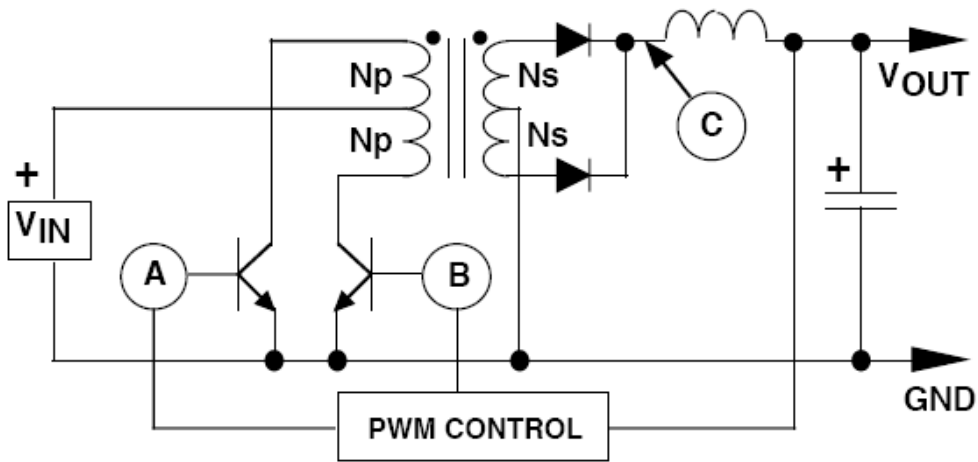
The same voltage polarity on the secondary turns on the top diode, and current flows into the output capacitor and the load. An important characteristic of a Push-Pull converter is that the switch transistors have to be able the stand off more than twice the input voltage: when one transistor is on (and the input voltage is forced across one primary winding) the same magnitude voltage is induced across the other primary winding, but it is "floating" on top of the input voltage. This puts the collector of the turned-off transistor at twice the input voltage with respect to ground. The "double input voltage" rating requirement of the switch transistors means the Push-Pull converter is best suited for lower input voltage applications. It has been widely used in converters operating in 12V and 24V battery-powered systems.
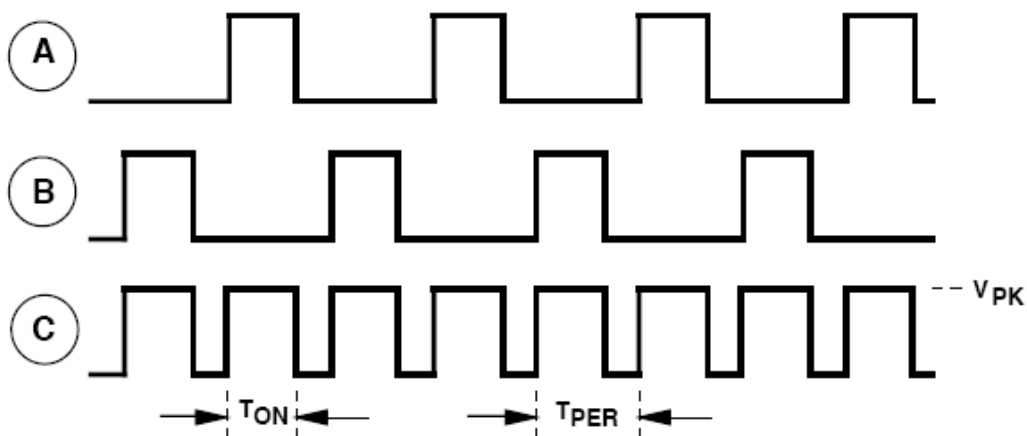
Figure shows a timing diagram which details the relationship of the input and output pulses. It is important to note that frequency of the secondary side voltage pulses is twice the frequency of

operation of the PWM controller driving the two transistors. For example, if the PWM control chip was set up to operate at 50 kHz on the primary

side, the frequency of the secondary pulses would be 100 kHz.

This highlights why the Push-Pull converter is well-suited for low voltage converters.

The voltage forced across each primary winding (which provides the power for conversion) is the full input voltage minus only the saturation voltage of the switch. If MOS-FET power switches are used, the voltage drop across the switches can be made extremely small, resulting in very high utilization of the available input voltage. Another advantage of the Push-Pull converter is that it can also generate multiple output voltages (by adding more secondary windings), some of which may be negative in polarity. This allows a power supply operated from a single battery to provide all of the voltages necessary for system operation.

A disadvantage of Push-Pull converters is that they require very good matching of

the switch transistors to prevent unequal on times, since this will result in saturation

of the transformer core (and failure of the converter).

Output Capacitor ESR effects:
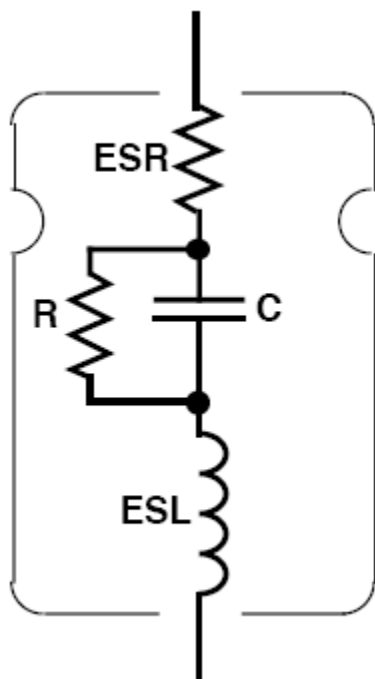
The primary function of the output capacitor in a switching regulator is filtering. As the converter operates, current must flow into and out of the output filter capacitor. The ESR of the output capacitor directly affects the performance of the switching regulator. ESR is specified by the manufacturer on good quality capacitors, but be certain that it is specified at the frequency of intended operation.

General-purpose electrolytes usually only specify ESR at 120 Hz, but capacitors intended for high-frequency switching applications will have the ESR guaranteed at high frequency (like 20 kHz to 100 kHz). Some ESR dependent parameters are: Ripple Voltage: In most cases, the majority of the output ripples voltage results from the ESR of the output capacitor. If the ESR increases (as it will at low operating temperatures) the output ripple voltage will increase accordingly.

Efficiency: As the switching current flows into and out of the capacitor (through the ESR), power is dissipated internally. This "wasted" power reduces overall regulator efficiency, and can also cause the capacitor to fail if the ripple current exceeds the maximum allowable specification for the capacitor.

Loop Stability: The ESR of the output capacitor can affect regulator loop stability. Products such as the LM2575 and LM2577 are compensated for stability assumingthe ESR of the output capacitor will stay within a specified range. Keeping the ESR within the "stable" range is not always simple in designs that must operate over a wide temperature range. The ESR of a typical aluminum electrolytic may increase by 40X as the temperature drops from 25°C to -40°C.

In these cases, an aluminum electrolytic must be paralleled by another type ofcapacitor with a flatter ESR curve (like Tantalum or Film) so that the effective ESR (which is the parallel value of the two ESR's) stays within the allowable range. Note: if operation below -40°C is necessary, aluminum electrolytics are probably not feasible for use.

Bypass Capacitors:

High-frequency bypass capacitors are always recommended on the supply pins of IC devices, but if the devices are used in assemblies near switching converters bypass capacitors are absolutely required. The components which perform the high-speed switching (transistors and rectifiers) generate significant EMI that easily radiates into PC board traces and wire leads. To assure proper circuit operation, all IC supply pins must be bypassed to a clean, low-inductance ground.

Proper Grounding:

The "ground" in a circuit is supposed to be at one potential, but in real life it is not.
When ground currents flow through traces which have non-zero resistance, voltage
differences will result at different points along the ground path. In DC or low-frequency circuits, "ground management" is comparatively simple: the only parameter of critical importance is the DC resistance of a conductor, since that defines the voltage drop across it for a given current. In high-frequency circuits, it is the inductance of a trace or conductor that is much more important.

In switching converters, peak currents flow in high-frequency (> 50 kHz) pulses, which can cause severe problems if trace inductance is high. Much of the "ringing" and "spiking" seen on voltage waveforms in switching converters is the result of high current being switched through parasitic trace (or wire) inductance.Current switching at high frequencies tends to flow near the surface of a conductor (this is called "skin effect"), which means that ground traces must be very wide on a PC board to avoid problems. It is usually best (when possible) to use one side of the PC board as a ground plane. The following diagram shows the poor grounding.
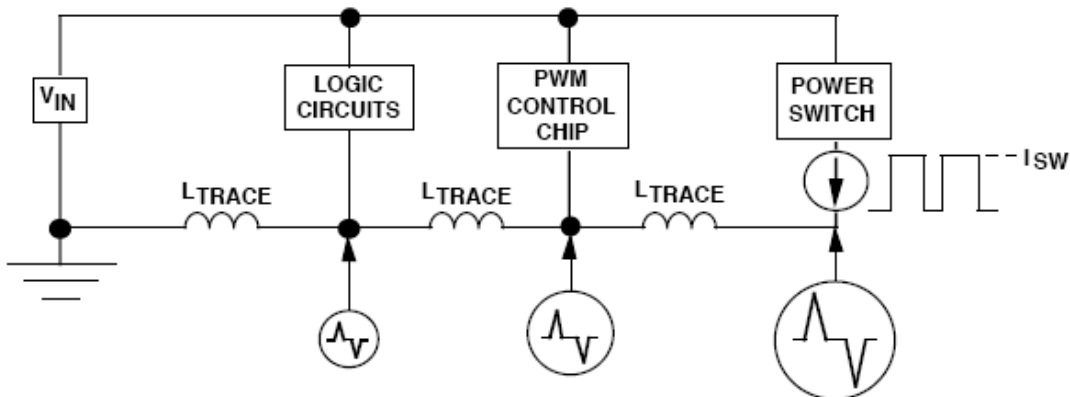
The layout shown has the high-power switch return current passing through a trace that also provides the return for the PWM chip and the logic circuits. The switching current pulses flowing through the trace will cause a voltage spike (positive and negative) to occur as a result of the rising and falling edge of the switch current. This voltage spike follows directly from the $v = L \, (di/dt)$ law of inductance. It is important to note that the magnitude of the spike will be different at all points along the trace, being largest near the power switch. Taking the ground symbol as a point of reference, this shows how all three circuits would be bouncing up and down with respect to ground. More important, they would also be moving with respect to each other.

Mis-operation often occurs when sensitive parts of the circuit "rattle" up and down due to ground switching currents. This can induce noise into the reference used to set the output voltage, resulting in excessive output ripple. Very often, regulators that suffer from ground noise problems appear to be unstable, and break into oscillations as the load current is increased (which increases ground currents). The figure shows good grounding.
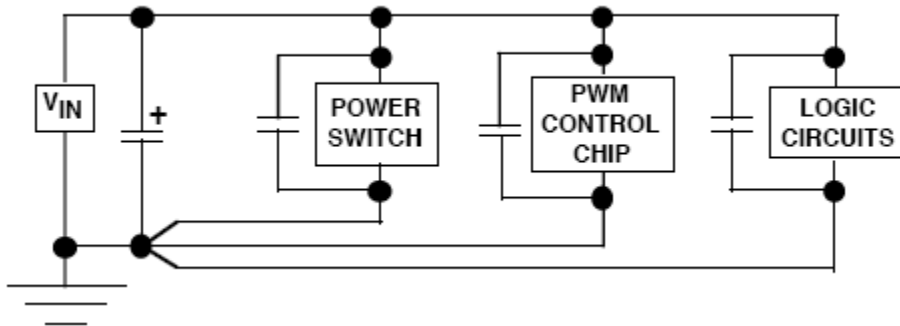
A big improvement is made by using single-point grounding. A good high-frequency electrolytic capacitor (like solid Tantalum) is used near the input voltage source to provide a good ground point. All of the individual circuit elements are returned to this point using separate ground traces.

This prevents high current ground pulses from bouncing the logic circuits up and down.
Another important improvement is that the power switch (which has the highest ground pin current) is located as close as possible to the input capacitor. This minimizes the trace inductance along its ground path. It should also be pointed out that all of the individual circuit blocks have

"local" bypass capacitors tied directly across them. The purpose of this capacitor is RF bypass, so it must be a ceramic or film capacitor (or both).

A good value for bypassing logic devices would be 0.01 µF ceramic capacitor(s), distributed as required.

If the circuit to be bypassed generates large current pulses (like the power switch), more capacitance is required. A good choice would be an aluminum electrolytic bypassed with a film and ceramic capacitor. Exact size depends on peak current, but the more capacitance used, the better the result. Transformer/Inductor Cores and Radiated Noise The type of core used in an inductor or transformer directly affects its cost, size, and radiated noise characteristics. Electrical noise radiated by a transformer is extremely important, as it may require shielding to prevent erratic operation of sensitive circuits located near the switching regulator. The most commonly used core types will be presented, listing the advantages and disadvantages of each.

Measuring Output Ripple Voltage:

The ripple appearing on the output of the switching regulator can be important to the circuits under power. Getting an accurate measurement of the output ripple voltage is not always simple. If the output voltage waveform is measured using an oscilloscope, an accurate result can only be obtained using a differential measurement method. The differential measurement shown uses the second channel of the oscilloscope to "cancel out" the signal that is common to both channels (by inverting the B channel signal and adding it to the A channel).

The reason this method must be used is because the fast-switching components in a switching regulator generate voltage spikes that have significant energy at very high frequencies. These signals can be picked up very easily by "antennas" as small as the 3" ground lead on the scope probe. Assuming the probes are reasonably well matched, the B channel probe will pick up the same radiated signal as the A channel probe, which allows this "common-mode" signal to be eliminated by adding the inverted channel B signal to channel A. It is often necessary to measure the RMS output ripple voltage, and this is usually done with some type of digital voltmeter. If the reading obtained is to be meaningful, the following must be considered:

Measuring Regulator Efficiency of DC-DC Converters:

The efficiency of a switching regulator is defined as:

$$\eta = \text{PLOAD} \ / \ \text{PTOTAL}$$

In determining converter efficiency, the first thing that must be measured is the total consumed power (PTOTAL). Assuming a DC input voltage, PTOTAL is defined as the total power drawn from the source, which is equal to:

$$\text{PTOTAL} \ = \ \text{VIN} \ \text{X} \ \text{IIN (AVE)}$$

It must be noted that the input current value used in the calculation must be the average value of the waveform (the input current will not be DC or sinusoidal). Because the total power dissipated must be constant from input to output, PTOTAL is also equal to the load power plus the internal regulator power losses:

$$\text{PTOTAL} \ = \ \text{PLOAD} \ + \ \text{PLOSSES}$$

Measuring (or calculating) the power to the load is very simple, since the output voltage and current are both DC. The load power is found by:

$$\text{PLOAD} = \text{VOUT} \ \text{X} \ \text{ILOAD}$$

Measuring the input power drawn from the source is not simple. Although the input voltage to the regulator is DC, the current drawn at the input of a switching regulator is not. If a typical "clip-on" current meter is used to measure the input current, the taken data will be essentially meaningless. The average input current to the regulator can be measured with reasonable accuracy by using a wide-bandwidth current probe connected to an oscilloscope.

The average value of input current can be closely estimated by drawing a horizontal line that divides the waveform in such a way that the area of the figure above the

line will equal the "missing" area below the line. In this way, the "average" current shown is equivalent to the value of DC current that would produce the same input power.

If more exact measurements are needed, it is possible to force the current in the line going to the input of the DC-DC converter to be DC by using an L-C filter between the power source and the input of the converter If the L-C filter components are adequate, the current coming from the output of the DC power supply will be DC current (with no high-frequency switching component) which means it can be accurately measured with a cheap clip-on ammeter and digital volt meter.

It is essential that a large, low-ESR capacitor be placed at CIN to support the input of the switching converter. The L-C filter that the converter sees looking back into the source presents a high impedance for switching current, which means CIN is necessary to provide the switching current required at the input of the converter.

Measuring Regulator Efficiency of Off-Line Converters:

Off-Line converters are powered directly from the AC line, by using a bridge rectifier and capacitive filter to generate an unregulated DC voltage for conversion. Measuring the total power drawn from the AC source is fairly difficult because of the power factor.   If both the voltage and current are sinusoidal, power factor is defined as the cosine of the phase angle between the voltage and current waveforms.

The capacitive-input filter in an off-line converter causes the input current to be very non-sinusoidal. The current flows in narrow, high-amplitude pulses (called Haversine pulses) which requires that the power factor be re-defined in such cases. For capacitive-input filter converters, power factor is defined as:
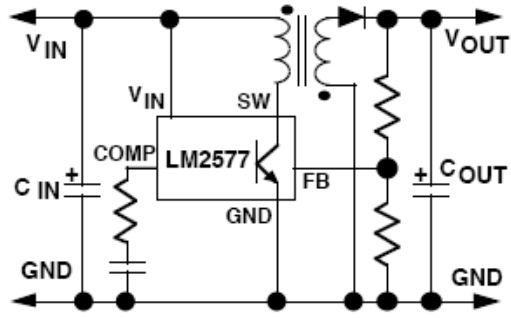
$$P.F. \;=\; PREAL \;/\; PAPPARENT$$

LM 2577: An Example of a Complete FlyBack/ Boost Regulator IC
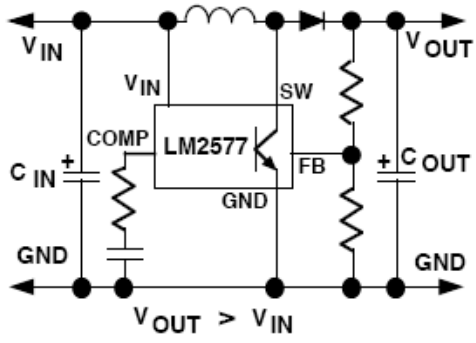
BOOST REGULATOR

FLYBACK REGULATOR

LINEAR REGULATORS

- All electronic circuits need a dc power supply for their operation. To obtain this dc voltage from 230 V ac mains supply, we need to use rectifier.
- Therefore the filters are used to obtain a "steady" dc voltage from the pulsating one.
- The filtered dc voltage is then applied to a regulator which will try to keep the dc output voltage constant in the event of voltage fluctuations or load variation.
- We know the combination of rectifier & filter can produce a dc voltage. But the problem with this type of dc power supply is that its output voltage will not remain constant in the event of fluctuations in an ac input or changes in the load current(I_L).
- The output of unregulated power supply is connected at the input of voltage regulator circuit.
- The voltage regulator is a specially designed circuit to keep the output voltage constant.
- It does not remain exactly constant. It changes slightly due to changes in certain parameters.

Factors affecting the output voltage:

    i) I_L (Load Current)

    ii) V_{IN} (Input Voltage)

    iii)   T (Temperature)

IC Voltage Regulators:

       They are basically series regulators with all the basic blocks present inside the IC. Therefore it is easier to use IC voltage regulator instead of discrete voltage regulators.

Important features of IC Regulators:

1. Programmable output
2. Facility to boost the voltage/current
3. Internally provided short circuit current limiting

4. Thermal shutdown

5. Floating operation to facilitate higher voltage output

Classifications of IC voltage regulators:

IC Voltage Regulator

Fixed Volt Reg.   Adjustable O/P Volt Reg   Switching Reg
Positive/negative
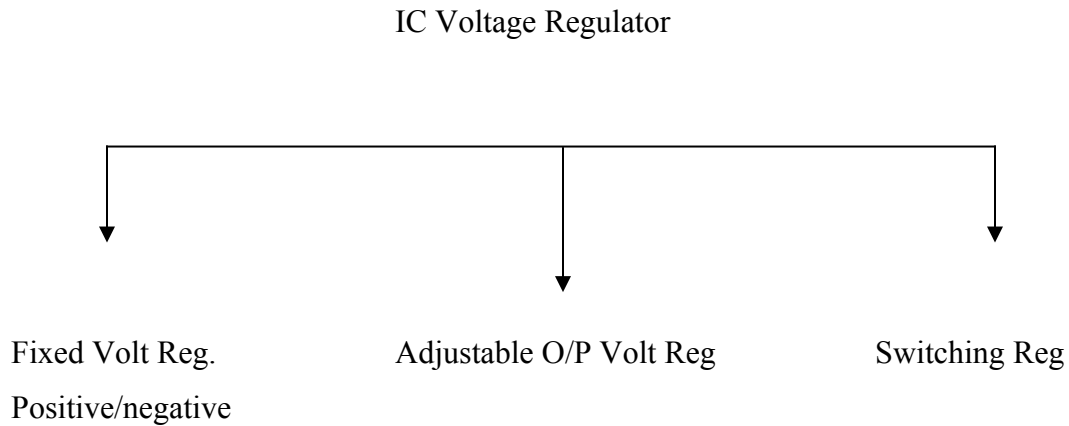
- Fixed & Adjustable output Voltage Regulators are known as Linear Regulator.
- A series pass transistor is used and it operates always in its active region.

Switching Regulator:

1. Series Pass Transistor acts as a switch.

2. The amount of power dissipation in it decreases considerably.

3. Power saving result is higher efficiency compared to that of linear.

Adjustable Voltage Regulator:

Advantages of Adjustable Voltage Regulator over fixed voltage regulator are,

1. Adjustable output voltage from 1.2v to 57 v

2. Output current 0.10 to 1.5 A

3. Better load & line regulation

4. Improved overload protection

5. Improved reliability under the 100% thermal overloading

Adjustable Positive Voltage Regulator (LM317):

Unregulated supply Vin

Load
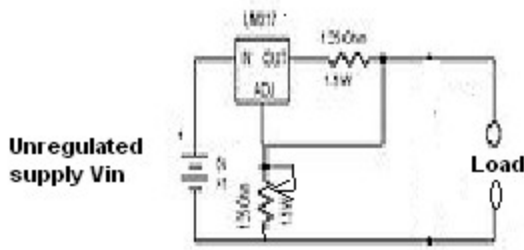
- LM317 series adjustable 3 terminal positive voltage regulator, the three terminals are Vin, Vout & adjustment (ADJ).
- LM317 requires only 2 external resistors to set the output voltage.
- LM317 produces a voltage of 1.25v between its output & adjustment terminals. This voltage is called as Vref.
- Vref (Reference Voltage) is a constant, hence current I1 flows through R1 will also be constant. Because resistor R1 sets current I1. It is called "current set" or "program resistor".
- Resistor R2 is called as "Output set" resistors, hence current through this resistor is the sum of I1 & Iadj
- LM317 is designed in such as that Iadj is very small & constant with changes in line voltage & load current.
- The output voltage Vo is, $V_o = R1 I1 + (I1 + Iadj) R2$ ------------- (1)

        Where $I1 = Vref/R1$

        $V_o = (Vref/R1)R1 + Vref/R1 + Iadj\ R2$

          $= Vref + (Vref/R1)R2 + Iadj\ R2$

        $V_o = Vref\ [1 + R2/R1] + Iadj\ R2$ ------------- (2)

R1 = Current (I1) set resistor

R2 = output (Vo) set resistor

Vref = 1.25v which is a constant voltage between output and ADJ terminals.

- Current Iadj is very small. Therefore the second term in (2) can be neglected.
- Thus the final expression for the output voltage is given by

$$Vo= 1.25v[1 + R2/R1] \qquad \text{-------------} \quad (3)$$

Eqn (3) indicates that we can vary the output voltage by varying the resistance R2.
The value of R1 is normally kept constant at 240 ohms for all practical applications.

Practical Regulator using LM317:
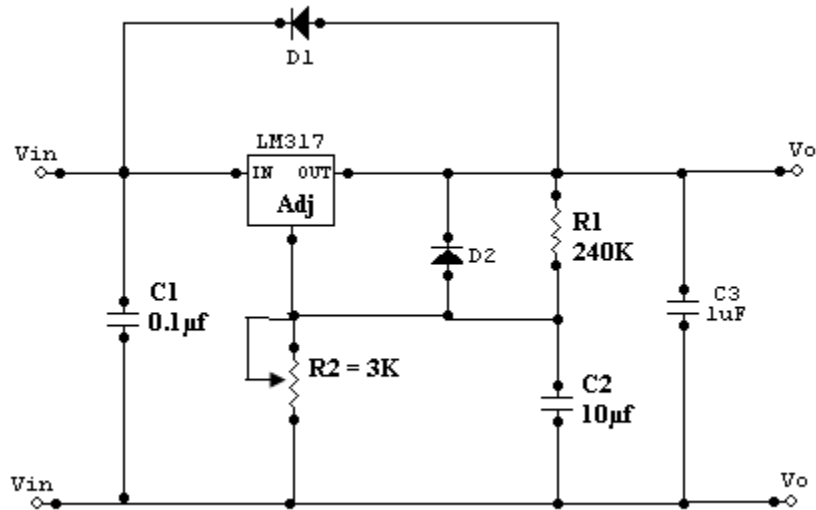
- If LM317 is far away from the input power supply, then 0.1μf disc type or 1μf tantalum capacitor should be used at the input of LM317.
- The output capacitor Co is optional. Co should be in the range of 1 to 1000μf.

- The adjustment terminal is bypassed with a capacitor C2 this will improve the ripple rejection ratio as high as 80 dB is obtainable at any output level.
- When the filter capacitor is used, it is necessary to use the protective diodes.
- These diodes do not allow the capacitor C2 to discharge through the low current point of the regulator.
- These diodes are required only for high output voltages (above 25v) & for higher values of output capacitance 25μf and above.

IC 723 – GENERAL PURPOSE REGULATOR

Disadvantages of fixed voltage regulator:

1. Do not have the shot circuit protection
2. Output voltage is not adjustable

These limitations can be overcomes in IC723.

Features of IC723:

1. Unregulated dc supply voltage at the input between 9.5V & 40V
2. Adjustable regulated output voltage between 2 to 3V.
3. Maximum load current of 150 mA (I_{Lmax} = 150mA).
4. With the additional transistor used, I_{Lmax} upto 10A is obtainable.
5. Positive or Negative supply operation
6. Internal Power dissipation of 800mW.
7. Built in short circuit protection.
8. Very low temperature drift.
9. High ripple rejection.

The simplified functional block diagram can be divided in to 4 blocks.

1. Reference generating block

2. Error Amplifier

3. Series Pass transistor

4. Circuitry to limit the current

1. Reference Generating block:

      The temperature compensated Zener diode, constant current source & voltage reference amplifier together from the reference generating block. The Zener diode is used to generate a fixed reference voltage internally. Constant current source will make the Zener diode to operate at affixed point & it is applied to the Non – inverting terminal of error amplifier. The Unregulated input voltage ±Vcc is applied to the voltage reference amplifier as well as error amplifier.

2. Error Amplifier:

      Error amplifier is a high gain differential amplifier with 2 input (inverting & Non-inverting). The Non-inverting terminal is connected to the internally generated reference voltage. The Inverting terminal is connected to the full regulated output voltage.
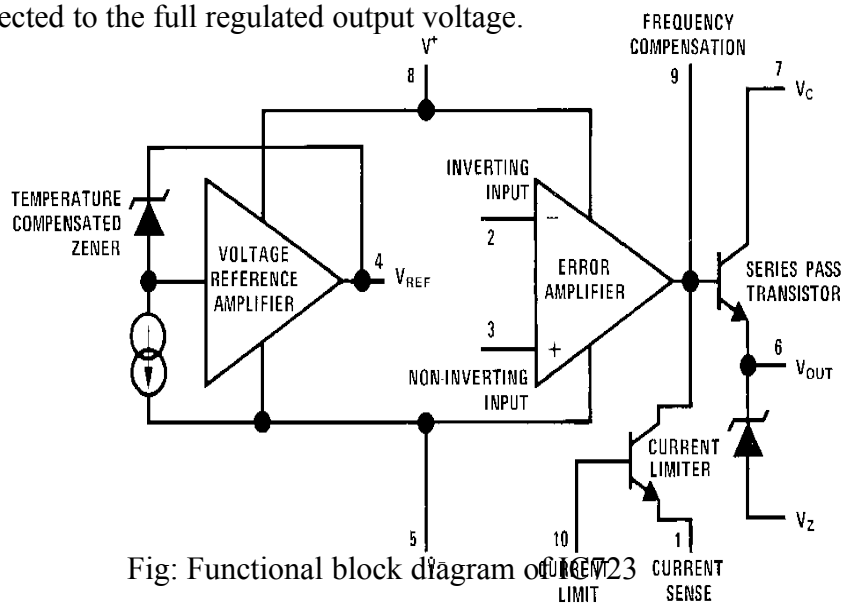
Fig: Functional block diagram of IC 723

```
NC        1        14   NC
Current limit   2        13   Frequency compensation
Current sense   3        12   +Vcc
Inverting Input  4   IC 723  11   Vc
Non-Inverting Input 5      10   Vo
Vref       6        9    Vz
-Vcc       7        8    NC
```

Fig : Pin diagram of IC723

3. Series Pass Transistor:

       Q1 is the internal series pass transistor which is driven by
the error amplifier. This transistor actually acts as a variable resistor
& regulates the output voltage. The collector of transistor Q1 is
connected to the Un-regulated power supply. The maximum collector
voltage of Q1 is limited to 36Volts. The maximum current which can
be supplied by Q1 is 150mA.

4. Circuitry to limit the current:

       The internal transistor Q2 is used for current sensing & limiting. Q2 is
normally OFF transistor. It turns ON when the I_L exceeds a predetermined limit.

- Low voltage , Low current is capable of supplying load voltage which is equal to or
  between 2 to 7Volts.

$$V_{load} = 2 \text{ to } 7V$$

$$I_{load} = 150mA$$

IC723 as a LOW voltage LOW current :
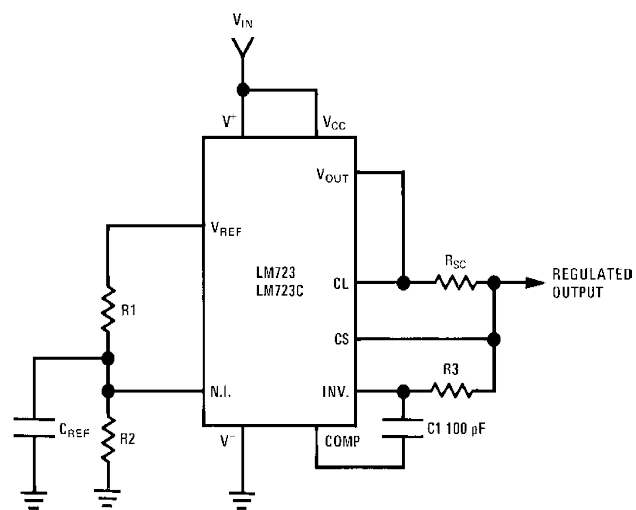
Fig: Typical circuit connection diagram

- R1 & R2 from a potential divider between Vref & Gnd.
- The Voltage across R2 is connected to the Non – inverting terminal of the regulator IC

$$Vnon\text{-}inv = \frac{R2}{R1 + R2} \; Vref$$

- Gain of the internal error amplifier is large

$$Vnon\text{-}inv = Vin$$

- Therefore the Vo is connected to the Inverting terminal through R3 & R_{SC} must also be equal to $V_{non\text{-}inv}$

$$Vo = \; Vnon\text{-}inv = \frac{R2}{R1 + R2} \; Vref$$

R1 & R2 can be in the range of 1 KΩ to 10KΩ & value of R3 is given by

$$R3 = R1 \| R2 = \frac{R1R2}{R + R2}$$

- Rsc (current sensing resistor) is connected between Cs & C_L. The voltage drop across Rsc is proportional to the I_L.
- This resistor supplies the output voltage in the range of 2 to 7 volts, but the load current can be higher than 150mA.
- The current sourcing capacity is increased by including a transistor Q in the circuit.

- The output voltage , $Vo_{V_{IN}} = \frac{R2}{R1 + R2} \; Vref$

IC723 as a HIGH voltage LOW Current:
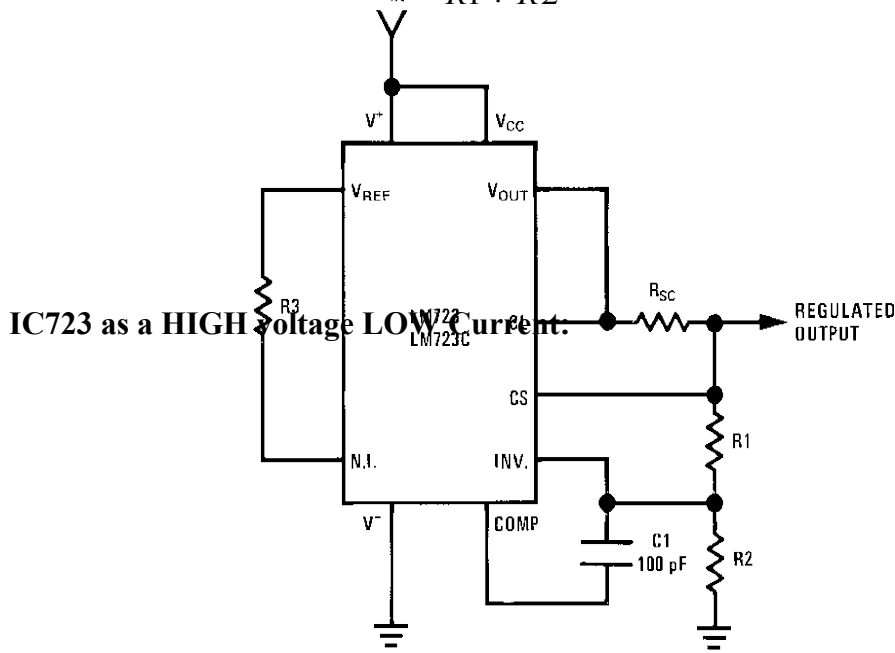
Fig: Typical circuit connection diagram

- This circuit is capable of supplying a regulated output voltage between the range of 7 to 37 volts with a maximum load current of 150 mA.
- The Non – inverting terminal is now connected to Vref through resistance R3.
- The value of R1 & R2 are adjusted in order to get a voltage of Vref at the inverting terminal at the desired output.

$$\text{Vin} = \text{Vref} = \frac{R2}{R1 + R2} \text{ Vo}$$

$$\text{Vo} = \frac{R1 + R2}{R2} \text{ Vref}$$

Or

$$\text{Vo} = [1 + \frac{R1}{R2}] \text{ Vref}$$

- Rsc is connected between C_L & Cs terminals as before & it provides the short circuit current limiting

$$Rsc = \frac{0.6}{ILimit}$$

- The value of resistors R3 is given by ,

$$R3 = R1 \; ll \; R2 = \frac{R1R2}{R + R2}$$

IC723 as a HIGH voltage HIGH Current:
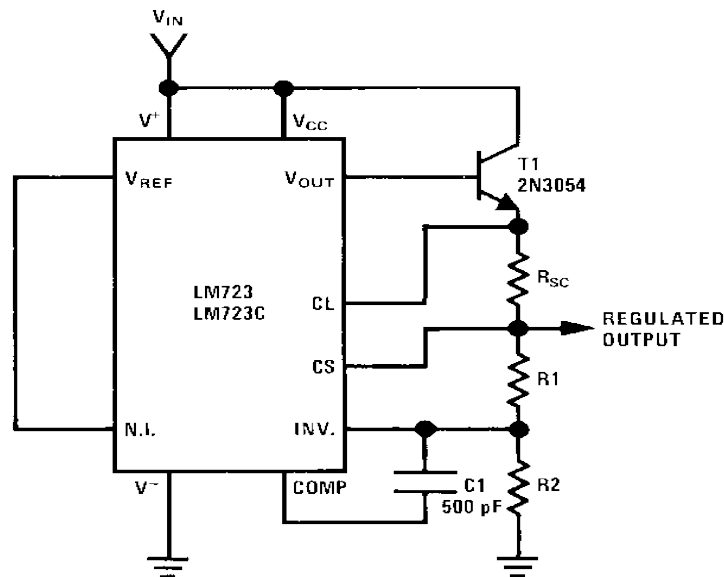
Fig: Typical circuit connection diagram

- An external transistor Q is added in the circuit for high voltage low current regulator to improve its current sourcing capacity.
- For this circuit the output voltage varies between 7 & 37V.
- Transistor Q increase the current sourcing capacity thus $I_{L(MAX)}$ ia greater than 150mA.

- The output voltage Vo is given by ,

$$V_o = \left[\frac{R_1 + R_2}{R_2} \right] V_{ref}$$

- The value of Rsc is given by $R_{sc} = \dfrac{0.6}{I_{Limit}}$

SWITCHING REGULATOR:

An example of general purpose regulator is Motorola's MC1723. It can be used in many different ways, for example, as a fixed positive or negative output voltage regulator, variable regulator or switching regulator because of its flexibility.

To minimize the power dissipation during switching, the external transistor used must be a switching power transistor.

To improve the efficiency of a regulator, the series pass transistor is used as a switch rather than as a variable resistor as in the linear mode.

- A regulator constructed to operate in this manner is called a series switching regulator. In such regulators the series pass transistor is switched between cut off & saturation at a high frequency which produces a pulse width modulated (PWM) square wave output.
- This output is filtered through a low pass LC filter to produce an average dc output voltage.
- Thus the output voltage is proportional to the pulse width and frequency.

- The efficiency of a series switching regulator is independent of the input & output differential & can approach 95%
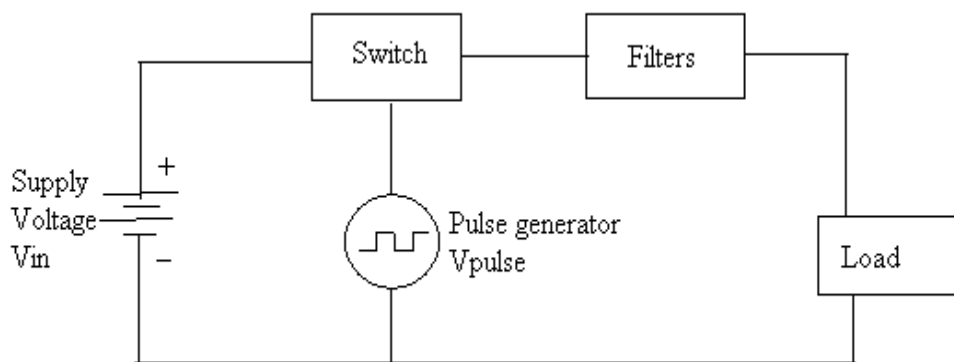
Fig : Basic Switching regulator

A basic switching regulator consists of 4 major components,

1. Voltage source Vin
2. Switch S1
3. Pulse generator Vpulse
4. Filter F1

1. Voltage Source Vin:

It may be any dc supply – a battery or an unregulated or a regulated voltage. The voltage source must satisfy the following requirements.

- It must supply the required output power & the losses associated with the switching regulator.
- It must be large enough to supply sufficient dynamic range for line & load regulations.
- It must be sufficiently high to meet the minimum requirement of the regulator system to be designed.
- It may be required to store energy for a specified amount of time during power failures.

2. Switch S1:

It is typically a transistor or thyristor connected as a power switch & is operated in the saturated mode. The pulse generator output alternately turns the switch ON & OFF

3. Pulse generator Vpulse:

It provides an asymmetrical square wave varying in either frequency or pulse width called frequency modulation or pulse width modulation respectively. The most effective frequency range for the pulse generator for optimum efficiency 20 KHz. This frequency is inaudible to the human ear & also well within the switching speeds of most inexpensive transistors & diodes.

- The duty cucly of the pulse wave form determines the relationship between the input & output voltages. The duty cycle is the ratio of the on time ton, to the period T of the pulse waveform.

$$\text{Duty cycle} = \frac{ton}{ton + toff}$$

$$= \frac{ton}{T} = ton \ f.$$

Where   ton = On-time of the pulse waveform

toff=off-time of the pulse wave form

T = time period = ton + toff

= 1/frequency or

T = 1/f

- Typical operating frequencies of switching regulator range from 10 to 50khz.
- Lower operating frequency improve efficiency & reduce electrical noise, but require large filter components (inductors & capacitors).

4. Filter F1:

It converts the pulse waveform from the output of the switch into a dc voltage. Since this switching mechanism allows a conversion similar to transformers, the switching regulator is often referred to as a dc transformer.

The output voltage Vo of the switching regulator is a function of duty cycle & the input voltage Vin.

Vo is expressed as follows,

$$Vo = \frac{ton}{T} \; Vin$$

- This equation indicates that, if time period T is constant, Vo is directly proportional to the ON-time, ton for a given value of Vin. This method of changing the output voltage by varying ton is referred to as a pulse width modulation.
- Similarly, if ton is held constant, the output voltage Vo is inversely proportional to the period T or directly proportional to the frequency of the pulse waveform. This method of varying the output voltage is referred to as frequency modulation (FM).
- Switching regulator can operate in any of 3 modes

i)   Step – Down

ii)   Step – Up

iii)   Polarity inverting

MONOLITHIC SWITCHING REGULATOR [µA78S40]:

The µA78S40 consists of a temperature compensated voltage reference, duty cycle controllable oscillator with an active current limit circuit, a high gain comparator, a high- current, high voltage output switch, a power switching diode & an uncommitted op-amp.

Important features of the µA78S40 switching regulators are:

- Step up, down & Inverting operation
- Operation from 2.5 to 40V input
- 80dB line & load regulations
- Output adjustable from 1.3 to 40V
- Peak current to 1.5A without external resistors
- Variable frequency, variable duty cycle device

The internal switching frequency is set by the timing capacitor C_T, connected between pin12 & ground pin 11. the initial duty cycle is 6:1. The switching frequency & duty cycle can be modified by the current limit circuitry, I_{PK}sense, pin14, 7 the comparator, pin9 & 10.

Comparator:

The comparator modifies the OFF time of the output switch transistor Q1 & Q2. In the step – up & step down modes, the non-inverting input(pin9) of the comparator is connected to the

voltage reference of 1.3V (pin8) & the inverting input (pin10) is connected to the output terminal via the voltage divider network.
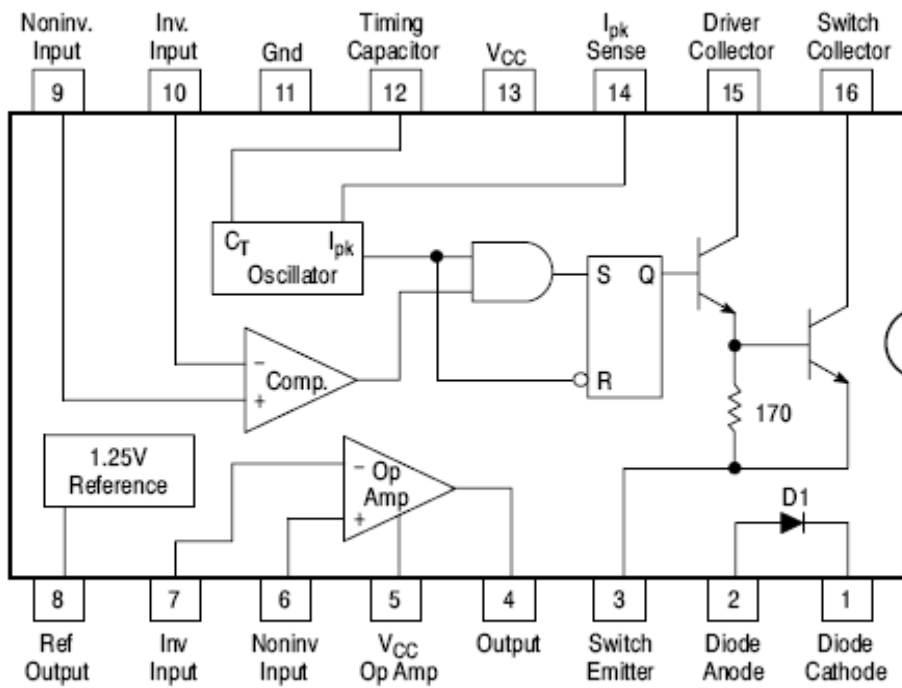
Fig: Functional block diagram of μA78S40
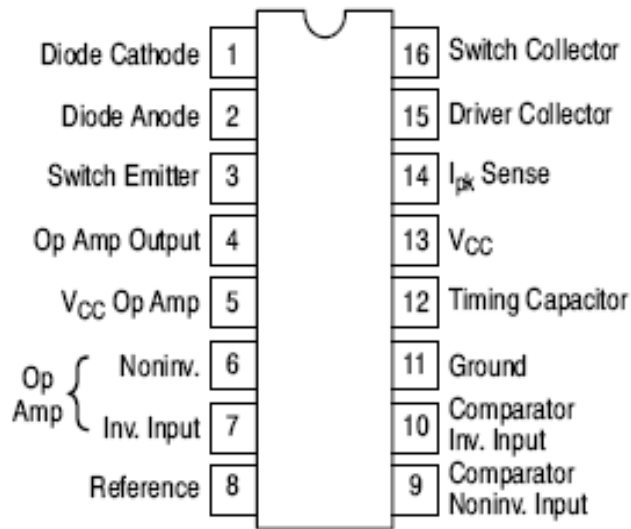
- In the Inverting mode ➜ the non – inverting input is connected to both the voltage reference & the output terminal through 2 resistors & the inverting terminal is connected to ground.
- When the output voltage is correct, the comparator output is in high state & has no effect on the circuit operation.
- However, if the output is too high & the voltage at the inverting terminal is higher than that at the non-inverting terminal , then the comparator output goes low.
- In the LOW state   the comparator inhibits the turn on of the output switching transistors. This means that, as long as the comparator output is low, the system is in off time.
- As the output current rises or the output voltage falls, the off time of the system decreases.
- Consequently, as the output current nears its maximum Io_{MAX}, the off time approaches its minimum value.

In all 3 modes (Step down, step up, Inverting), the current limit circuit is completed by connecting a sense resistor Rsc, between I_{PK} sense & Vcc.

- The current limit circuit is activated when a 330mV potential appears across Rsc.
- Rsc is selected such that 330mV appears across it when the desired peak current I_{PK}, flows through it.
- When the peak current is reached, the current limit circuit is turned on.
- The forward voltage drop, V_D, across the internal power diode is used to determine the value of inductor L off time & efficiency of the switching regulator.
- Another important quantity used in the design of a switching regulator is the saturation voltage Vs

  ✓ In the step down mode an "output saturation volt" is 1.1V typical, $1.3V_{MAX}$.
  ✓ In the step up mode an "Output saturation volt" is 0.45V typical, 0.7 maximum.

$$Rsc = \frac{330mV}{DesiredPeakCurrent}$$

✓ The desired peak current value is reached, the current limiting circuit turns ON & immediately terminates the ON time & starts OFF time.

- As we increase I_L (load current), Vout will decreased, to compensate for this, the ON time of the output is increased automatically.

- If the I_L decreased then Vout increased, to compensate for this, the OFF time of the output is increased automatically.

(i) Step – Down Switching Regulator:

- C_T is the timing capacitor which decides the switching frequency.
- Rsc is the current sensing resistance. Its value is given by

$$Rsc = \frac{330mV}{DesiredPeakCurrent}$$

- The Non-inverting terminal of the internal op-amp(pin9) is connected to the 1.3V reference (pin8).
- Resistances R1 & R2 from a potential divider, across the output voltage Vo. Their value should be such that the potential at the inverting input of the op-amp should be equal to 1.3V ref when Vo is at its desired level.

- $V_{(-)} = 1.3V = \dfrac{R2}{R1 + R2} \ Vo$

The output capacitance Co is used fro reducing the ripple contents in the output voltage. It acts as a filter along with the inductor L.

- The inductor L is a part of filter connected on the output side, to reduce the ripple percentage.

- The 0.1μF capacitor connected between pin8 & ground bypasses any noise voltage coupled to the reference (pin8).
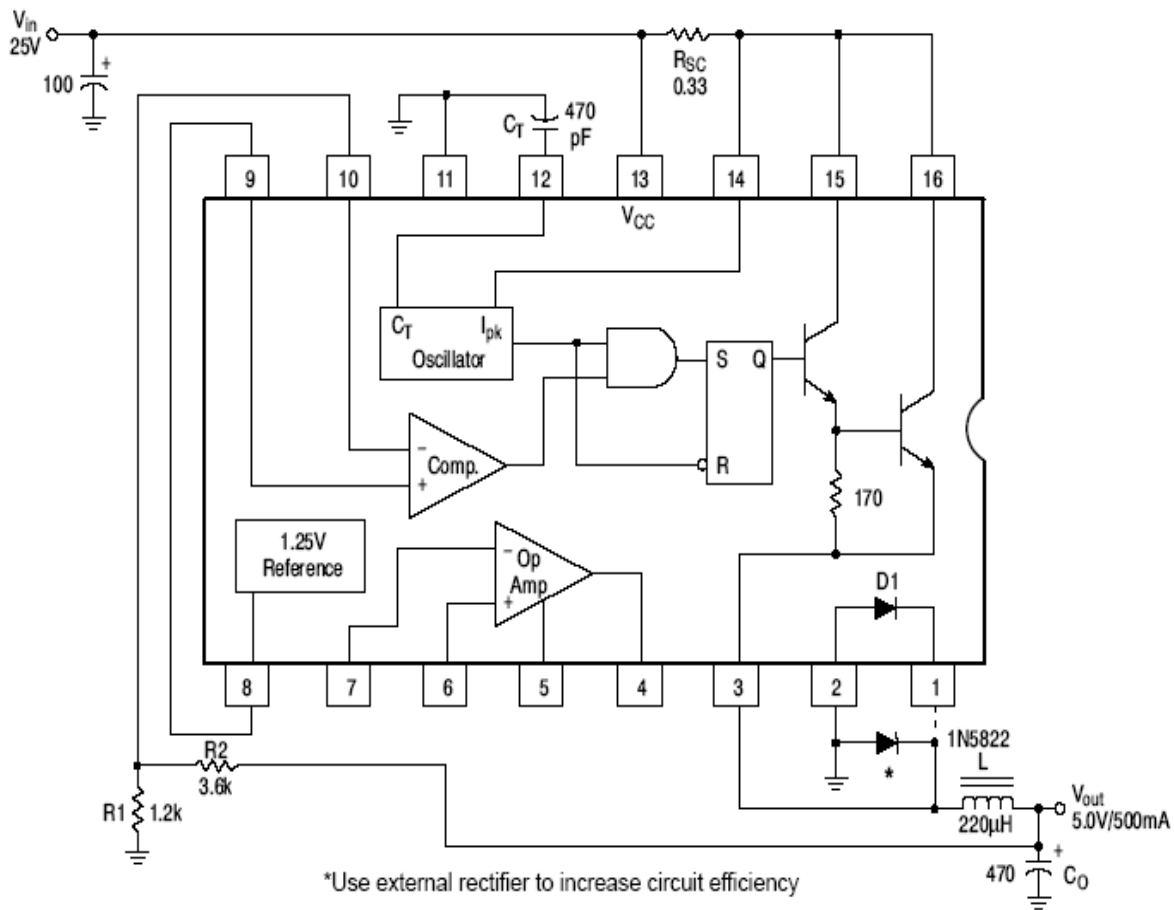
Figure 6. Step–Down Converter

(ii)   Step – Up Switching Regulator:

- Note that inductor is connected between the collectors of Q1 & Q2.
- When Q1 is ON, the output is shorted & the collector current of Q1 flows through L.
- The diode D1 is reverse biased & Co supplies the load current.
- The inductor stores the energy. When the Q1 is turned OFF, there is a self induced emf that appears across the inductor with polarities.
- The output voltage is given by,

$$Vo = Vin + V_L$$

- Hence it will be always higher than Vin & step up operation is achieved.
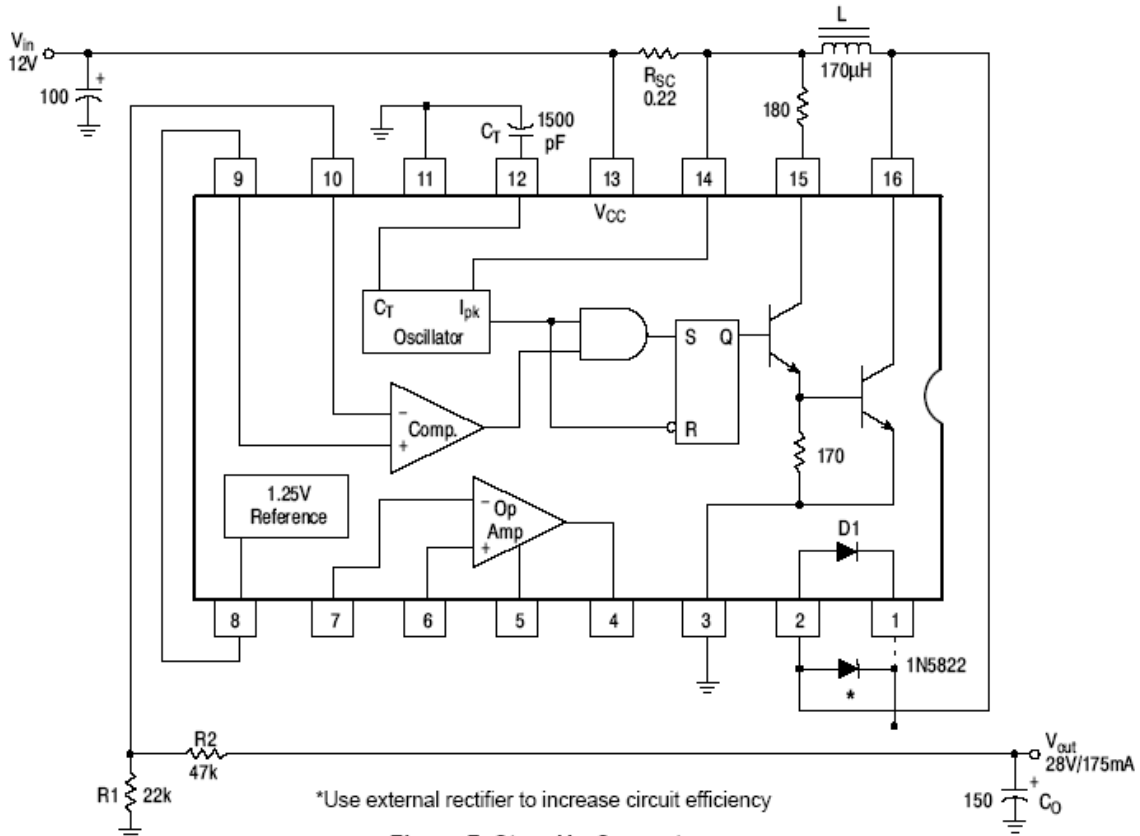
Figure 7. Step–Up Converter
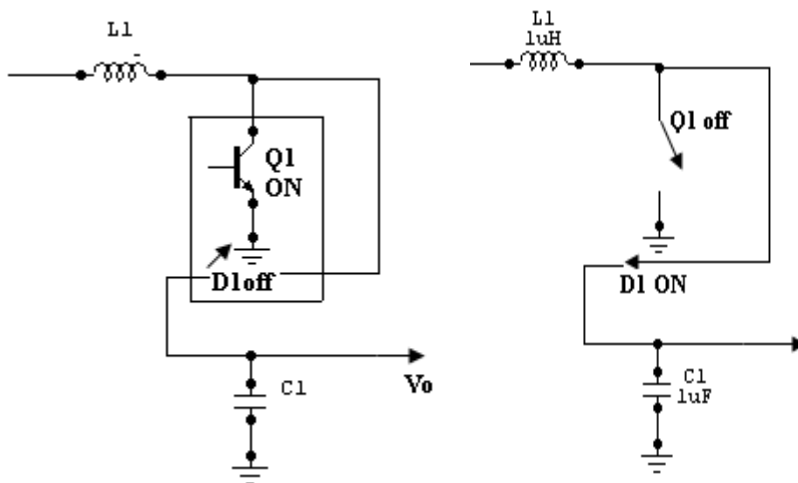
With Q1 ON   with Q1 oFF

(iii)   Inverting Switching Regulator:

Inverting switching regulator converts a positive input voltage into a negative output voltage which is higher in magnitude.
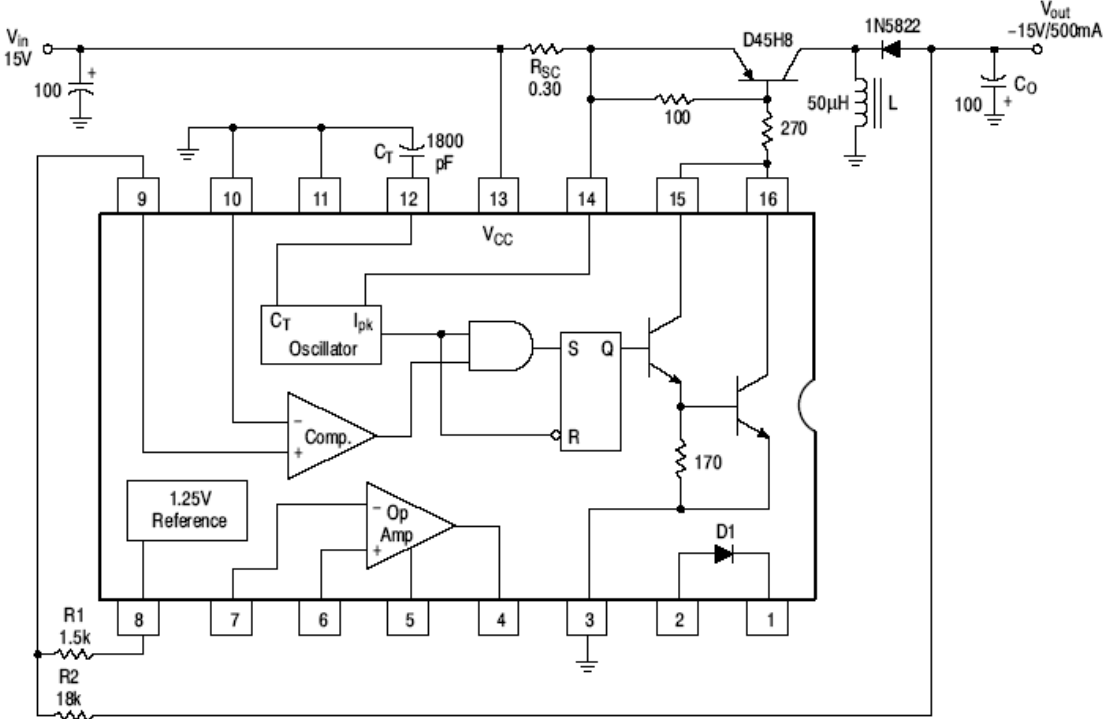
THE SWITCHED CAPACITOR FILTER

Basic Representation:
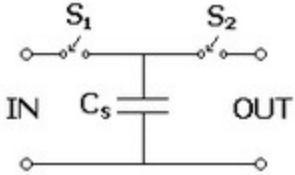
Switched-capacitor resistor

The simplest switched capacitor (SC) circuit is the switched capacitor resistor, made of one capacitor C and two switches S_1 and S_2 which connect the capacitor with a given frequency alternately to the input and output of the SC. Each switching cycle transfers a charge q from the input to the output at the switching frequency f. Recall that the charge q on a capacitor C with a voltage V between the plates is given by:

$$q = CV$$

where V is the voltage across the capacitor. Therefore, when S_1 is closed while S_2 is open, the charge transferred from the source to C_S is:

$$q_{IN} = C_S V_{IN}$$

and when S_2 is closed while S_1 is open, the charge transferred from C_S to the load is:

$$q_{OUT} = C_S V_{OUT}$$

Thus, the charge transferred in each cycle is:

$$q = q_{OUT} - q_{IN} = C_S(V_{OUT} - V_{IN})$$

Since a charge q is transferred at a rate f, the rate of transfer of charge per unit time is:

$$I = qf$$

Note that we use I, the symbol for electric current, for this quantity. This is to demonstrate that a continuous transfer of charge from one node to another is equivalent to a current. Substituting for q in the above, we have:

$$I = C_S(V_{OUT} - V_{IN})f$$

Let us define V, the voltage across the SC from input to output, thus:

$$V = V_{OUT} - V_{IN}$$

We now have a relationship between I and V, which we can rearrange to give an equivalent resistance R:

$$R = \frac{V}{I} = \frac{1}{C_s f}$$

Thus, the SC behaves like a resistor whose value depends on C_S and f.

The SC resistor is used as a replacement for simple resistors in integrated circuits because it is easier to fabricate reliably with a wide range of values. It also has the benefit that its value can be adjusted by changing the switching frequency. See also: operational amplifier applications.

This same circuit can be used in discrete time systems (such as analog to digital converters) as a track and hold circuit. During the appropriate clock phase, the capacitor samples the analog voltage through switch one and in the second phase presents this held sampled value to an electronic circuit for processing.

Switched Capacitor Circuits :

In the last decade or so manyactive filters with resistors and capacitors have been replaced with a special kind of filter called a switched capacitor filter. The switched capacitor filter allows for very sophisticated, accurate, and tuneable analog circuits to be manufactured without using resistors. This is useful for several reasons. Chief among these is that resistors are hard to build on integrated circuits (they take up a lot of room), and the circuits can be made to depend on ratios of capacitor values (which can be set accurately), and not absolute values (which vary between manufacturing runs).

The Switched Capacitor Resistor:

To understand how switched capacitor circuits work, consider the circuit shown with a capacitor connected to two switches and two different voltages.
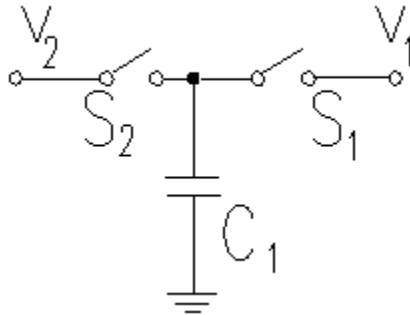
If S_2 closes with S_1 open, then S_1 closes with switch S_2 open, a charge (q is transferred from v_2 to v_1 with

$$\Delta q = C_1(v_2 - v_1)$$

If this switching process is repeated N times in a time (t, the amount of charge transferred per unit time is given by

$$\frac{\Delta q}{\Delta t} = C_1(v_2 - v_1)\frac{N}{\Delta t}$$

Recognizing that the left hand side represents charge per unit time, or current, and the the number of cycles per unit time is the switching frequency (or clock frequency, f_{CLK}) we can rewrite the equation as

$$i = C_1(v_2 - v_1)f_{CLK}$$

Rearranging we get

$$\frac{(v_2 - v_1)}{i} = \frac{1}{C_1 f_{CLK}} = R$$

which states that the switched capacitor is equivalent to a resistor. The value of this resistor decreases with increasing switching frequency or increasing capacitance, as either will increase the amount of charge transfered from v_2 to v_1 in a given time.

The Switched Capacitor Integrator:

Now consider the integrator circuit. You have shown (in a previous lab) that the input-output relationship for this circuit is given by (neglecting initial conditions):

$$v_o(t) = -\frac{1}{RC_2} \int v_i(t) dt = -\omega' \int v_i(t) dt$$

We can also write this with the "s" notation (assuming a sinusoidal input, Ae^{st}, $s=j\omega$)

$$V_o(s) = -\frac{\omega'}{s}$$

If you replaced the input resistor with a switched capacitor resistor, you would get

$$\omega' = \frac{1}{RC_2} = f_{CLK} \frac{C_1}{C_2}$$

Thus, you can change the equivalent ω' of the circuit by changing the clock frequency. The value of ω' can be set very precisely because it depends only on the ratio of C_1 and C_2, and not their absolute value.

Switched Capacitor Filter Ics:

We will see some of the Switched capacitor filter Ics such as MF 5, MF10 and MF100
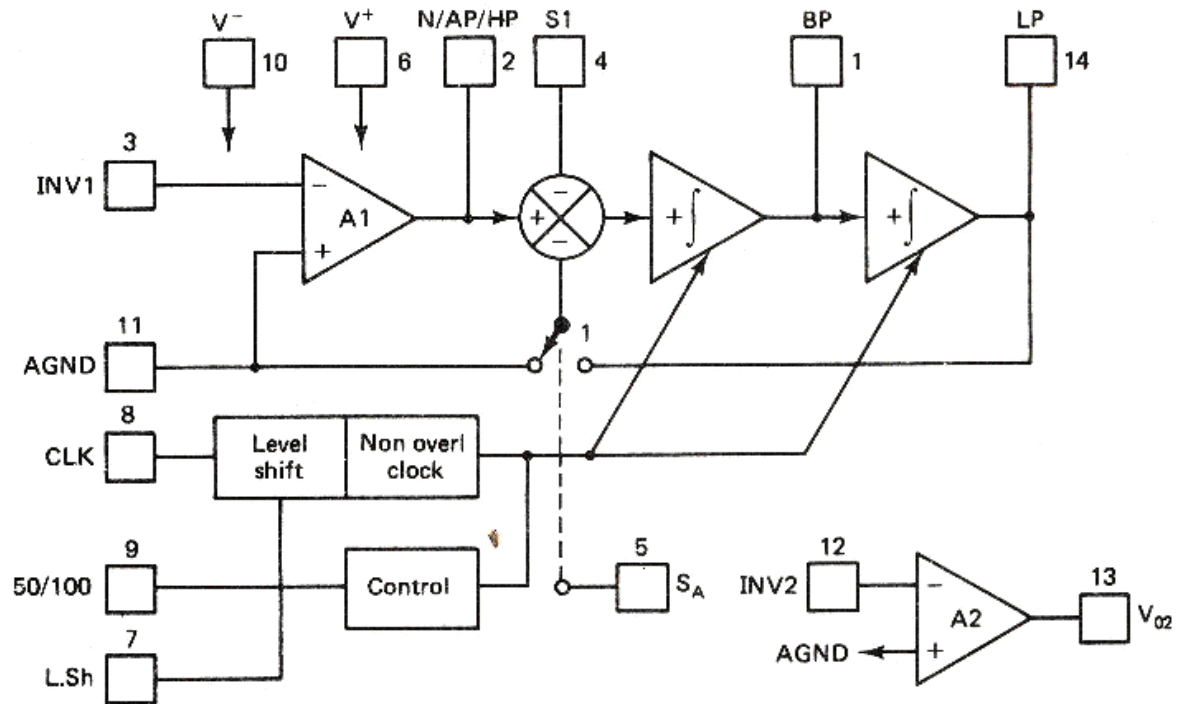
MF 5 :

It is the basic type of filter. This is called as universal filter because it can be used to synthesize any type of filters such as Band pass, Low-pass, High-pass, notch and all-pass. The block diagram

of MF5 was shown here. It consists of an operational amplifier, two positive integrators and summing node. A MOS switch is controlled by the logic input given at pin 5.

This switch is useful in connecting one of the inputs of first integrator to either ground or to the output of the second integrator. The way in which the external resistors are connected determines the characteristics of the filter. The maximum recommended clock frequency is 1 MH_z. There were three modes of operation and out of all modes, mode 3 is best. All the modes have three outputs with the combinations of different filter functions. And MF5 Can Operate with single or split power supply. The clock frequency to center frequency ration is selected with a help of pin 9. There were two ratio options 50:1 and 100:1.

Dual-in-line package

BP	1	14	LP
N/AP/HP	2	13	V_{02}
INV1	3	12	INV2
S1	4 (MF5)	11	AGND
S_A	5	10	V−
V+	6	9	50/100
L.Sh	7	8	CLK

Top view
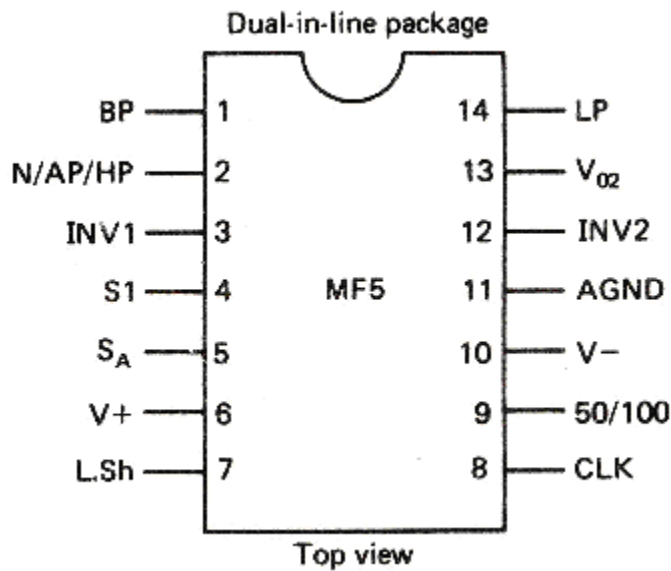
MF10:

The MF10 contains two of the second-order universal filter sections found in the MF5. Therefore with MF10, two second order filters or one fourth-order filter can be built. As the MF5 and MF10 have similar filter sections, the design procedure for them is same.
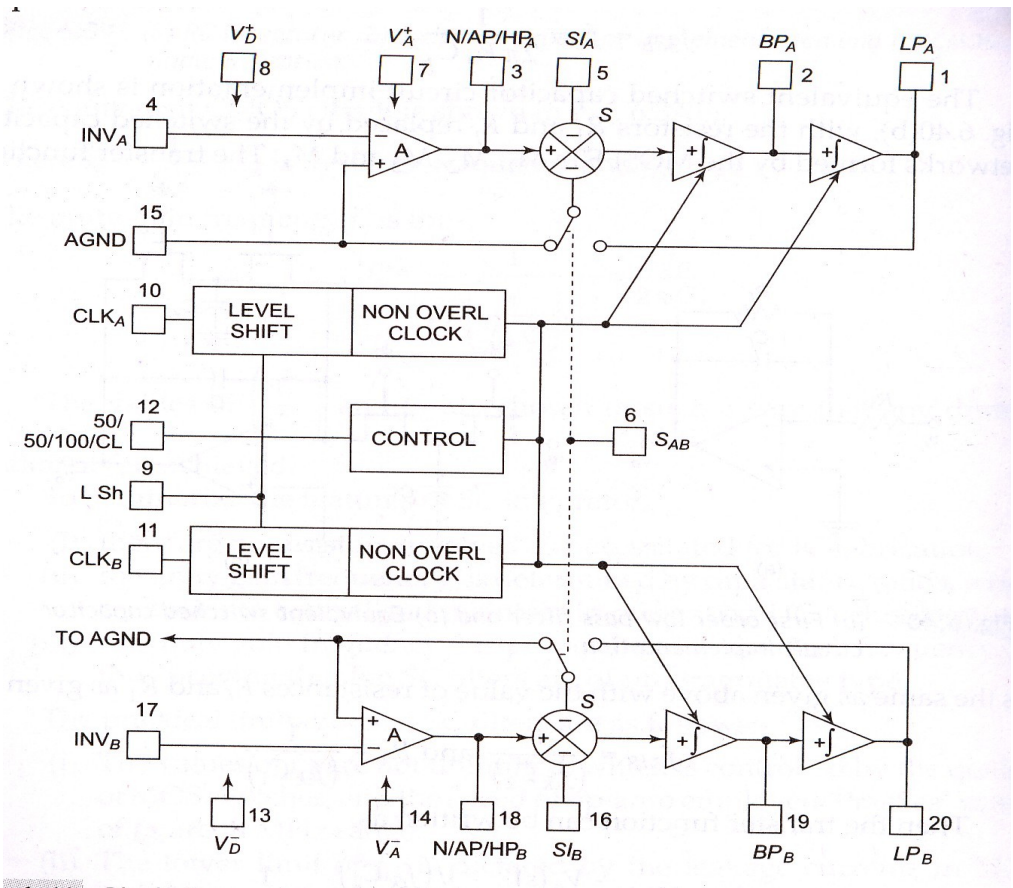
The LMF100 Switched Capacitor Filter:

In this lab you will be using the MF100, or LMF100 integrated circuit is a versatile circuit with four switched capacitor integrators, that can be connected as two second order filters or one fourth order filter. With this chip you can choose f' to either be 1/50 or 1/100 of the clock frequency (this is given by the ratio C_1/C_2 in the discussion above),. By changing internal and external connections to the circuit you can obtain different filter types (lowpass, highpass, bandpass, notch (bandreject) or allpass).

2nd Order Filters	
Filter Type	**Transfer Function**
Low Pass	$$H_{LP}(s) = \frac{H_{OLP}\omega_0^2}{s^2 + s\dfrac{\omega_0}{Q} + \omega_0^2}$$
High Pass	$$H_{HP}(s) = \frac{H_{OHP}s^2}{s^2 + s\dfrac{\omega_0}{Q} + \omega_0^2}$$
Band Pass	$$H_{BP}(s) = \frac{H_{OBP}\dfrac{\omega_0}{Q}s}{s^2 + s\dfrac{\omega_0}{Q} + \omega_0^2}$$
Notch (Band Reject)	$$H_{N}(s) = \frac{H_{ON}\left(\omega_0^2 + s^2\right)}{s^2 + s\dfrac{\omega_0}{Q} + \omega_0^2}$$

The pinout for the LMF100 is shown below (from the data sheet):
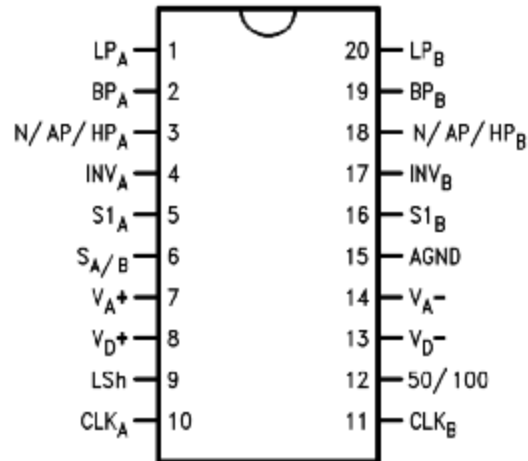
See that the chip, for the most part, is split into two halves, left and right. A block diagram of the left half ((and a few pins from the right half) is shown below.
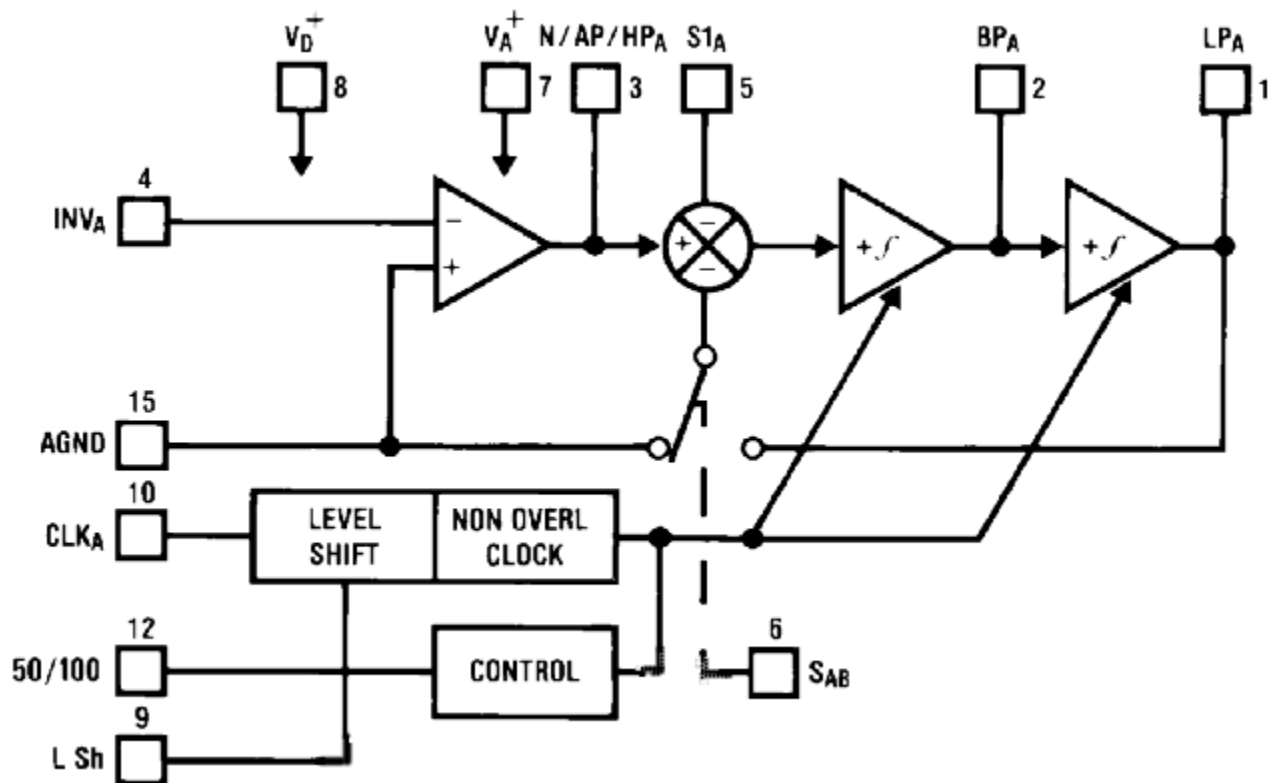
The pins are described as

50/100 - determines if the value of ω' is $\omega_{CLK}/100$, or $\omega_{CLK}/50$.

- CLK_A - is ω_{CLK}.

- INV_A - the inverting input to the op-amp

- $N/AP/HP_A$ - an intermediate output, and the non-inverting input to the summer. Used for Notch, All Pass or High Pass output.

- BP_A - another intermediate output, the output of the first integrator. Used for Band Pass output.

- LP_A - the output of the second integrator. Used for Low Pass output.

- $S1_A$ - an inverting input to the summer.

- S_{AB} - determines if the switch is to the left or to the right. That is, this pin determines if the second inverting input to the summer is ground (AGND), or the low pass output.

The two integrators are switched capacitor integrators. Their transfer functions are given by,

$$\frac{\omega'}{s}$$

where ω' is $\omega_{CLK}/100$, or $\omega_{CLK}/50$, depending on the state of the 50/100 pin. Note that the integrator is non-inverting.

A Typical Circuit:

The diagram below shows one of the modes (mode 1) of operations
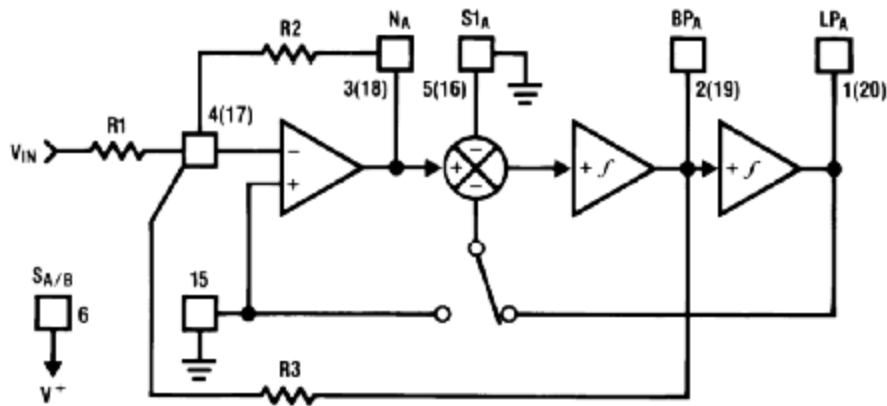
FIGURE 7. MODE 1

The filter specifications as given in the datasheet, and given below.

MODE 1: Notch 1, Bandpass, Lowpass Ou

$$f_{notch} = f_0 \text{ (See Figure 7)}$$

f_0 = center frequency of the complex po

$$= \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

f_{notch} = center frequency of the imaginary ze

H_{OLP} = Lowpass gain (as $f \rightarrow 0$) = $-\dfrac{R2}{R1}$

H_{OBP} = Bandpass gain (at $f = f_0$) = $-\dfrac{R3}{R1}$

H_{ON} = Notch output gain as $\left.\begin{array}{l} f \rightarrow 0 \\ f \rightarrow f_{CLK}/2 \end{array}\right\}$

$$Q = \frac{f_0}{BW} = \frac{R3}{R2}$$

The low pass (LP_A) output is easily given in terms of the band pass output (BP_A), as well as the band pass output as a function of the summer (SUM, not labeled on diagram).

$$LP_A = \frac{\omega'}{s} BP_A \ (1), \qquad BP_A = \frac{\omega'}{s} SUM \ (2)$$

The summer output (SUM) is simply the output of the op amp (N_A) minus the lowpass output (LP_A). However we can see that the op amp is set up as the inverting summing circuit. So

$$SUM = N_A - LP_A$$

$$SUM = -V_{IN} \frac{R_2}{R_1} - BP_A \frac{R_2}{R_3} - LP_A$$

Replace SUM on the left hand side using equation *(2)* from above, and LP_A using equation *(1)*.

$$BP_A \frac{s}{\omega'} = -V_{IN} \frac{R_2}{R_1} - BP_A \frac{R_2}{R_3} - \frac{\omega'}{s} BP_A$$

Rearranging brings

$$\frac{BP_A}{V_{IN}} = \frac{-\dfrac{R_2}{R_1}}{\dfrac{s}{\omega'} + \dfrac{R_2}{R_3} + \dfrac{\omega'}{s}} = \frac{-\dfrac{R_2}{R_1} s\omega'}{s^2 + \dfrac{R_2}{R_3} s\omega' + \omega'^2}$$

Equating this with the transfer function for a bandpass circuit

$$H_{BP}(s) = \frac{H_{OBP} \dfrac{\omega_0}{Q} s}{s^2 + s \dfrac{\omega_0}{Q} + \omega_0^2}$$

yields,

$$\omega_0 = \omega' = \frac{\omega_{CLK}}{100} \text{ or } \frac{\omega_{CLK}}{50},$$

$$Q = \frac{R_3}{R_2}, \quad \text{and}$$

$$H_{OBP} = -\frac{R_3}{R_1}$$

Similarly, the relationship between low pass and band pass, equation (1), can be used to find the low pass transfer function. The notch filter transfer function is derived in the same way.

POWER AUDIO AMPLIFIER IC LM380:

Features of LM380:

1. Internally fixed gain of 50 (34dB)
2. Output is automatically self centring to one half of the supply voltage.
3. Output is short circuit proof with internal thermal limiting.
4. Input stage allows the input to be ground referenced or ac coupled.
5. Wide supply voltage range (5 to 22V).
6. High peak current capability.
7. High impedence.
8. Low total harmonic distortion
9. Bandwidth of 100KHz at Pout = 2W & $R_L = 8\Omega$

Introduction:

Small signal amplifier are essentially voltage amplifier that supply their loads with larger amplifier signal voltage.

On the other hand , large signal or power amplifier supply a large signal current to current operated loads such as speakers & motors.

In audio applications, however, the amplifier called upon to deliver much higher current than that suppkied by general purpose op-amps. This means that loads such as speakers & motors requiring substantial currents cannot be driven directly by the output of general purpose opo-amps.

However there are two possible solutions,

- To use discrete or monolithic power transistors called power boosters at the output of the op-amp
- To use specialized ICs designed as power amplifiers.
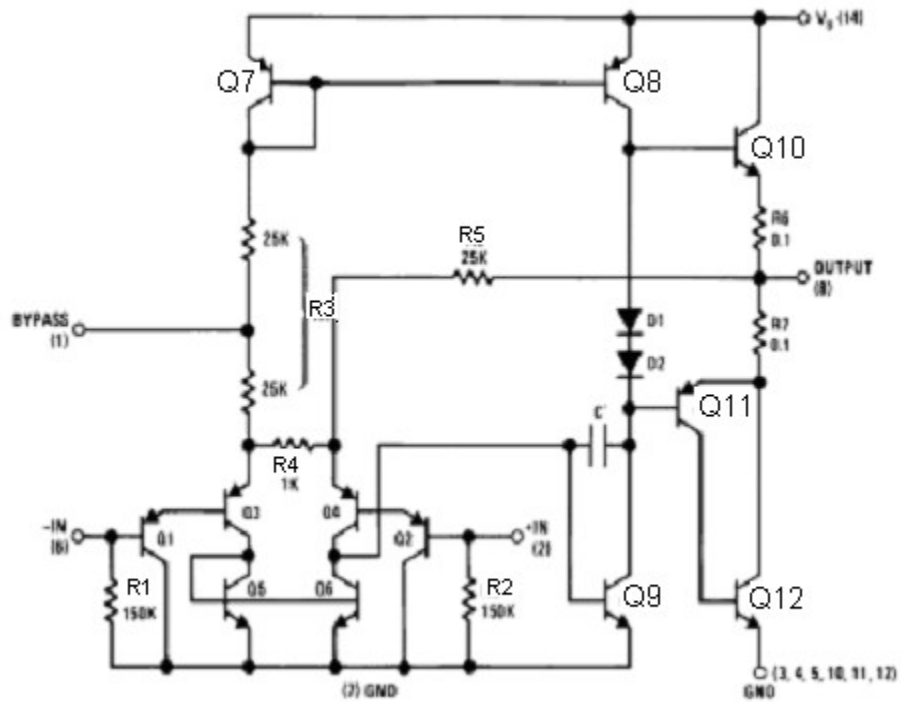
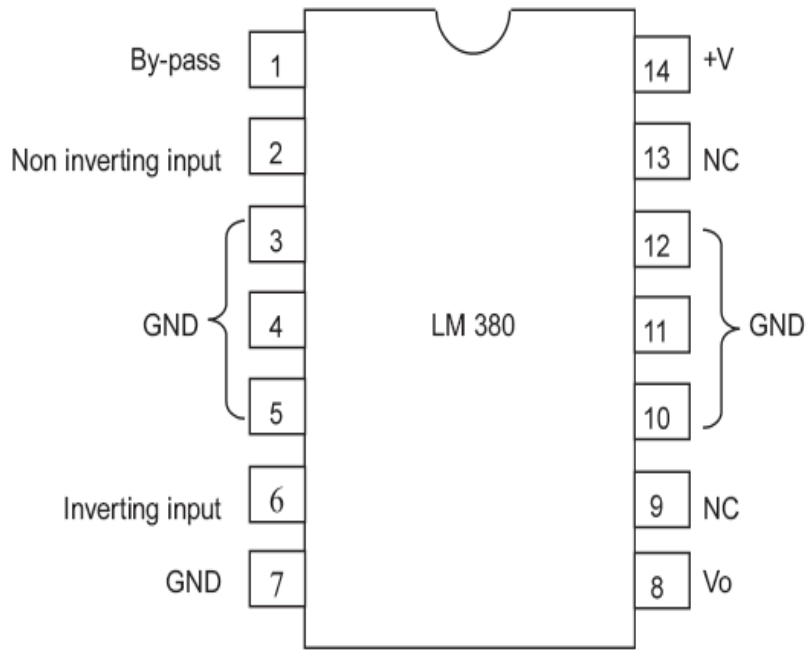Fig : Functional block diagram of Audio Power Amplifier
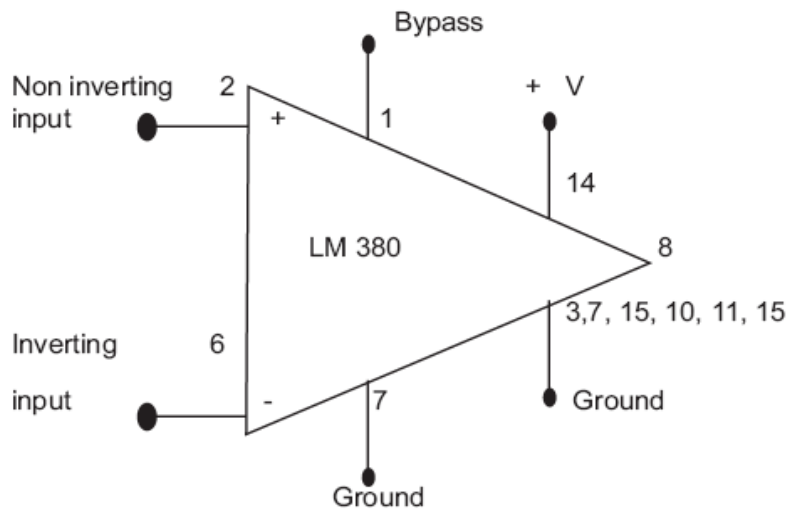
Fig: Pin diagram

Fig : Block diagram

LM380 circuit description:

It is connected of 4 stages,

(i) PNP emitter follower

(ii) Different amplifier

(iii) Common emitter

(iv) Emitter follower

(i) PNP Emitter follower:

- The input stage is emitter follower composed of PNP transistors Q1 & Q2 which drives the PNP Q3-Q4 differential pair.
- The choice of PNP input transistors Q1 & Q2 allows the input to be referenced to ground i.e., the input can be direct coupled to either the inverting & non-inverting terminals of the amplifier.

(ii) Differential Amplifier:

- The current in the PNP differential pair Q3-Q4 is established by Q7, R3 & +V.
- The current mirror formed by transistor Q7, Q8 & associated resistors then establishes the collector current of Q9.
- Transistor Q5 & Q6 constitute of collector loads for the PNP differential pair.
- The output of the differential amplifier is taken at the junction of Q4 & Q6 transistors & is applied as an input to the common emitter voltage gain.

(iii) Common Emitter:

- Common Emitter amplifier stage is formed by transistor Q9 with D1, D2 & Q8 as a current source load.
- The capacitor C between the base & collector of Q9 provides internal compensation & helps to establish the upper cutoff frequency of 100 KHz.

- Since Q7 & Q8 form a current mirror, the current through D1 & D2 is approximately the same as the current through R3.
- D1 & D2 are temperature compensating diodes for transistors Q10 & Q11 in that D1 & D2 have the same characteristics as the base-emitter junctions of Q11. Therefore the current through Q10 & (Q11-Q12) is approximately equal to the current through diodes D1 & D2.

(iv) (Output stage) - Emitter follower:

- Emitter follower formed by NPN transistor Q10 & Q11. The combination of PNP transistor Q11 & NPN transistor Q12 has the power capability of an NPN transistors but the characteristics of a PNP transistor.
- The negative dc feedback applied through R5 balances the differential amplifier so that the dc output voltage is stabilized at +V/2;
- To decouple the input stage from the supply voltage +V, by pass capacitor in order of micro farad should be connected between the by pass terminal (pin 1) & ground (pin 7).
- The overall internal gain of the amplifier is fixed at 50. However gain can be increased by using positive feedback.

APPLICATIONS:

(i) Audio Power Amplifier:
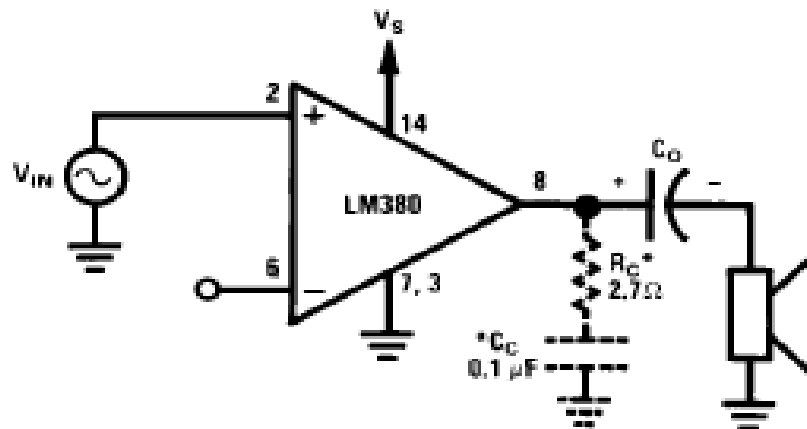
- Amplifier requires very few external components because of the internal biasing, compensation & fixed gain.
- When the power amplifier is used in the non inverting configuration, the inverting terminal may be either shorted to ground, connected to ground through resistors & capacitors.
- Similarly when the power amplifier is used in the inverting mode, the non inverting terminal may be either shorted to ground or returned to ground through resistor or capacitor.
- Usually a capacitor is connected between the inverting terminal & ground if the input has a high internal impedance.
- As a precautionary measure, an RC combination should be used at the output terminal (pin 8) to eliminate 5-to-10 MHz oscillation.
- C1 is coupling capacitor which couples the output of the amplifier to the 8 ohms loud speaker which act as a load. The amplifier will amplify the V_{in} applied at the non-inverting terminal.

**(ii) LM 380 as a High gain:**
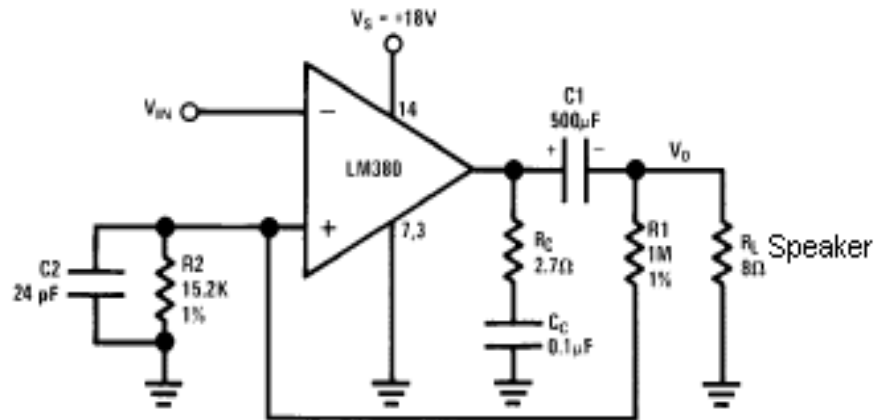
- The gain of LM380 is internally fixed at 50. But it can be increased by using the external components.
- The increase in gain is possible due to the use of positive feedback, this setup to obtain a gain 200.

(iii) LM 380 as a variable Gain:

- Instead of getting a fixed gain of 50, it is possible to obtain a variable gain up to 50 by connecting a potentiometer between the input terminals.
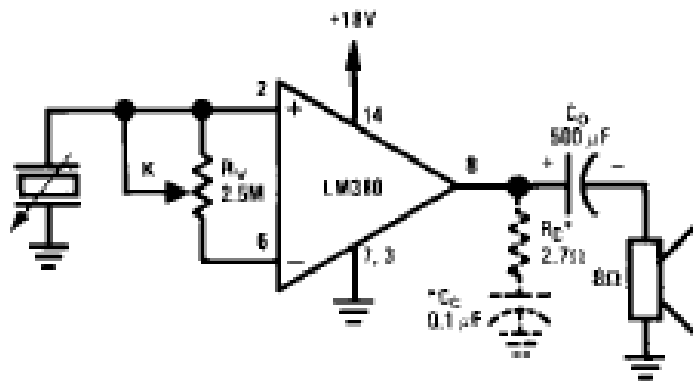
(iv) LM 380 as a Bridge Audio Power Amplifier:
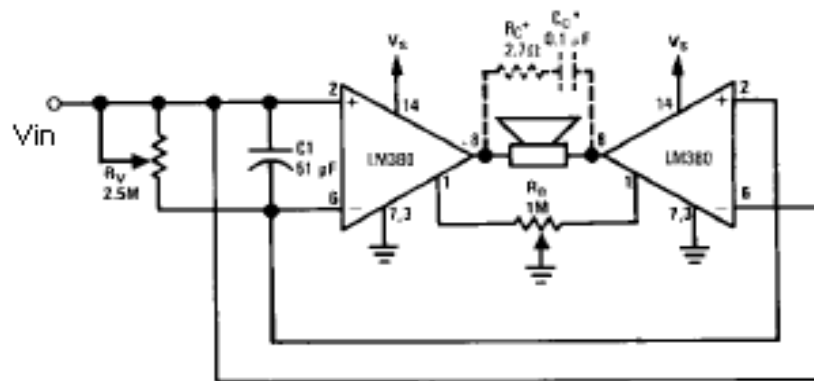
- If a certain application requires more power than what is provided by a single LM380 amplifier, then 2 LM380 chips can be used in the bridge configuration.
- With this arrangement we get an output voltage swing which is twice that of a single LM380 amplifier.
- As the voltage is doubled, power output will increase by four times that of a single LM380 amplifier. The pot R4 is used to balance the output offset voltages of the two chips.

(v) Intercom system using LM 380:

- When the switch is in Talk mode position, the master speaker acts as a microphone.
- When the switch is in Listen position, the remote speaker acts as a microphone.
- In either phone the overall gain of the circuit is the same depends on the turns of transformer T.
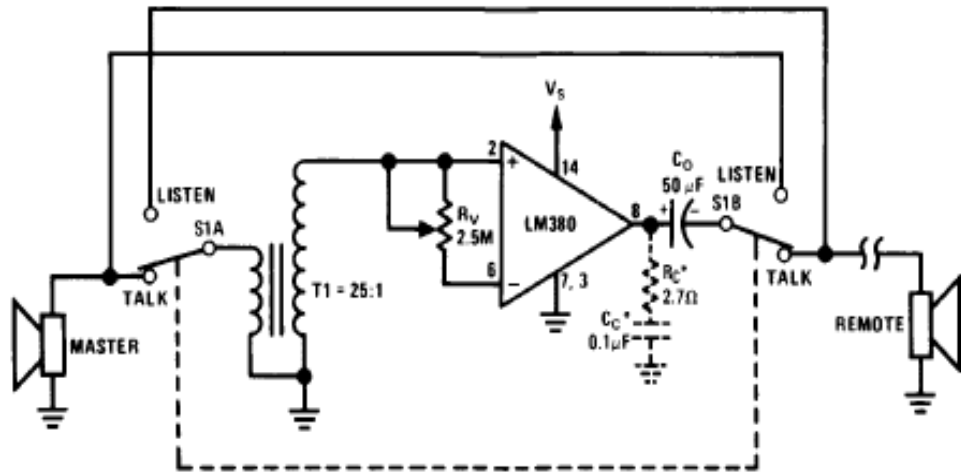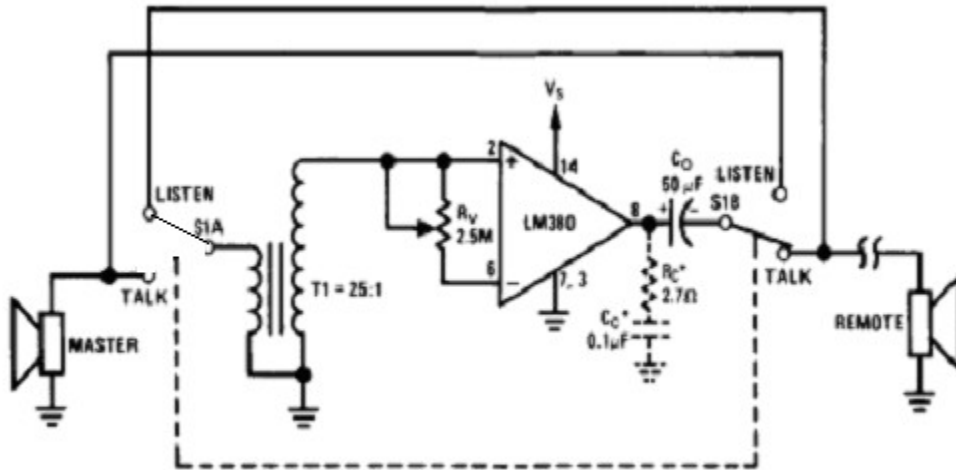
Fig: Talk mode

Fig: Listen mode

OPTOCOUPLERS/OPTOISOLATORS:

- Optocouplers or Optoisolators is a combination of light source & light detector in the same package.

- They are used to couple signal from one point to other optically, by providing a completer electric isolation between them. This kind of isolation is provided between a low power control circuit & high power output circuit, to protect the control circuit.

- Depending on the type of light source & detector used we can get a variety of optocouplers. They are as follows,

    (i)   LED – LDR optocoupler

    (ii)   LED – Photodiode optocoupler

    (iii)   LED – Phototransistor optocoupler

Characteristics of optocoupler:

(i)   Current Transfer Ratio (CTR)

(ii)   Isolation Voltage

(iii)   Response Time

(iv)   Common Mode Rejection

(i) Current Transfer Ratio:

      It is defined as the ratio of output collector current (I_c) to the input forward current (I_f)

$$CTR = I_c/I_f * 100\%$$

      Its value depends on the devices used as source & detector.

(ii) Isolation voltage between input & output:

      It is the maximum voltage which can exist differentially between the input & output without affecting the electrical isolation voltage is specified in K Vrms with a relative humidity of 40 to 60%.

(iii)Response Time:

Response time indicates how fast an optocoupler can change its output state. Response time largely depends on the detector transistor, input current & load resistance.

(iv)Common mode Rejection:

Eventhough the optocouplers are electrically isolated for dc & low frequency signals, an impulsive input signal (the signal which changes suddenly) can give rise to a displacement current $I_c = C_f * dv/dt$. This current can flow between input & output due to the capacitance C_f existing between input & output. This allow the noise to appear in the output.

Types of optocoupler:
(i) LED – Photodiode optocoupler:
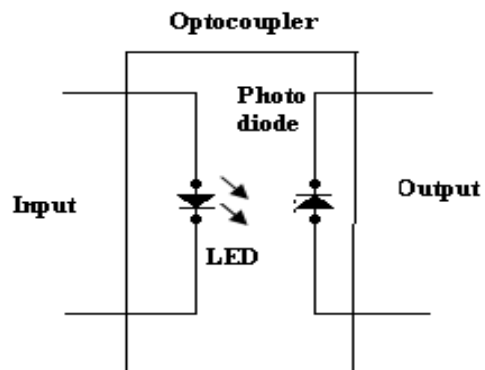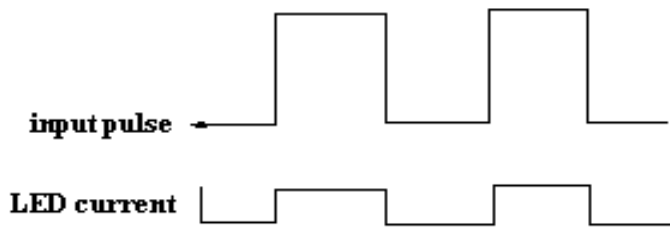
- LED photodiode shown in figure, here the infrared LED acts as a light source & photodiode is used as a detector.
- The advantage of using the photodiode is its high linearity. When the pulse at the input goes high, the LED turns ON. It emits light. This light is focused on the photodiode.
- In response to this light the photocurrent will start flowing though the photodiode. As soon as the input pulse reduces to zero, the LED turns OFF & the photocurrent through the photodiode reduces to zero. Thus the pulse at the input is coupled to the output side.

(ii) LED – Phototransistor Optocoupler:
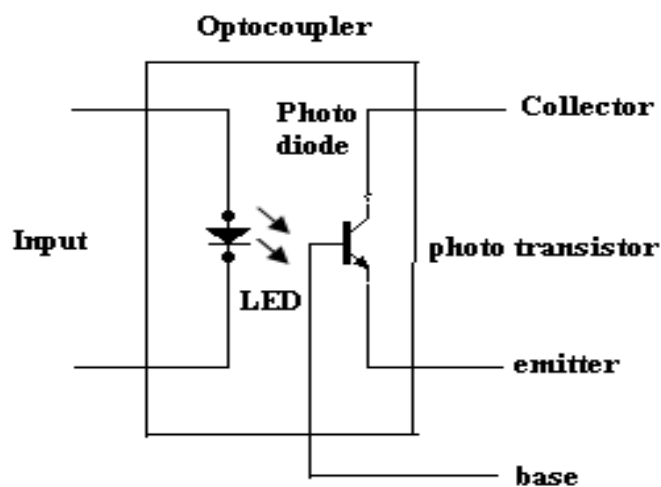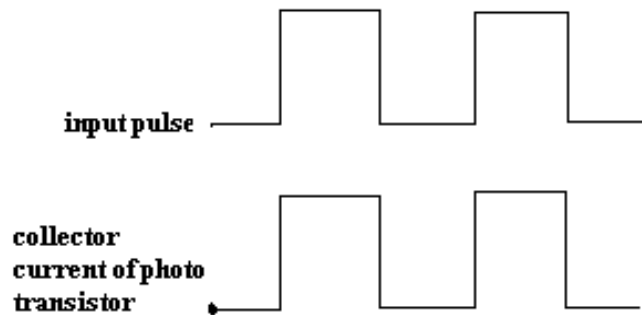
- The LED phototransistor optocoupler shown in figure. An infrared LED acts as a light source and the phototransistor acts as a photo detector.

- This is the most popularly used optocoupler, because it does not need any additional amplification.

- When the pulse at the input goes high, the LED turns ON. The light emitted by the LED is focused on the CB junction of the phototransistor.

- In response to this light photocurrent starts flowing which acts as a base current for the phototransistor.

- The collector current of phototransistor starts flowing. As soon as the input pulse reduces to zero, the LED turns OFF & the collector current of phototransistor reduces to zero. Thus the pulse at the input is optically coupled to the output side.

Advantages of Optocoupler:

- Control circuits are well protected due to electrical isolation.
- Wideband signal transmission is possible.
- Due to unidirectional signal transfer, noise from the output side does not get coupled to the input side.
- Interfacing with logic circuits is easily possible.
- It is small size & light weight device.

Disadvantages:

- Slow speed.

- Possibility of signal coupling for high power signals.
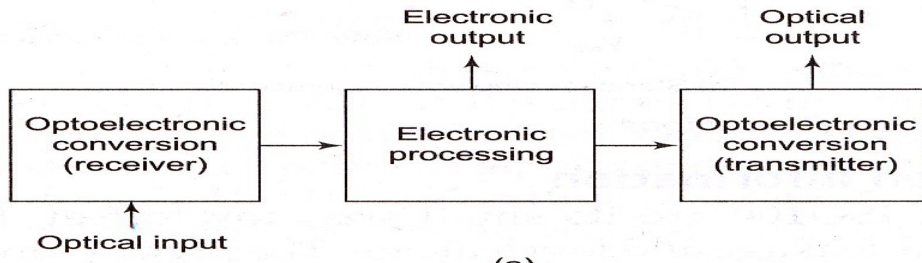
Applications:

Optocouplers are used basically to isolate low power circuits from high
power circuits.

- At the same time the control signals are coupled from the control circuits to the high power circuits.
- Some of such applications are,
    - (i)   AC to DC converters used for DC motor speed control
    - (ii)   High power choppers
    - (iii) High power inverters
- One of the most important applications of an optocoupler is to couple the base driving signals to a power transistor connected in a DC-DC chopper.

- Note that the input & output waveforms are 180º out of phase as the output is taken at the collector of the phototransistor.
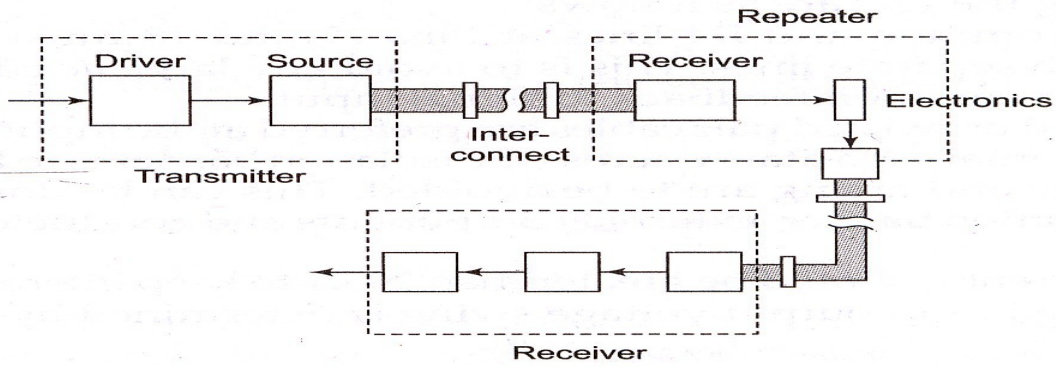
Optocoupler IC:

The optocouplers are available in the IC form MCT2E is the standard optocoupler IC which is used popularly in many electronic application.
- This input is applied between pin 1& pin 2. An infrared light emitting diode is connected between these pins.
- The infrared radiation from the LED gets focused on the internal phototransistor.
- The base of the phototransistor is generally left open. But sometimes a high value pull down resistance is connected from the Base to ground to improve the sensitivity.
- The block diagram shows the opto-electronic-integrated ciruit (OEIC) and the major components of a fiber-optic communication facility.

Optical input

(a)

Repeater

Driver · Source · Inter-connect · Receiver · Electronics

Transmitter

Receiver

(b)