Video Graphics Array (VGA)

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Image Source: Google Images

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  - Design goals
  - Evolution
- The protocol
  - Signals
  - Timing
  - Voltages
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- VGA settings and configurations
- Modern alternatives (HDMI)

History

From Analog to LCD

Early VGA

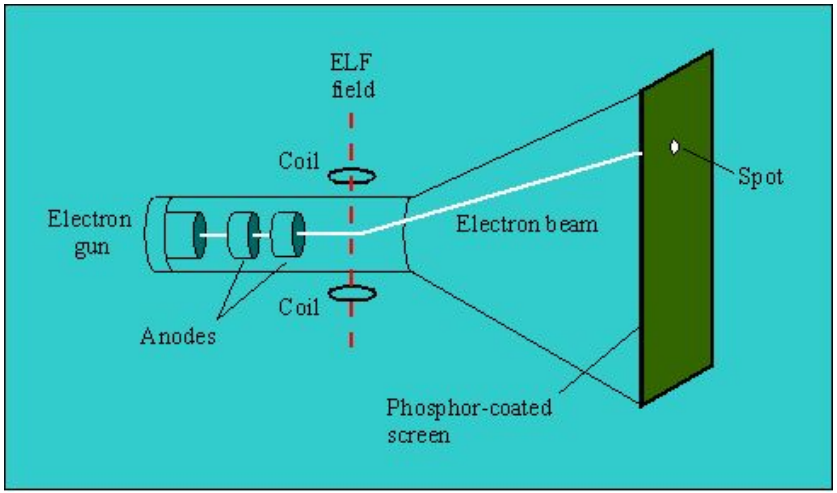
- Introduced by IBM in 1987
- Resolution: 640x480
- Designed specifically for analog displays

https://1000logos.net/ibm-logo/

Analog Displays

- Used Cathode Ray Tubes(CRT)
- Electron beam activates pixels
- Scans across the screen in rows
- Works similar to a typewriter

https://topclassactions.com/lawsuit-settlements/closed-settlements/14097-crt-antitrust-litigation-class-action-settlement/



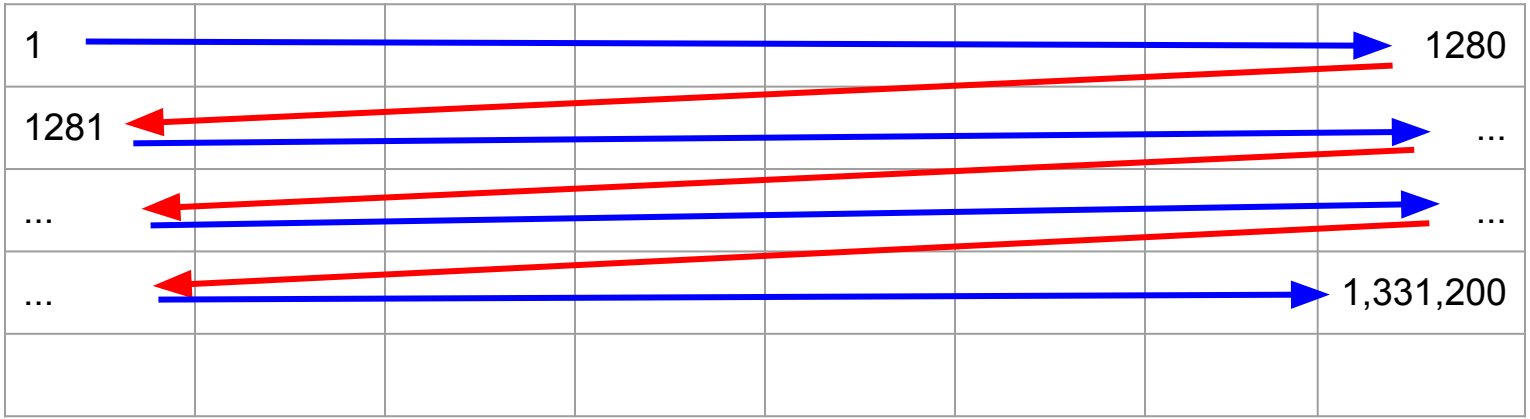
https://cdn.ttgtmedia.com/WhatIs/images/crt.gif

Analog Displays

https://gizmodo.com/its-easier-to-understand-how-tvs-work-when-you-watch-th-1822190499

Backup If Video Doesn't Work

Incoming Data [pixel 1331200, …, pixel 2, pixel 1] → Receiver



Left to Right, Top to Bottom
(just like you read)

LCD Displays

- Replaced analog displays
- Allows for much higher resolutions
- Uses digital data
- Most support VGA

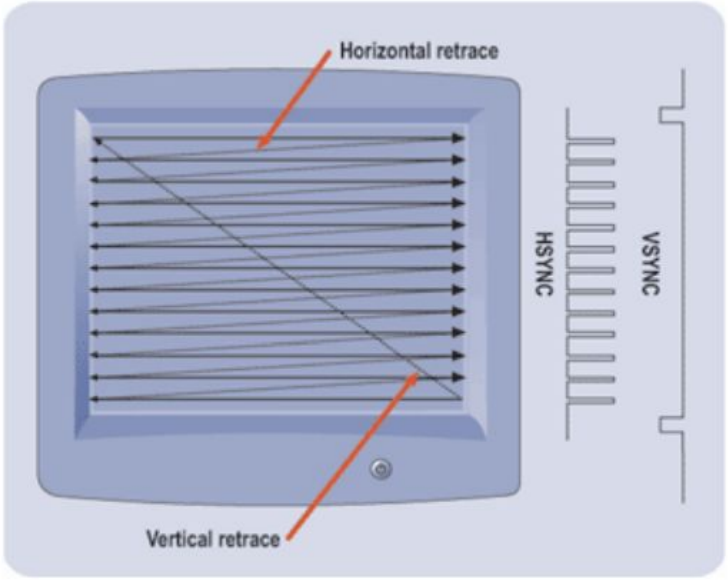
https://www.thegoodguys.com.au/linden-50-inches127cm-fhd-led-lcd-tv-l50htv17

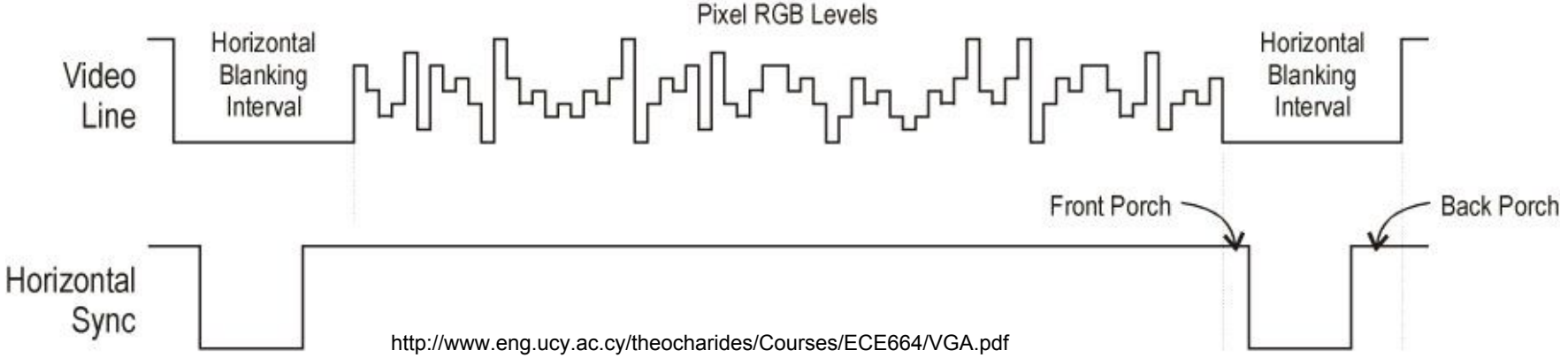
The Protocol

Signals, Timing, Specifications

Horizontal/Vertical Scan

- Scan speed determined by screen size and refresh rate
- Sync pulses moderate scan speed

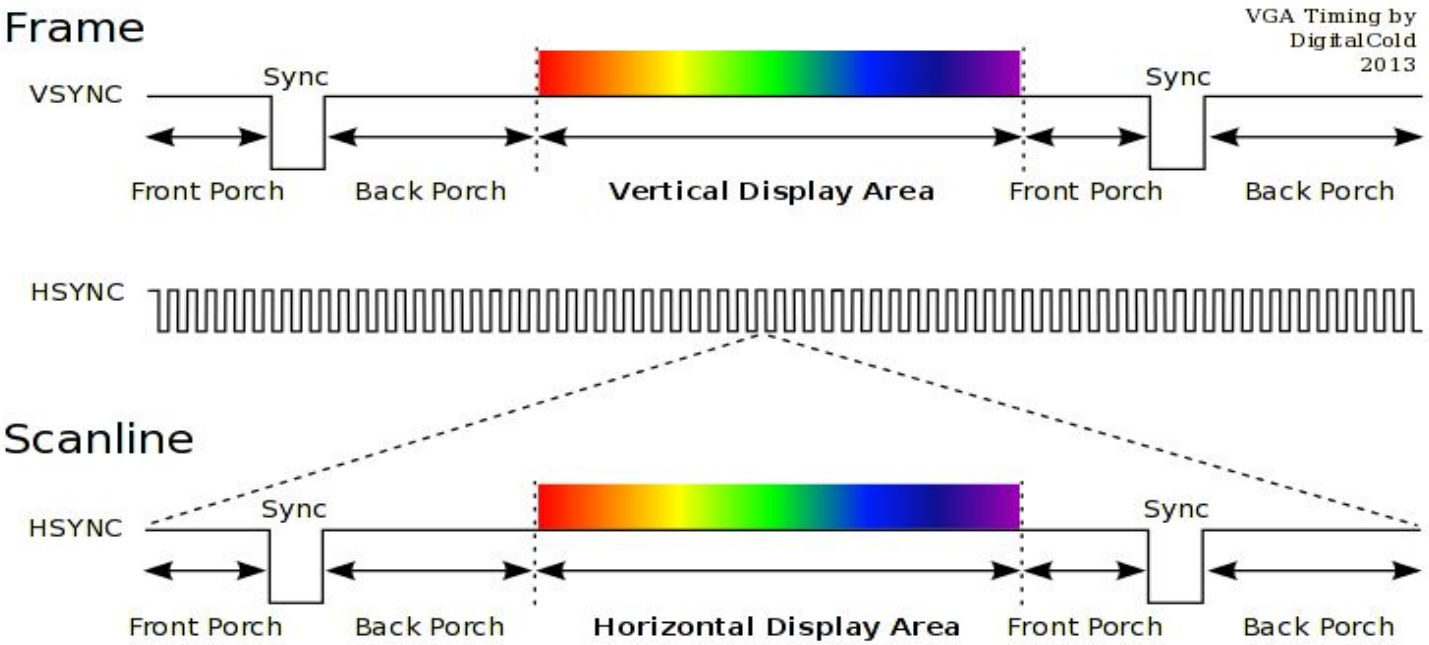




http://www.eng.ucy.ac.cy/theocharides/Courses/ECE664/VGA.pdf
http://www.eecg.toronto.edu/~tm4/rgbout.html

Timing

http://www.jimmellon.co.uk/vga-timing-diagram.html



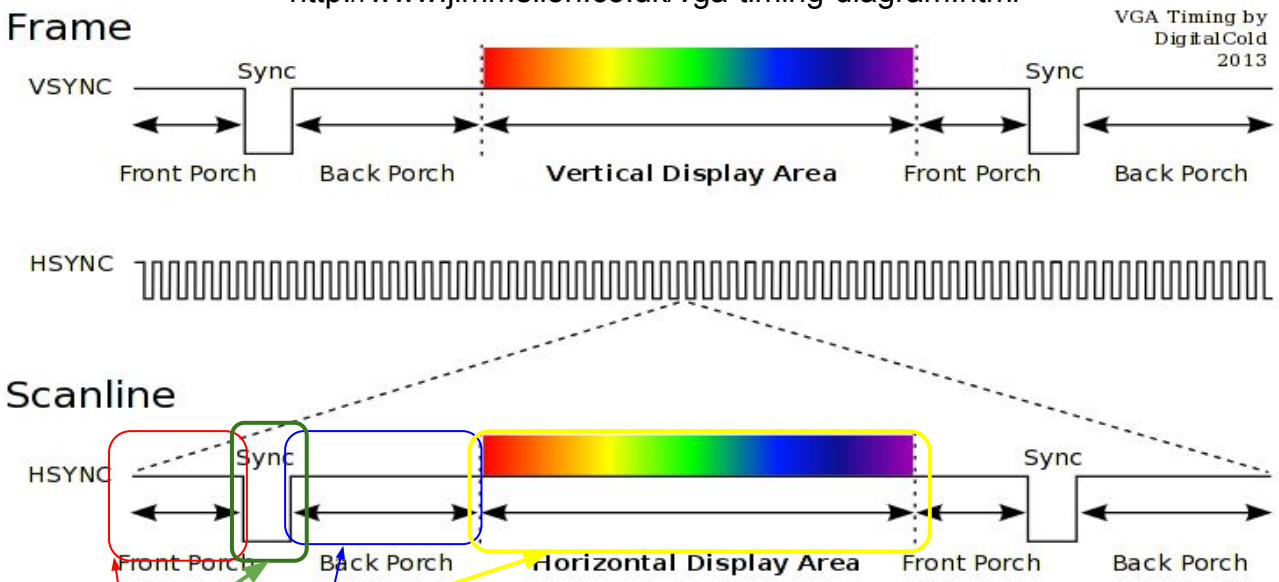
30 second problem. Given:

- Resolution = 1280 x 1024 @ 60 Hz
  - **How many pixels in one horizontal line?**
- Pixel frequency = 108 MHz
- Horizontal Front Porch = 48 pixels, Back Porch = 248 pixels, Sync Pulse = 112 pixels

Find the time to scan one horizontal line

Answer

http://www.jimmellon.co.uk/vga-timing-diagram.html



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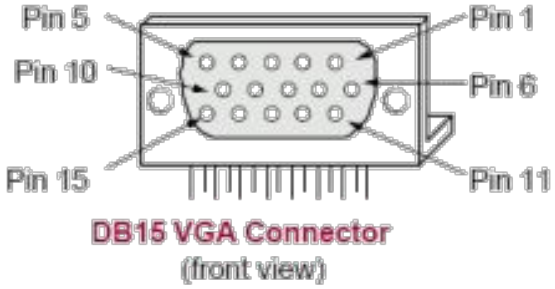
Find the time to scan one horizontal line

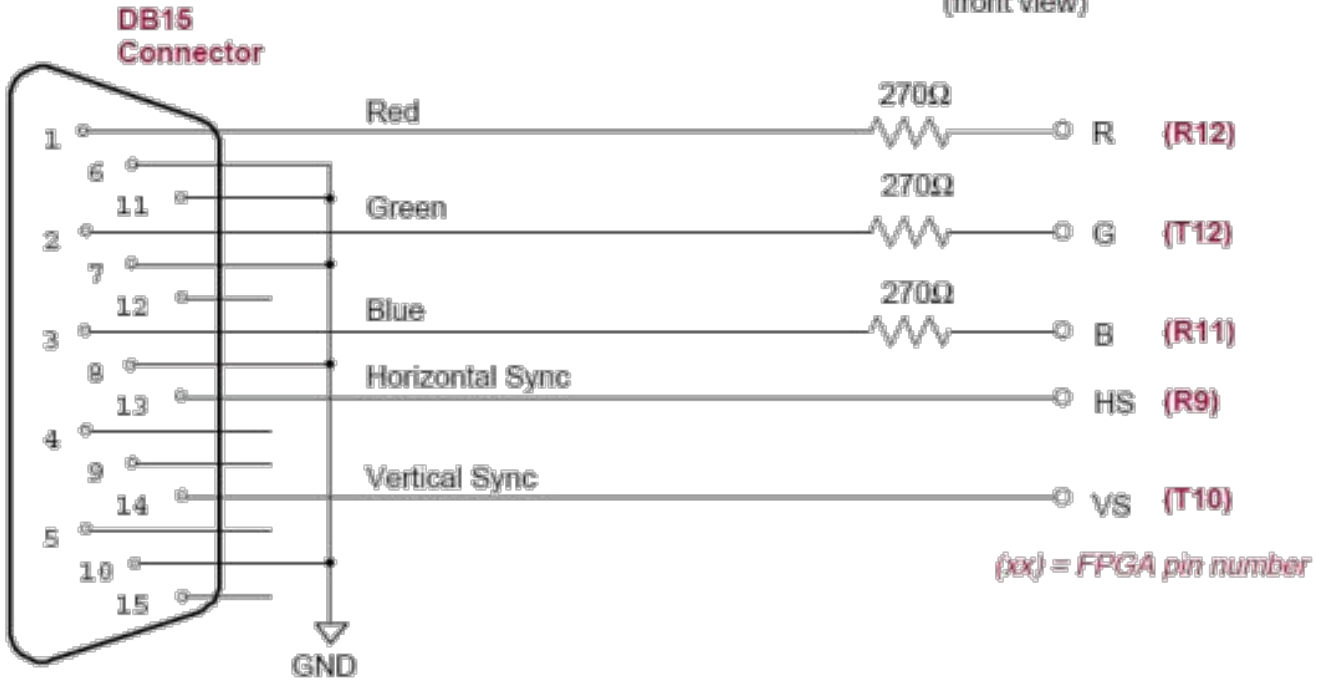
$$48 + 112 + 248 + 1280 = 1688\ pixels/line$$

$$\frac{1\ second}{108 * 10^6\ pixels} * 1688 \frac{pixels}{line} \approx \frac{15.6\ \mu s}{line}$$

The Cable

- 5 protocol pins
- 5 ground pins
- 4 ID pins
- 1 key pin





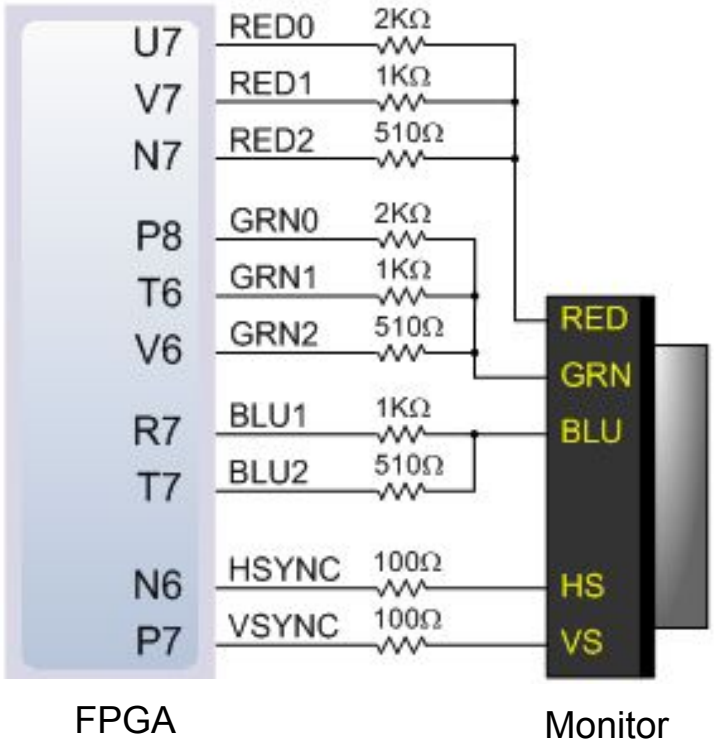
https://goo.gl/images/AANogs

Our Implementation

Progress and Plans

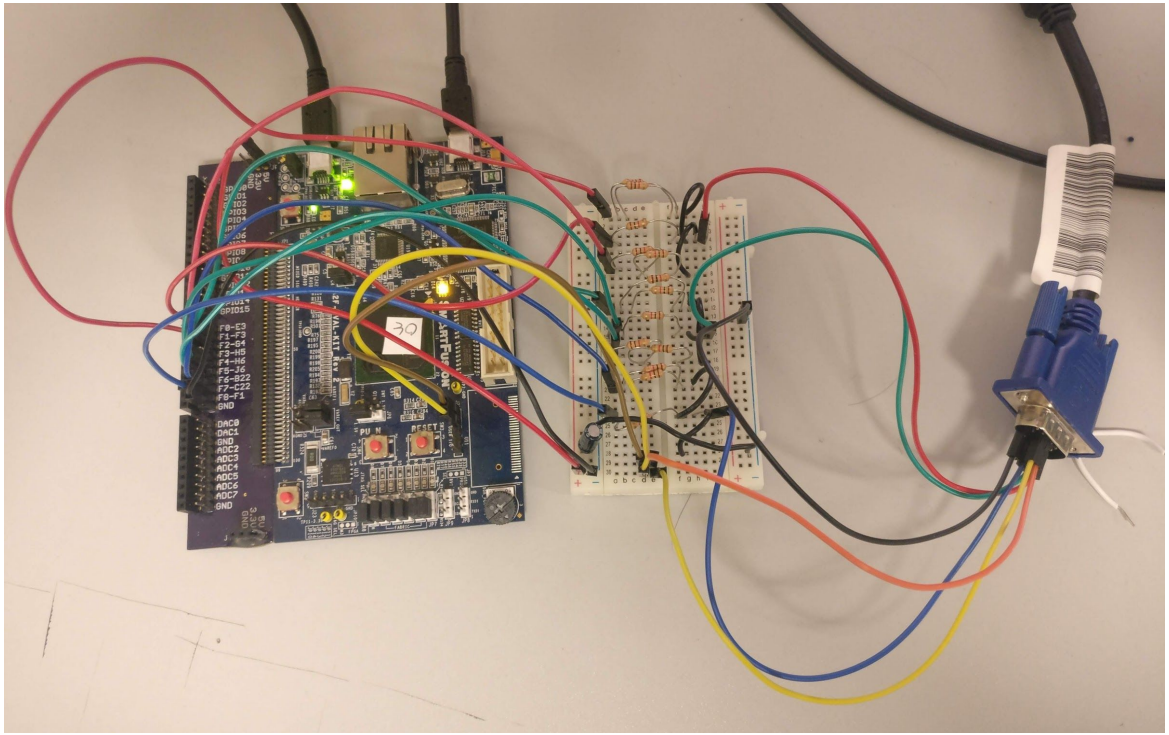
Analog Voltage Outputs

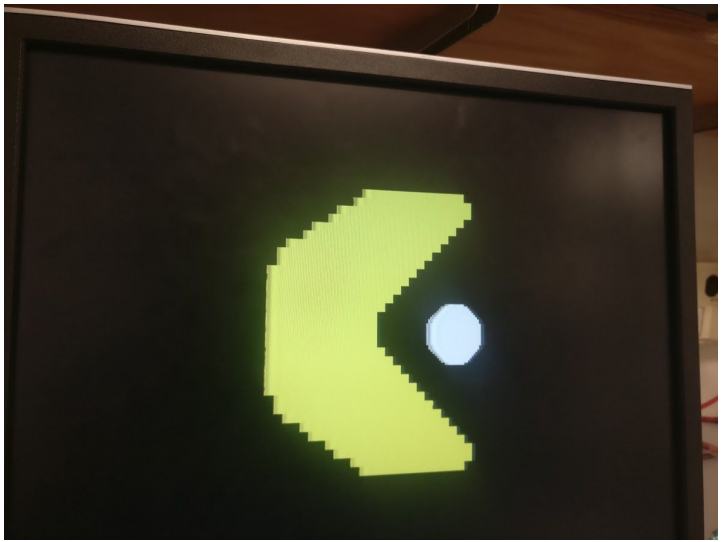
- Vestigial from analog TV
  - Current LCDs use a ADC
- R/G/B: 0 - 0.7 Volts
- Hysnc/Vsync: 3.3 or 5.5 Volts
- RGB stored in 8 bits for alignment



https://www.youtube.com/watch?v=wzhDRIX2Ors&t=11s

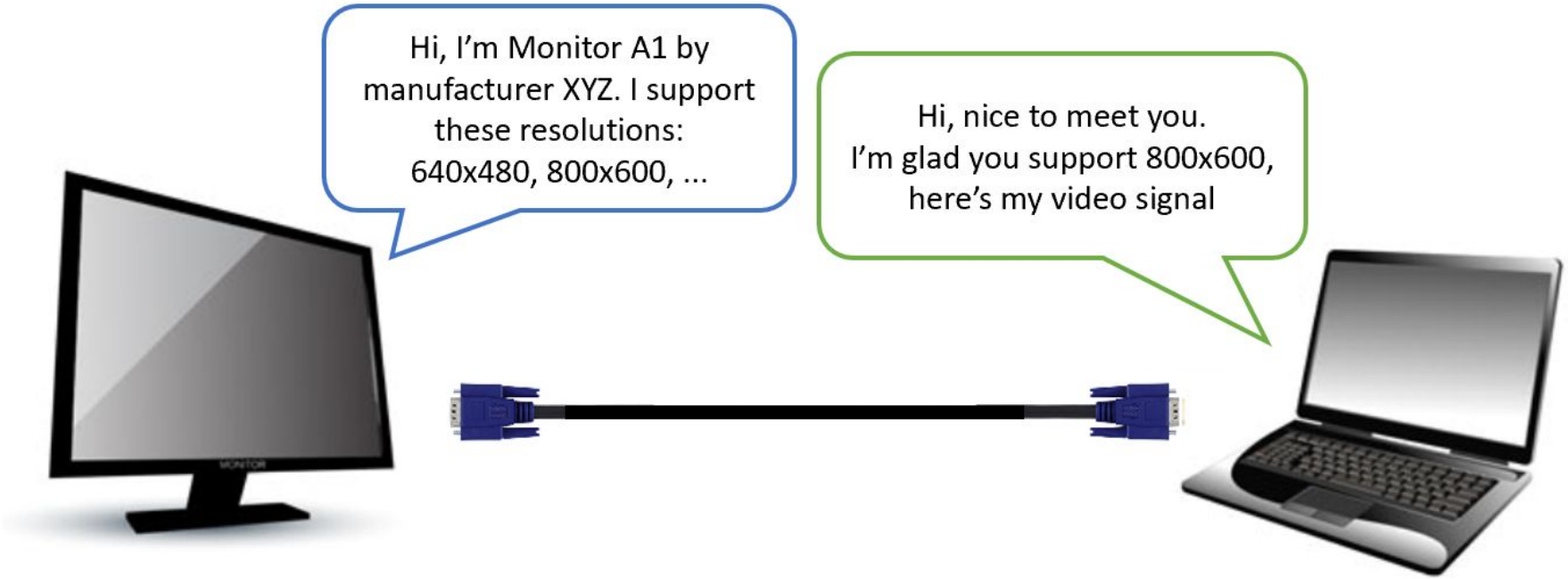
Physical Interface With Monitor





VGA Settings

Monitor Identification and Image Storage



Adapted from:
https://www.epiphan.com/blog/what-is-edid-and-why-is-it-important/

Display Data Channel (DDC)

- Displays can share supported displays modes
- Historically utilizes dedicated ID pins ID0-ID3
- Extended display identification data (EDID) stored in EEPROM
  - Describes capabilities of monitor and supported graphics modes
  - Stored as a 128 or 256 byte binary file
  - Former key pin provides 5V to power ROM even when monitor is off
- DDC2B - Most common form
  - Based on I2C serial communication
  - Uses ID1 as SDA and ID3 as SCL
  - Unidirectional, monitor slave always provides EDID at address 0x50

Extended Display Data Channel (E-DDC)

- Most modern form of the DDC standard
- Range of EDID storage extended up to 32 KiB
- 256 byte segments are selected by passing a 8-bit segment index to I2C address 0x30
  - Segment range is 0x00 - 0x7F
  - Read performed immediately after like normal DDC2B
  - Index auto-resets on NACK or STOP to provide backwards compatibility

Methods for Storing Image Data

- **Standard**: Maintain a frame buffer the size of the screen with 1 byte of RGB data per pixel

  Pros: Can be used for video or complex images
  Cons: Memory intensive

- **Memory-Efficient**: Store “sprites” of independent bitmap objects and their positions in the frame

  Pros: Uses less memory, possible without main CPU
  Cons: Only practical as a primary tool for simple bitmaps

https://en.wikipedia.org/wiki/File:Pac-man.png

HDMI

High Definition Multimedia Interface

HDMI Keeps Evolving

- Released in early 2000s and began seeing it in 2004-2005
- Today covers Version 1.0-1.2a
- Version 2.1 supports approximately 10x the bandwidth
  - 4k at greater than 30 Hz
  - 8k at 120 Hz with Display Stream Compression (DSC)
  - Deep color (twice as many bits/color)

https://www.diffen.com/difference/HDMI_vs_VGA

https://img.dxcdn.com/productimages/sku_489282_1.jpg

HDMI Transmits Digital Data

- TMDS - Transition Minimized Differential Signaling
- Advanced encoding scheme
  - 10-bit transmission for every 8 bits
  - Edge minimizing
  - DC balance
- ~162 MHz
- 1 pixel/clock
- Extremely Reliable

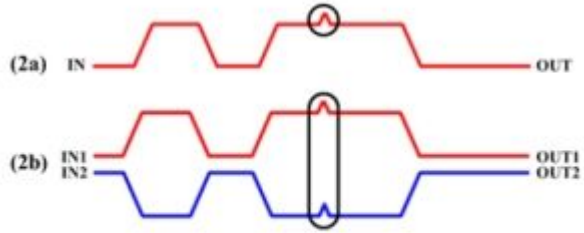
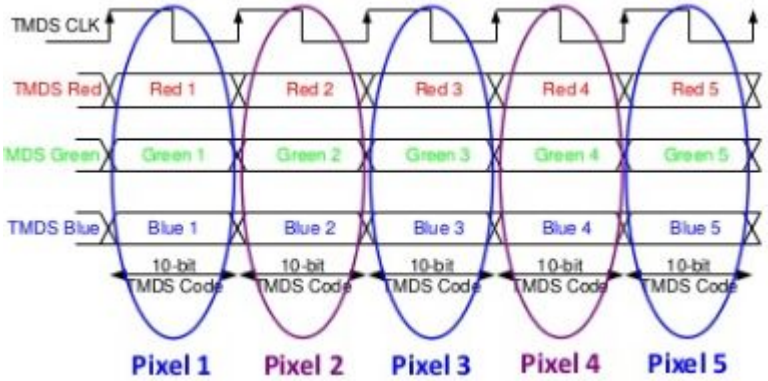


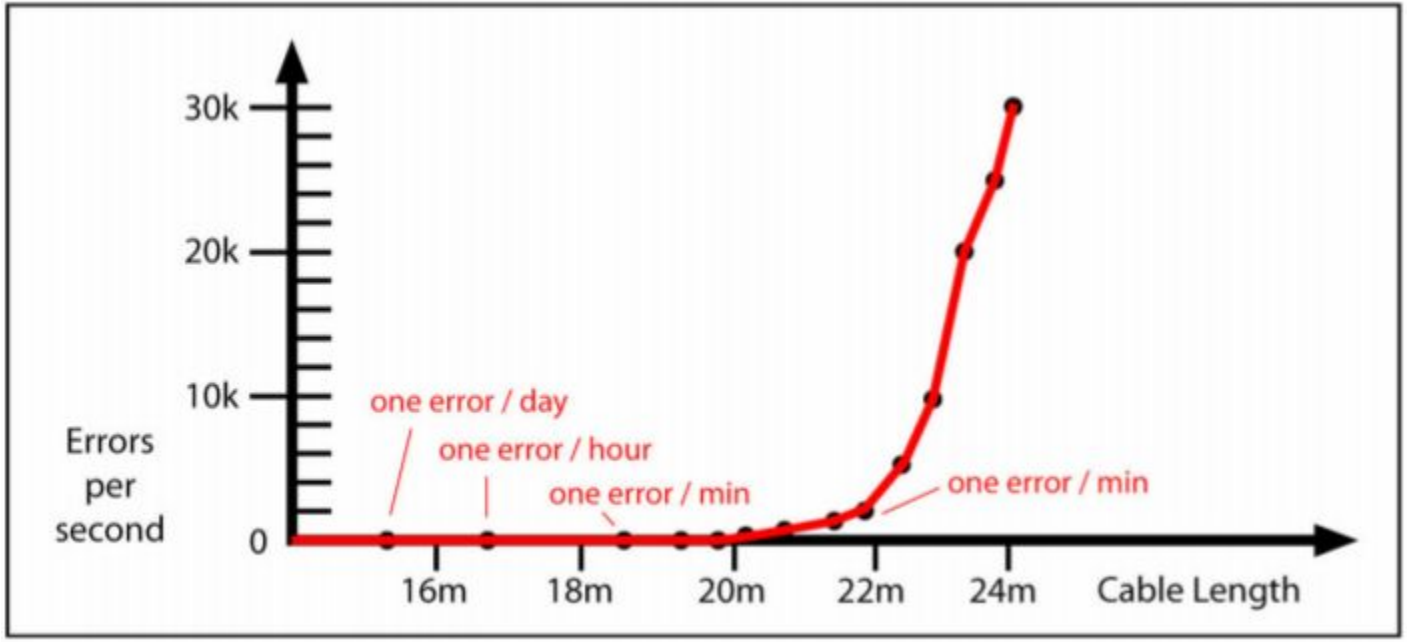
Figure 2. Impact of noise on (2a) single-ended signals; (2b) differential signals. Noise is highlighted with black.

https://www.army-technology.com/wp-content/uploads/static-progressive/nri/army/clients/Omnetics/omnetics_fig2.jpg



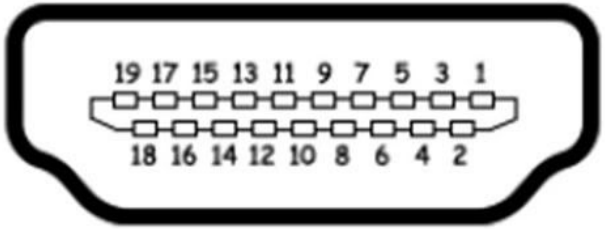
https://image.slidesharecdn.com/hdmivijaychachara152-140526050115-phpapp02/95/hdmi-15-638.jpg?cb=1401082522

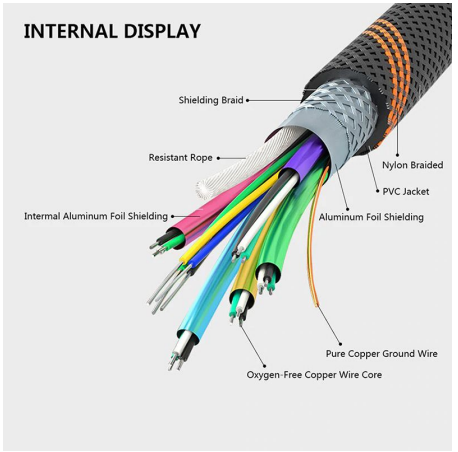
Reliable



https://www.fpga4fun.com/files/HDMI_Demystified_rev_1_02.pdf

HDMI Pinout





https://ae01.alicdn.com/kf/HTB1erTXRpXXXXaJXVXXq6xXFXXXG/SAMZHE-Braid-HDMI-Cable-HDMI-to-HDMI-2-0-4K-2K-Double-magnetic-ring-shielded-for.jpg

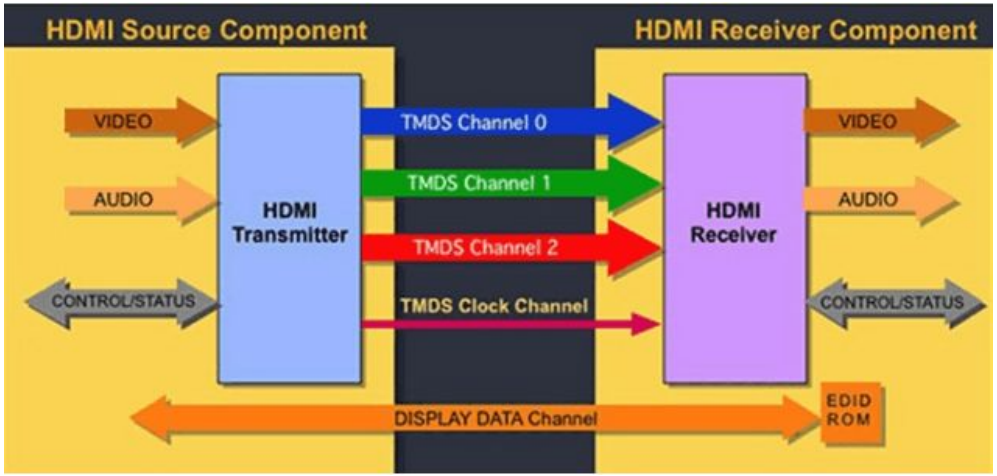
	Pin#	Signal
Blue	1	TMDS data 2+
	2	TMDS data 2 shield
	3	TMDS data 2-
Green	4	TMDS data 1+
	5	TMDS data 1 shield
	6	TMDS data 1-
Red	7	TMDS data 0+
	8	TMDS data 0 shield
	9	TMDS data 0-
	10	TMDS clock+

Pin#	Signal	
11	TMDS clock shield	Clock
12	TMDS clock-	
13	CEC	
14	No connected	
15	DDC clock	Display Data Channel (for encryption key exchange)
16	DDC data	
17	Ground	
18	+5V power	
19	Hot plug detect	Notify Device of Connection

http://articles.triplewidemedia.com/choosing-right-video-cable-hdmi/

HDMI Transmits More Than Video

- Audio is encoded in the RGB channels
- Display Data Channel
  - Resolution
  - Aspect ratio
  - Serial number
  - Encryption data



https://www.cablestogo.com/learning/library/digital-signage/intro-to-tmds

3 Big Takeaways

3 Big Takeaways

1. VGA was created for analog displays
2. Even for simple protocols, memory and latency requirements necessitate unconventional approaches
3. HDMI can encode audio and continues to increase bandwidth capabilities to support higher quality displays

Where To Learn More

VGA:
https://www.youtube.com/watch?v=wzhDRIX2Ors
HMDI Overview:
https://www.audioholics.com/hdtv-formats/hdmi-interface-a-beginners-guide
HDMI More in Depth:
https://www.cablestogo.com/learning/library/digital-signage/intro-to-tmds
HDMI Eye-pattern, cable, and speed:
https://www.fpga4fun.com/files/HDMI_Demystified_rev_1_02.pdf

Any Questions?

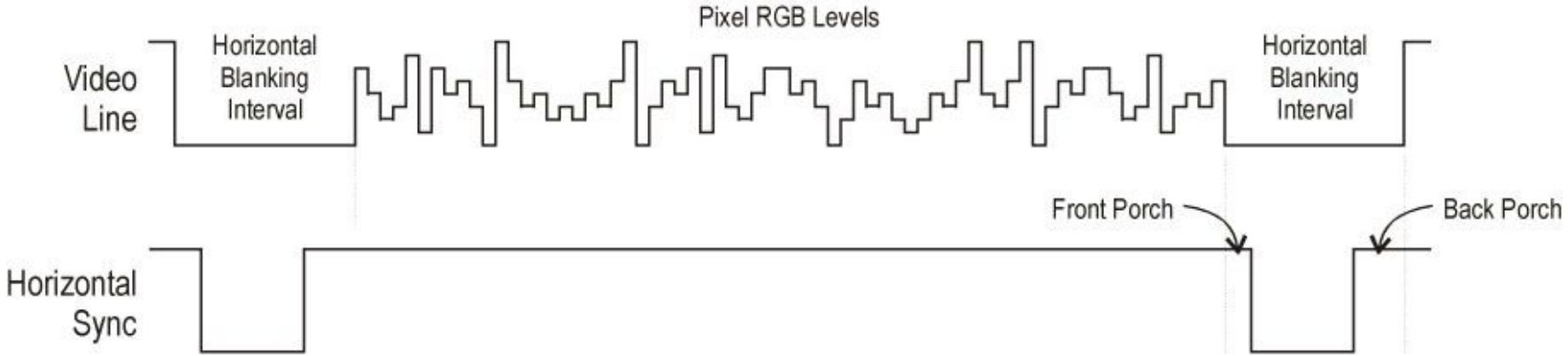
Takeaways:

1. VGA was created for analog displays
2. Even for simple protocols, memory and latency requirements necessitate unconventional approaches
3. HDMI can encode audio and continues to increase bandwidth capabilities to support higher quality displays

Any Questions?

Bonus: Coding The Verilog

1. Use a counter that increments every pixel to generate the horizontal sync signal
2. Use a counter that increments every line to generate vertical sync signal
3. Drive R, G, and B low if in the front porch or sync pulse
4. Drive R, G, and B to appropriate levels if in the visible region
   a. Helper function that considers the current location to find the pixel color
   b. Image stored in memory



http://www.eecg.toronto.edu/~tm4/rgbout.html

Control data encoding

Input control bit		Output codeword
C0	**C1**	**0 ... 9**
0	0	0010101011
0	1	0010101010
1	0	1101010100
1	1	1101010101

On Channel 0 the C0 and C1 bits encode the HSync and VSync signals. On the other channels they encode the CTL0 through CTL3 signals which are unused by DVI but in the case of HDMI are used as a preamble indicating the type of data about to be transferred (Video Data or Data Island), the HDCP status and so on.

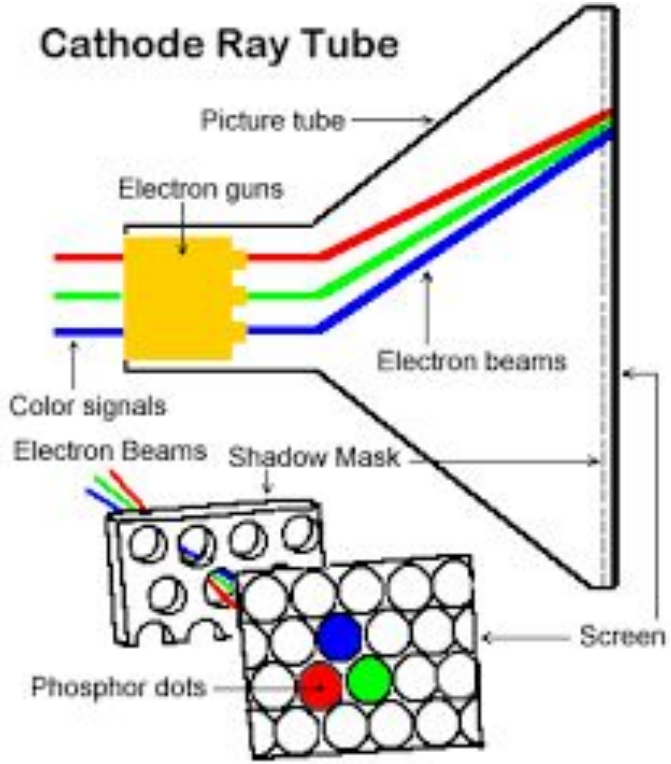
HDMI Fun Fact

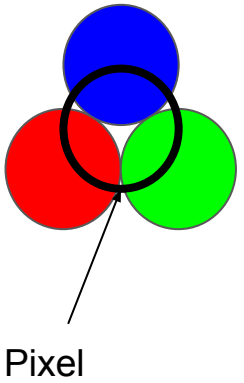
HDMI is not free

- $10,000 fee
- $0.04-0.15 per-unit royalty

https://images-na.ssl-images-amazon.com/images/I/712Bi59beRL._SX425_.jpg

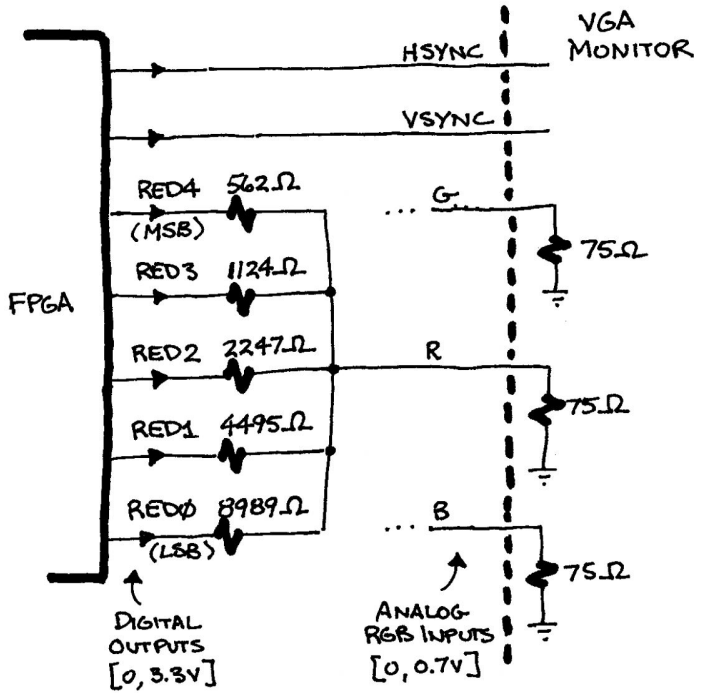
Color Mixing





https://encrypted-tbn0.gstatic.com/images?q=tbn:ANd9GcR7tOO7iLTDaJssTkBcls4JdH6_FmQpydjbM7zTJ7iTGum0fFh2

Clearly better explanation about DAC and ADC



http://www.xess.com/blog/a-simple-vga-interface-for-the-xula-fpga-board/